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A new universal gate for low power SoC applications

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Abstract. This paper formulates a new design technique for an area and energy efficient Universal NAND gate. The proposed robust three transistors (3T) based NAND gate is just as effective for dynamic power control in CMOS VLSI circuits for System on Chip (SoC) applications. The 3T NAND gate is intuitively momentous and lead to better performance measures in terms of dynamic power, reduced area and high speed while maintaining comparable performance than the other available NAND gate logic structures. Simulation tests were performed by employing standard Berkeley Predictive Technology Model (BPTM) 22 nm, 45 nm and 90 nm process technologies. The experiment and simulation results show that, the proposed 3T NAND gate effectively outperforms the basic CMOS NAND gate with excellent driving capability and signal integrity with exact output logic levels.

Keywords. Low power; CMOS; pass-transistor; NAND gate; Koomey's law.

1. Introduction

Not so long ago, researches were focused on developing portable applications in pursuit of high performance, thus increasing system complexity. Natural fallout of this process has been abridged battery life and long term reliability issues. Analysis of such systems, points to increased power consumption as the main factor (Rabaey & Pedram 1996). Reduction in feature size also causes tunnelling effects. These realizations spurred interest in the area of low power design consequently creating a new field of electronics. Therefore along with area and speed, power consumption is an important criterion in measuring system performance (Goel *et al* 2006; Mariano & Monico 2011; Baskaran *et al* 2011).

The significance of a universal gate is that programmable chips can be made of only one kind of gate, either NAND or NOR gate making manufacturing process simple and reducing the number of different processors required to make a computer. The benefit of utilizing a combination

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of low-power components in conjunction with low-power design methodologies is more important now than ever before. Low power requirements continue to grow extensively as components become battery-powered, smaller and require more functionality. Koomey's law describes a long-term trend in the history of computing hardware and has actually been somewhat faster than Moore's law. Jonathan Koomey articulated the trend as follows: 'at a fixed computing load, the amount of battery you need will fall by a factor of two every year and a half' (Koomey Jonathan *et al* 2011).

In order to realize ultra low power SoC applications, circuits should be operated with low power dissipating gates. In reality, digital control systems have been designed approximately with either NAND or NOR gates, all the essential logic functions being derived from collections of interconnected NANDs or NORs. Low power and high reliability needs along with cost/performance advantages make NAND flash memory the ideal data storage solution for portable electronic devices. Designers are progressively more turning to embedded NAND solutions for dynamic, on-board storage. To support the ever-changing needs of current and emerging applications, the authors have developed the most appropriate NAND solution for these applications.

In this work, we present a circuit level design technique for universal NAND gate that reduces the overall dynamic power with reduced switching transistor count. The proposed design of 3T NAND gate is based on CMOS inverter and Pass Transistor Logic. The rest of the paper is organized as follows, in section 2, a review of CMOS Inverter and Pass Transistor Logic (PTL) is presented. In section 3, the proposed work on a 3T NAND gate is presented, which is followed by the simulation results and conclusions in sections 4 and 5, respectively.

2. Review of CMOS inverter and PTL

CMOS inverters are some of the most largely used and adaptable MOSFET inverters in chip designing. They operate with minimal power loss and at relatively high speed (Franco Maloberti 2001). Furthermore, the CMOS inverter has good logic buffer characteristics in that. Its noise margins are large in both low and high states. A CMOS inverter shown in figure 1 contains a PMOS and a NMOS devices connected at the drain and gate terminals, a supply voltage VDD

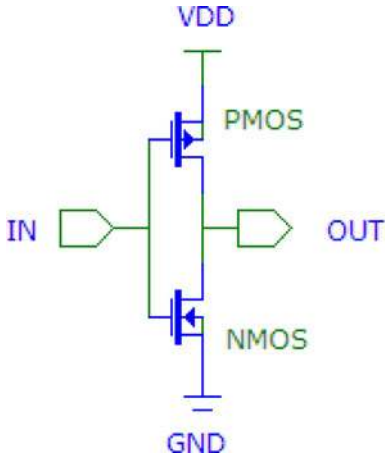

Figure 1. CMOS inverter.

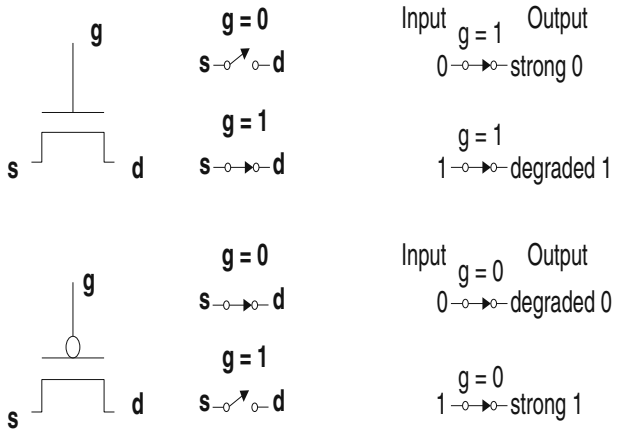

Figure 2. Pass transistor logic.

at the PMOS source terminal, and a ground connected at the NMOS source terminal, were IN is connected to the gate terminals and OUT is connected to the drain terminals (Franco Maloberti 2001). As the input to the inverter varies between logic 0 and logic 1, the state of the NMOS and PMOS varies accordingly to make output as logic 1 and logic 0, respectively.

The most popular and widely used alternative to complementary CMOS is pass-transistor logic. Pass-transistor logic attempts to decrease the quantity of transistors necessary to realize the logic by allowing the principal inputs to drive gate terminals (Radhakrishnan *et al* 1985; Srinivasan *et al* 2012) as well as drain/source terminals as shown in figure 2. It is observed from figure 2 that when the device getting used as a pass-transistor may conduct current in either direction. The NMOS transistors pass a strong logic 0 but a weak logic 1 (threshold voltage drop. High = VDD -V_{thn}) and PMOS transistors pass a strong logic 1 but a weak logic 0 (threshold voltage drop. Low = V_{thp}). Thus, NMOS switches are best for pull-down network and the PMOS switches are best for pull-up network.

3. Proposed 3T NAND design

The new design of 3T NAND gate is shown in figure 3. The high density layout, speed and compact design advantages of PTL and CMOS inverter design style can be utilized efficiently to design 3T NAND circuit. The 3T NAND functionality can be explained as follows.

- The PMOS M1 and NMOS M2 on the left form a modified CMOS inverter structure. The PMOS M3 on the right acts as a pass transistor.
- When A=1, M3 is OFF and the modified inverter on the left (M1 & M2) functions as a normal CMOS inverter. Therefore, the output is the complement of input B.
- When A=0 & B=0, M2 is OFF, M1 and M3 are ON which leads to an undefined output state 'X', because M1 tends to pull down the output node while M3 tends to pull up the output node.

  Similarly when A=0 & B=1, M1 is OFF, M2 and M3 are ON leading to an undefined output state 'X', because M2 tends to pull down the output node while M3 tends to pull up the output node.

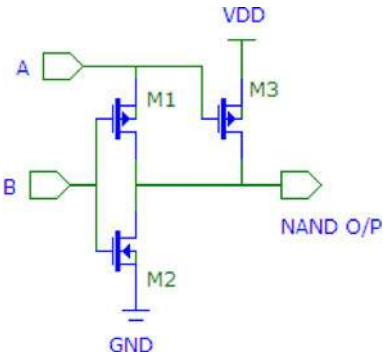

Figure 3. 3T NAND.

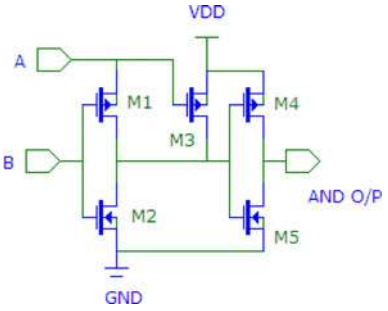

Figure 4. AND gate.

- For A=0 & B=0 or 1, a strong logic '1' output is required. It is possible to obtain exact output logic levels with the proposed circuit, if the channel width of M3 is made 6 times that of M2 or 3 times that of M1. That is

$$W_{M3} = 6 \times W_{M2} = 3 \times W_{M1}.$$

Thus, M3 becomes much stronger than M1 and M2, giving a strong logic '1' at output when input A=0.

The proposed 3T NAND gate is exempted from body bias effect, as there is no stacking of transistors. Exact output logic levels are attained for all the input combinations without any voltage degradation. An AND gate operation could be obtained with an additional CMOS inverter at the NAND output with 5 transistors totally as shown in figure 4.

4. Simulation results

The Performance of the 3T NAND gate is evaluated based on its power dissipation, delay and power delay product (PDP) compared with conventional CMOS four transistors (4T) NAND gate. Schematics are designed for all circuits using Custom Designer in Synopsys for TSMC 0.18 μm technology. The original netlists obtained from the schematics are modified according to BPTM 22 nm process technology (Geetha Priya *et al* 2012). The modified netlists are simulated using Synopsys HSPICE for power and delay estimations.

Table 1. Simulation results of NAND gates compared (power in W, delay in pS and PDP in J).

Process Tech.	90 nm @ VDD=1.2 V		45 nm @ VDD=0.5 V		22 nm @ VDD=0.2 V	
Parameters	3T NAND	4T CMOS NAND	3T NAND	4TCMOS NAND	3T NAND	4TCMOS NAND
Dynamic power	8.4200 E-09	10.2812 E-09	4.9058 E-11	6.1356 E-11	1.8661 E-12	2.4743 E-12
Delay	54.8	75.2	43.6	59.4	38.2	47.1
$PDP_{dynamic}$	461.4 E-21	773.1 E-21	213.8 E-23	364.4 E-23	71.2 E-24	116.5 E-24

All devices used are of standard threshold voltage (Vth) and the operating temperature taken is 27°C. The 3T NAND gate ensures optimum performance for frequency range between 50 MHz and 0.3 GHz. All the results were simulated and analysed in the range of 125 MHz to 0.25 GHz. Table 1 shows the simulation results of 3T & 4T NAND gates compared at 90 nm, 45 nm and 22 nm process technology (Zhao & Cao 2006). Dynamic power dissipation is estimated by applying all four possible input vectors (00, 01, 10 and 11) arbitrarily. Table 2 gives the simulation results of 3T NAND at 22 nm process for various supply voltages (0.2 V, 0.45 V, 0.6 V and 0.75 V).

For 0.022 μm (22 nm) process, the length of the channel for all transistors was taken as L = 0.022 μm, channel width of M1, $W_{M1} = 0.200$ μm, channel width of M2, $W_{M2} = 0.100$ μm, and channel width of M3, $W_{M3} = 0.600$ μm.

For 0.045 μm (45 nm) process, the length of the channel for all transistors was taken as L = 0.045 μm, channel width of M1, $W_{M1} = 1.000$ μm, channel width of M2, $W_{M2} = 0.500$ μm, and channel width of M3, $W_{M3} = 3.000$ μm.

For 0.090 μm (90 nm) process, the length of the channel for all transistors was taken as L = 0.090 μm, channel width of M1, $W_{M1} = 2.000$ μm, channel width of M2, $W_{M2} = 1.000$ μm, and channel width of M3, $W_{M3} = 6.000$ μm.

Figure 5 shows transfer characteristics for proposed 3T NAND gate with perfect output logic levels without any voltage degradation. Figure 6 gives the power savings of 3T NAND gate showing an improvement of more than 22% of less power consumption over conventional CMOS NAND Gate (4T) as the process technology diminishes.

From table 1, we can state the following.

- Considering the power dissipation, 3T NAND gate shows less dynamic power dissipation compared to conventional CMOS NAND gate. The reduction in dynamic power dissipation comes from the fact of reduced internal capacitances as transistors count is less, which results in less glitches at the outputs.

Table 2. Simulation results of 3T NAND gate @ 0.022 μm (22 nm) for various supply voltages (supply voltage in V, power in W and delay in pS).

Supply voltage	Dynamic power	Delay	Average power for various input vectors			
			00	01	10	11
0.2	1.0661 E-12	38.2	3.0021 E-13	5.8750 E-13	1.7239 E-13	1.4215 E-14
0.45	5.8167 E-12	37.4	6.7812 E-13	9.0081 E-13	5.0414 E-13	4.6900 E-14
0.6	10.6535 E-12	37.0	9.3406 E-13	11.1775 E-13	8.6580 E-13	7.8640 E-14
0.75	16.3971 E-12	36.6	11.3810 E-13	12.3462 E-13	9.4174 E-13	10.8979 E-14

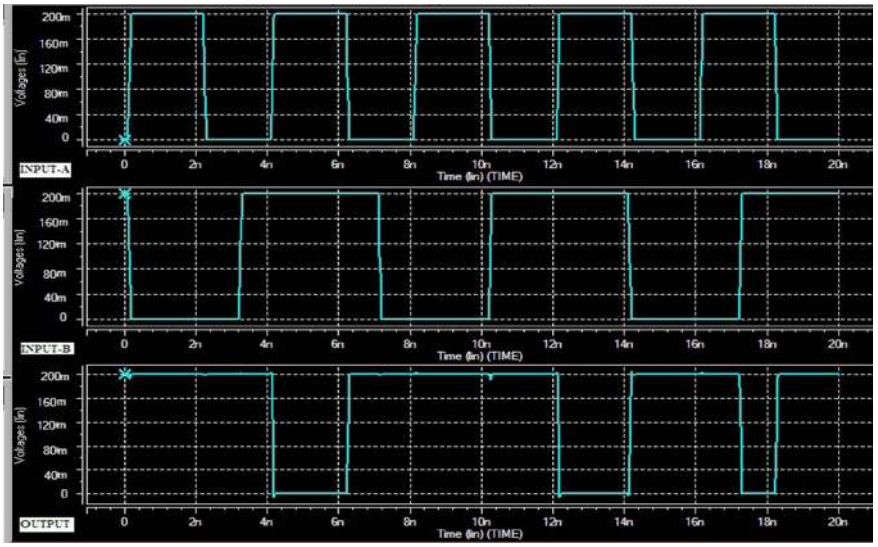

Figure 5. Transfer characteristics of 3T NAND gate @ 22 nm.

- With regards to the speed, it can be seen that the benefit of the pass transistor logic structure introduced here, exhibiting the smallest propagation delay than CMOS NAND gate.
- The power-delay product (PDP) column confirms the energy-efficiency for the 3T NAND gate built using the new logic structure. This presents the lowest PDP metric, due to the combined reduction of power consumption and propagation delay.

From table 2, we can state the following.

- We have carried out a separate set of simulations to determine the maximum power supply voltage that 3T NAND gate can tolerate at 0.022 μm (22 nm) process technology while maintaining its correct functionality. As shown in column supply voltage, the proposed NAND can operate properly with 0.2 to 0.8 V supply voltage.

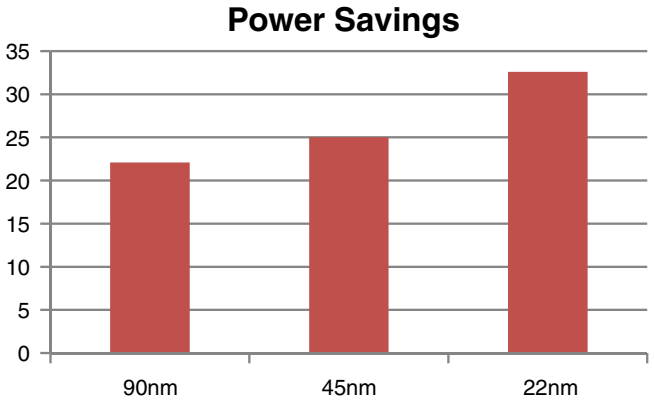

Figure 6. Power savings of 3T NAND gate.

- With increase in supply voltage, the dynamic power increases and the delay improves.
- The average power column for different input vectors shows the fact that subthreshold leakage is dependent on input vectors.
- With respect to the implementation area, it can be seen that the proposed NAND gate required the smallest area due to less transistor count, which can also be considered as one of the factors for presenting lower delay and power consumption.
- It is a good candidate for battery-operated applications where low dissipation modules with standby modes are required.

5. Conclusion

This paper presents features of 3T NAND gate based on PTL and CMOS logic. HSPICE simulations at 22 nm showed power savings up to 32.6% and speed improvements up to 23%, for a joint optimization of 63% for the PDP. Throughout logic design, the proposed 3T NAND gate could be used to reduce the dynamic power of VLSI SoC circuits.

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