Approach to suppress ambipolar conduction in Tunnel FET using dielectric pocket

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The impact of high-*k* dielectric pocket (DP) on the ambipolar conduction of tunnel field-effect transistors (TFETs) is demonstrated using two-dimensional Technology Computer Aided Design (TCAD) simulations. In the proposed structure of TFETs, an optimised portion of the upper drain region is replaced with a high-*k* DP at the channel–drain interface. It is demonstrated that due to the enhancement of the depleted drain region under DP, the minimum tunnelling width at channel–drain interface increases, and attains a maximum value for an optimum length and thickness of DP. Eventually, this increment in the minimum tunnelling width leads to a significant reduction in ambipolar conduction in TFETs. Furthermore, it is shown that performance parameters including the ON-state current, subthreshold swing and output characteristics are not affected by the presence of the proposed DP. Even, the gate-to-drain capacitance is reduced with the inclusion of DP at the channel–drain interface, thus leading to an improved cut-off frequency of TFETs. Moreover, it is also demonstrated that only a 10 nm of gate-on-drain overlapping along with this DP is capable of eliminating the ambipolarity completely for even a higher gate voltage of −0.8 V.

1. Introduction: To achieve high switching speed and low power consumption, the feature size of metal–oxide–semiconductor field-effect transistors (MOSFETs) used in complementary MOS (CMOS) technology is aggressively scaled down to tens of nanometres. Owing to the continuous scaling of device dimensions, conventional MOSFETs face some critical problems such as short channel effects and large standby power dissipation [1]. A conventional MOSFET even suffers from the limitation of subthreshold swing to 60 mV/decade due to its current transport mechanism based on the thermionic injection of charge carriers over source–channel energy barrier [2]. Owing to these challenges in MOSFETs, an alternative device is needed for the future requirement of low power application in CMOS technology. Among the next generation of the devices proposed by researchers, a TFET is regarded as one of the most promising successors of a conventional MOSFET [3]. The band-to-band tunnelling (BTBT) mechanism of current transport empowers TFETs to overcome the aforementioned limitations faced by a conventional MOSFET [4]. A TFET is found to have some excellence over the conventional MOSFETs such as low subthreshold leakage current, sheer subthreshold swing and most importantly resilience to short channel effects, thus making it more suitable for the future requirement of high switching speed and low standby power devices. Regardless of all the advantages, TFETs have two major drawbacks such as low ON-state current and ambipolar conduction at channel–drain junction [5]. The researchers have already suggested some techniques to improve the ON-state current of TFETs such as using a source pocket at the source–channel junction, double-gate structure, high-*k* gate dielectric or using a source material of lower bandgap than that of the channel [6–9]. Several techniques such as gate dielectric engineering, gate–drain underlap and overlap, drain doping engineering, gate work function engineering, spacer engineering etc. have been demonstrated to eliminate the ambipolar conduction at channel–drain junction [10–22]. Although all these techniques are able to reduce the ambipolar conduction at the cost of degradation in analogue and/or high-frequency (HF) performances. Even some of these techniques are found to have the drawbacks such as fabrication complexity, and increased drain resistance which reduces the ON-state current of TFETs. For example, a heavily doped pocket at channel–drain interface reduces the ambipolarity in TFETs but this reduction comes at the cost of an increment in gate-to-drain capacitance $\left(C_{\mathrm{gd}}\right)$ which, further, degrades the HF performances of TFETs [12]. Similarly, a technique of gate-on-drain overlapping (OL) is demonstrated to suppress the ambipolar conduction in TFETs up to a gate voltage of −0.5 V when a minimum OL length of 30 nm is used; thus, limiting the scalability of the drain region. Even, the gate-to-drain capacitance is also increased for the device proposed with larger gate-on-drain OL which results in limited HF performances [15]. Again, a technique based on gate–drain underlap is found promising for the reduction of ambipolar conduction in TFETs by lowering the energy band of the channel at the channel–drain interface. It also reduces the gate-to-drain capacitance which, further, improves the HF performances of TFETs. However, the requirement of minimum gate underlap length to suppress ambipolarity limits the scaling of channel length in TFETs [21]. Using drain doping engineering, another method is proposed based on Gaussian doping in the drain region which offers improved device performances of TFETs [22]. However, the physical implementation of an asymmetric Gaussian doping is very complex in nature. So it can be concluded that even after much exhaustive research on TFETs, we still needs to find a suitable structure with proper material engineering to achieve better device performances.

In this work, we have proposed a novel structure of n-channel single-gate TFET (SG-TFET) to reduce the ambipolarity using a high-*k* dielectric pocket (DP) in the drain region. A number of works have been reported showing a reduction in the short channel effects, subthreshold leakage current and lateral electric field at a channel–drain junction in MOSFETs with the help of DP [23–26]. In this work, however, DP has been used for different purpose. The proposed device, DP SG-TFET, is expected to reduce the ambipolar conduction with the help of depleted drain region under DP at the channel–drain junction. In this work, we have compared our proposed structure with the conventional SG-TFET to demonstrate the impact of DP on device performances. Through two-dimensional (2D) TCAD simulations, we have shown that the proposed structure completely removes the ambipolar conduction up to a negative gate voltage −0.5 V without deteriorating the ON-state current, and subthreshold swing. Furthermore, we have demonstrated the impact of gate-on-drain OL along with DP which shows a huge reduction in the ambipolar conduction.

2. Device structure and simulation approach: The 2D cross-sectional view of the conventional n-channel SG-TFET and

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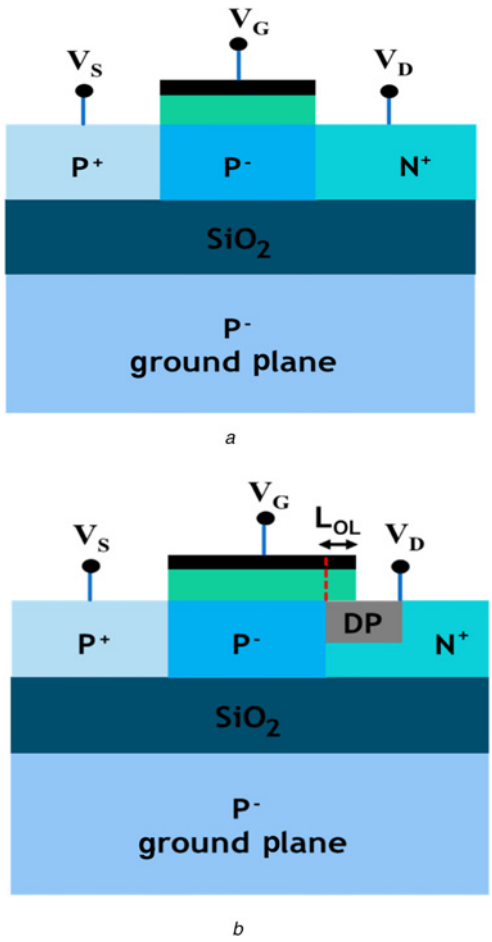

Fig. 1 *Cross-sectional view of*
a Conventional
b Proposed structure of SG-TFETs

proposed DP SG-TFET are shown in Fig. 1. As compared to the conventional SG-TFET, drain region of the proposed structure has been scaled down with an optimum length (L_{DP}) and thickness (T_{DP}). Furthermore, a high-k DP of the same length and thickness has been mounted above the scaled drain region. This is the only structural difference between the proposed and conventional SG-TFETs. Table 1 has listed the details of all design parameters used for these two structures in our simulations.

Table 1 List of parameters taken for device simulations

Parameters	SG-TFET	DP SG-TFET
gate length, nm	50	50
gate work function, eV	4.3	4.3
source and drain lengths, nm	100	100
source doping (N_A), cm^{-3}	1×10^{20}	1×10^{20}
channel doping (N_A), cm^{-3}	1×10^{16}	1×10^{16}
drain doping (N_D), cm^{-3}	5×10^{18}	5×10^{18}
gate oxide thickness (t_{OX}) silicon dioxide (SiO_2), nm	2	2
Silicon-On-Insulator (SOI) thickness (t_{Si}), nm	10	10
oxide thickness (t_{SiO2}) of SOI, nm	25	25
ground plane doping (N_A), cm^{-3}	1×10^{16}	1×10^{16}
DP (HfO_2) length, nm	—	30
DP (HfO_2) thickness, nm	—	5
dielectric constant of HfO_2	—	25

The fabrication process of the proposed device is similar to that of the conventional SG-TFET, except for an additional step for fabricating DP in the drain region. The fabrication of DP in source and drain regions for MOSFETs has been proposed by many researchers in the past, which ensures the fabrication feasibility of our proposed device [23–26]. A DP in drain region can be fabricated based on the method reported by *Jurczak et al.* in their work [24]. First, a depression of 5 nm in drain region can be performed using anisotropic plasma etching to define the thickness of DP. Then, DP can be deposited in a depression created inside the drain using plasma-enhanced chemical vapour deposition technique. After deposition of DP, the excess part of the depression region formed during the etching process is now refilled using selective epitaxial growth technique.

In this Letter, all the simulations have been performed using *Synopsys sentaurus* simulator [27]. The operation of TFETs mainly depends on the BTBT mechanism. The local BTBT model assumes the lateral electric field to be constant for the entire tunnelling region by approximating the tunnelling barrier as a triangular one. However, a non-local dynamic BTBT model considers the change of electric field for each point in the tunnelling region. Therefore, we have used a non-local dynamic BTBT model for accurate simulation of BTBT current in TFET. To include the impact of heavily doped source and drain regions, the bandgap narrowing model has also been enabled. Shockley–Red–Hall recombination, concentration-dependent mobility, electric field-dependent mobility and auger recombination have been included too. The BTBT model parameters have been carefully calibrated with the results published by Boucart and Ionescu [8].

3. Results and discussion: For different values of DP thickness, a comparison of transfer characteristics between the proposed and conventional SG-TFETs is presented in Fig. 2. The ambipolar conduction at channel–drain interface mainly depends on the rate of charge carriers tunnelling across the interface. The presence of a DP above scaled drain terminal provokes more depletion in the underlying drain region at channel–drain interface which, further, results in the reduction of band OL between drain and channel regions. Eventually, the reduction in band OL prevents the charge carriers to tunnel across the channel–drain interface, thus leading to a notable reduction in ambipolar conduction in TFETs even at a large value of negative gate voltage. During simulations, length of DP is kept fixed to an optimum value of 30 nm which is discussed later. Since, a high-k dielectric material has more impact on the electrostatic behaviours in the drain region under DP, hafnium oxide is preferred over silicon dioxide. As we can observe from Fig. 2 that the ambipolarity is approximately eliminated up to a gate voltage of −0.5 V for 5 nm of T_{DP}.

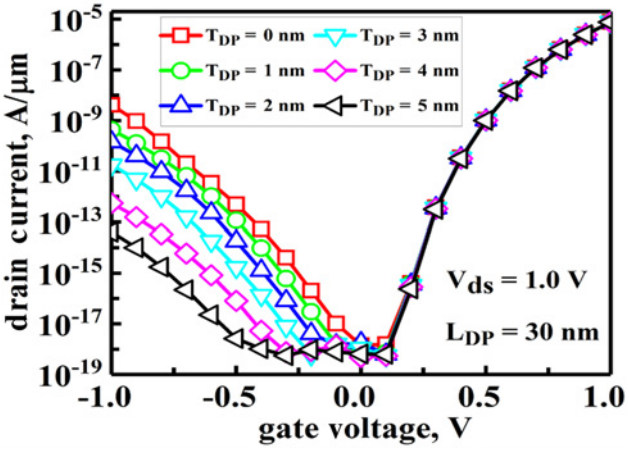

Fig. 2 *Transfer characteristics of the proposed device for varying* T_{DP}

Furthermore, we have noted that the value of ambipolar current for the proposed structure is very low compared with the conventional one for a gate voltage of −1.0 V. For the purpose of comparative analysis, the values of different performance parameters for the proposed and conventional structures are listed in Table 2. For more insight into the DP effect, Fig. 3 shows a comparison of the energy band diagrams for T_{DP} varying from 0 to 5 nm. We can observe from this figure that the minimum tunnelling width (W_{min}) increases with an increment in T_{DP}. The increased value of W_{min} causes a significant reduction in band OL of the channel and drain regions, which, further, lead to a reduction in tunnelling probability at the channel–drain interface.

For a comprehensive analysis, the lateral electric field of the proposed structure penetrating from drain to channel region is compared with the conventional one for varying T_{DP}. It is observed from Fig. 4 that the maximum electric field at channel–drain interface decreases with an increment in T_{DP}, thus leading to a reduction in the charge carriers tunnelling across the interface. As compared to the conventional SG-TFET, electric field at the channel–drain interface in the proposed structure is mostly shared by the depleted drain region formed under DP which, further, leads to a reduction in the lateral electric field at the channel–drain interface.

Next, the impact of varying L_{DP} on transfer characteristics is shown in Fig. 5. During the simulations, T_{DP} is kept fixed at its optimum value of 5 nm. It is observed from this figure that when L_{DP} is increased from 0 to 30 nm, ambipolar current (I_{amb}) is decreased from 4.16×10^{-9} to 4.15×10^{-14} A. Furthermore, it is found that the decrement in I_{amb} with increasing L_{DP} is not significant for $L_{DP} > 30$ nm. For more insight, Fig. 6 compares the energy band diagram for varying L_{DP}. It is evident from this figure that the minimum tunnelling width at channel–drain interface increases when L_{DP} is increased from 0 to 30 nm, thus leading to a significant reduction in I_{amb}. Since, W_{min} mainly depends on the depletion created in drain region at channel–drain interface, which attains the maximum value at $L_{DP} = 30$ nm, no further significant reduction in I_{amb} is noted for $L_{DP} > 30$ nm.

Table 2 Performance comparison of the conventional SG-TFET, DP SG-TFET, and DP SG-TFET with gate-on-drain OL

Performance parameters	SG-TFET	DP SG-TFET	DP SG-TFET with OL
I_{ON}, A	7.76×10^{-6}	7.76×10^{-6}	7.73×10^{-6}
I_{OFF}, A	1.41×10^{-18}	6.43×10^{-19}	4.57×10^{-19}
SS_{avg}, mV/decade	54	53.6	54.2
V_{th}, V	0.725	0.716	0.723
I_{amb}, A	4.16×10^{-9}	4.15×10^{-14}	3.39×10^{-16}

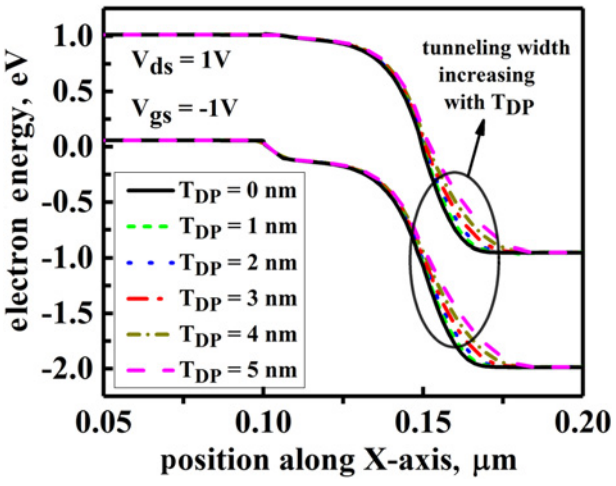

Fig. 3 *Comparison of energy band profiles of the proposed device with conventional one for varying T_{DP}*

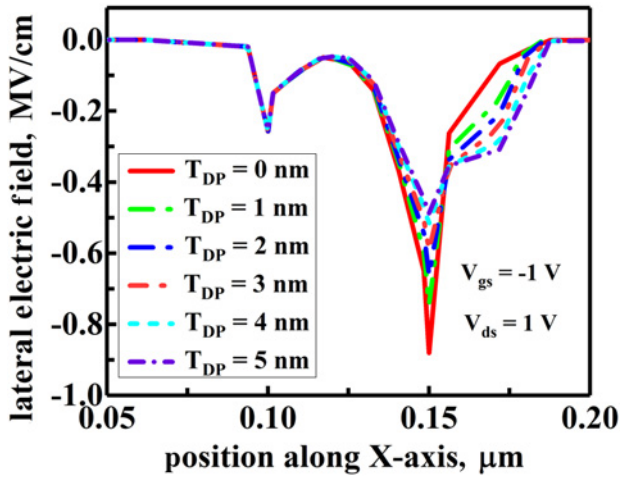

Fig. 4 *Comparison of lateral electric field of the proposed device with conventional one for varying T_{DP}*

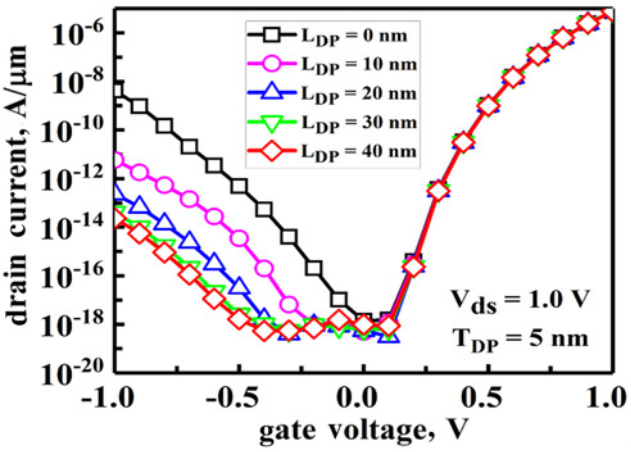

Fig. 5 *Transfer characteristics of the proposed device for varying L_{DP}*

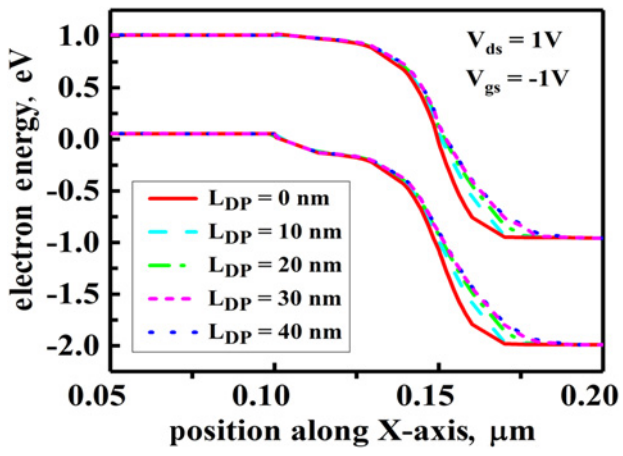

Fig. 6 *Comparison of energy band profiles of the proposed device with conventional one for varying L_{DP}*

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Additionally, Fig. 7 compares the output characteristics of the proposed structure with conventional SG-TFET for the different gate voltages. It is observed from this figure that DP has no significant impact on the output characteristics of SG-TFET, which is another advantage of the proposed structure. So, it can be concluded that our proposed structure yields enormous reduction in I_{amb} without degrading I_{ON}, Subthreshold Swing (SS), and/or output characteristics.

Furthermore, to demonstrate the impact of DP on the subthreshold current of TFETs, Fig. 8 compares the transfer characteristics of the proposed structure with conventional one if the channel of the device is scaled down to a shorter length. It can be noted from this figure that our proposed structure offers a lower subthreshold current than that of the conventional one for 30 nm of channel length which, in turn, results in the reduction of standby power dissipation in TFETs. Since, as shown in Fig. 4, the lateral electric field penetrating from drain to channel region is reduced with the presence of DP nearby the channel–drain interface, subthreshold current is reduced for the proposed structure. Owing to the presence of DP on the drain side and channel length downscaling both have no impact on the charge carriers tunnelling from source to channel region, I_{ON} is found to be nearly same for the proposed and conventional SG-TFET with different channel lengths. Next, the impact of gate-on-drain OL along with DP on the device performances is

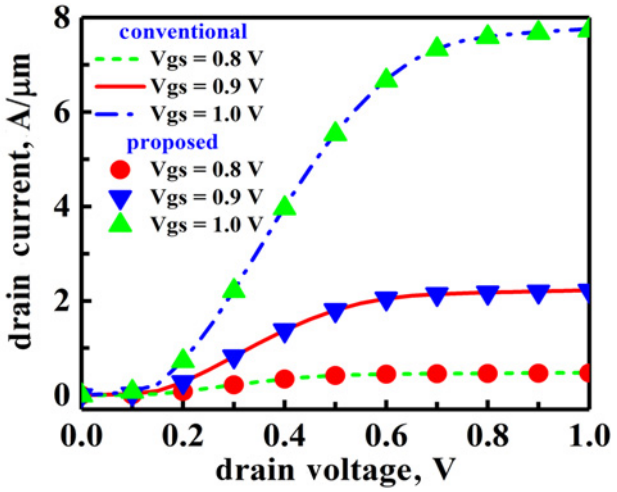

Fig. 7 *Comparison of output characteristics of the proposed device with conventional one for different V_{gs}*

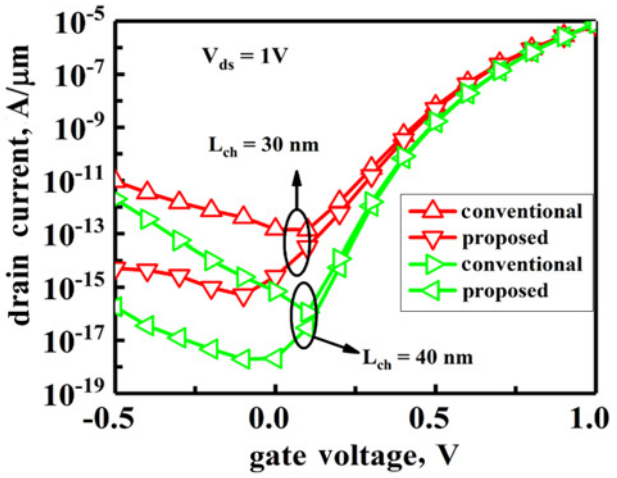

Fig. 8 *Comparison of subthreshold current of the proposed device with conventional one for two short channel lengths of 30 and 40 nm*

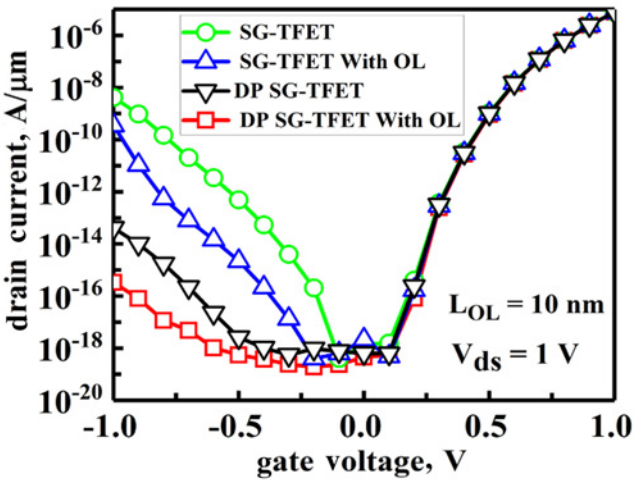

Fig. 9 *Transfer characteristics comparison of the proposed device with conventional one with and without gate-on-drain OL*

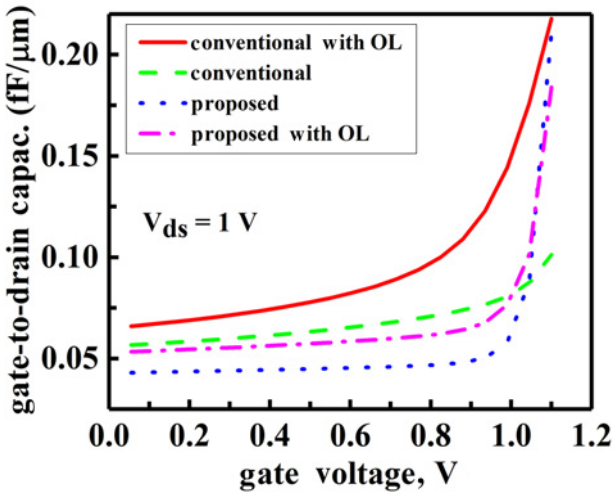

Fig. 10 *Comparison of the gate-to-drain capacitance of the proposed device with conventional one with and without gate-on-drain OL*

investigated. Gate-on-drain OL technique was first proposed by Abdi and Kumar to control the ambipolar conduction in TFETs [12]. However, this technique needs a larger length of the drain region to reduce I_{amb} significantly, which, in turn, limits the scaling of TFETs. Additionally, this technique increases the gate-to-drain capacitance $\left(C_{gd}\right)$ of TFETs, which, further, degrades the cut-off frequency. On the other hand, as shown in Fig. 9, the ambipolar conduction for our proposed structure is completely eliminated using only 10 nm of gate-on-drain OL along with DP up to a gate voltage of −0.8 V. Furthermore, it is demonstrated in Fig. 10 that the proposed structure with gate-on-drain OL offers lesser value of C_{gd} compared with conventional SG-TFET, thus improving the HF performances of TFETs. As shown in Fig. 10, the proposed structure without gate-on-drain OL offers smaller value of C_{gd} but a larger value of I_{amb} (as shown in Fig. 9) as compared with the structure with gate-on-drain OL. So, with this small trade-off between ambipolar conduction and HF performance, the proposed structure DP SG-TFET with or without gate-on-drain OL can be considered as the better structure of TFETs.

4. Conclusion: In this Letter, a new structure of SG-TFET with a high-k DP has been proposed to reduce the ambipolar conduction at the channel–drain interface. Using 2D numerical simulations, it

has been comprehensively shown that by using DP above the partially scaled drain region, the ambipolar conduction is eliminated up to a larger negative gate bias compared with the conventional SG-TFET. The design parameters of the proposed device (i.e. DP SG-TFET) such as length and thickness of DP have been optimised through simulations. The impact of these parameters on the device performances have been theoretically explained in details. It has also been demonstrated that the ON-state current, subthreshold slope, and output characteristics are not degraded with the inclusion of DP in the drain region. It has been found that the subthreshold leakage current in SG-TFET is reduced with the presence of DP at the channel–drain interface when the channel length of the device is scaled down. Eventually, a reduction in subthreshold leakage current leads to an improvement in the current switching ratio (I_{ON}/I_{OFF}). Moreover, the gate-to-drain capacitance for the proposed structure has been found to be less compared with the conventional SG-TFET. It has also been demonstrated that by using only 10 nm of gate-on-drain OL along with DP, the ambipolar conduction in SG-TFET can be eliminated up to a higher negative gate bias without deteriorating HF performances.

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