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Bias and geometry optimization of FinFET for RF stability performance

K. Sivasankaran · P.S. Mallick

Abstract This paper presents RF stability of FinFET at particular bias and geometry conditions. The article provides guideline for optimizing the FinFET at RF range. The FinFET geometrical parameters such as gate spacer length, height of silicon fin, and thickness of silicon fin along with gate material work function and bias conditions are adjusted to optimize the device for better stability performance at RF range. The critical frequency (f_k) is obtained for different bias and geometry conditions using numerical simulation. The result shows that the optimized FinFET exhibits good RF stability performance.

Keywords FinFET · Radio frequency · Stability · Numerical simulation

1 Introduction

Scaling of conventional planar MOSFETs down to 50 nm leads to severe Short Channel Effects (SCEs) and loses its gate controllability over the channel. In order to suppress the SCEs and to have better controllability of the channel, SOI devices and multi gate devices were introduced [1, 2]. These devices show better performances in terms of lower SCEs, higher switching speed and lower leakage current. In recent years, FinFETs received much attention because of better $I_{\text{on}}/I_{\text{off}}$ ratio and reduced fabrication complexity as compared to other multi-gate structures [3]. Many works were reported in fabrication and dc characteristics of FinFETs [4, 5]. The capabilities of FinFETs for analog applications are also reported in [6, 7]. Effect of geometrical parameter such as fin height (H_{fin}), fin width (W_{fin}), fin thickness (T_{fin}) and fin spacing (S_{fin}) on RF performance of SOI-FinFET was reported earlier [8]. Similarly, parasitic and geometry optimization of FinFET for RF applications were studied [9]. The impact of extrinsic capacitances on RF performance of FinFET were analyzed using numerical simulation [10]. It was shown that the extrinsic capacitances are larger than intrinsic capacitance which leads to RF performance degradation. However, the studies on the stability performance of FinFET have not received attention which is one of the important parameters for Radio Frequency Integrated Circuit (RFIC) design. In our previous works, we have studied the RF stability of Silicon Nanowire Transistor and symmetric DG-MOSFET [11, 12] and this paper presents the stability model and RF performance of optimized FinFET. The paper organized as follows: In Sect. 2, we have explained device structure and simulation setup followed by explanation of stability factor. The stability model for FinFET is explained in Sect. 3. In Sect. 4, we discuss about the bias and geometry optimization procedure of FinFET and obtained results were presented. Finally, the Sect. 5 concludes the work.

2 Device structure and simulation setup

Figure 1(a) shows the simulated 3D structure of FinFET which has physical channel length (L_g) of 22 nm [13], gate oxide thickness (t_{ox}) of 1 nm, T_{fin} of 8 nm and H_{fin} of 24 nm. The device has a n^+ source and drain region and p-type channel region with doping of 1×10^{20} cm^{-3} and 1×10^{16} cm^{-3} respectively. We have used HfO_2 as gate dielectric and Si_3N_4 as gate spacer. The use of poly-Si electrodes can cause dopant diffusion through high-k

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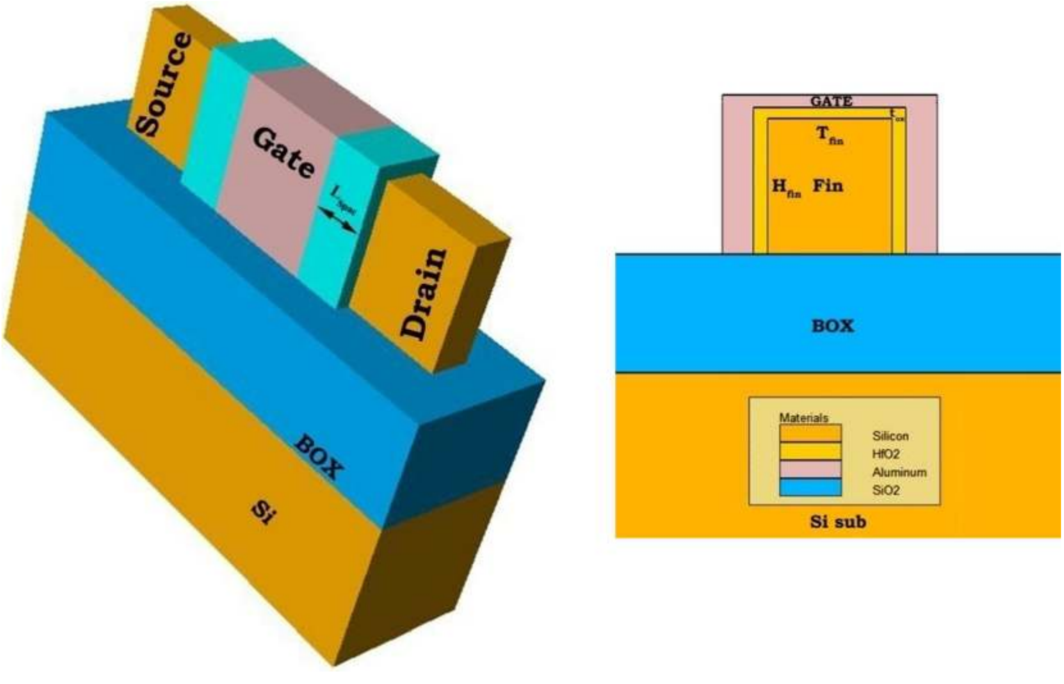


(a) (b)

Fig. 1 (**a**) 3-D Schematic view of FinFET (**b**) Cross-section view of FinFET showing T_{fin}, H_{fin}, t_{ox}, silicon substrate and buried oxide (*BOX*)

gate dielectric which increases capacitance equivalent thickness. We have used molybdenum as gate electrode instead of poly-Si to avoid this problem. In nanoscale FinFET devices, the quantum effects, non-equilibrium conditions, ballistic transport has impact on their performances. The NEGF model allows full quantum mechanical simulation of ballistic transport in nanoscale FinFET devices [14]. As the silicon body cross-section is uniform for the device, we have considered uncoupled mode space approach where NEGF formalism in transport direction is coupled with Schrodinger equation in transverse plane to find eigen energies and eigen functions. The effective mass approximation will reduce the computational complexity for the calculation of electron densities. The electron concentration is computed by solving two-dimensional (2-D) Schrodinger equation for each sub bands propagating from source to drain by providing eigen parameter with the effective mass approximation along Z-direction, assuming that confinement is in the transversal X–Y plane [15]. The threshold voltage (V_t) and $I_{\text{on}}/I_{\text{off}}$ ratio for the FinFET are obtained from dc characteristics and found 0.29 V and $\simeq 10^5$ respectively. The device shows an on current of 566.63 µA/µm in linear scale and off current of 510 pA/µm in log scale. The small signal ac analysis is performed to obtain intrinsic and extrinsic parameters of FinFET. The f_{max}, f_t and stability factor are calculated using extracted parameters. The device simulation is performed using ATLAS TCAD device simulator from Silvaco.

3 Stability factor and modeling

The stability factor, k, gives an indication whether a device conditionally/unconditionally stable. FinFETs are said to be unconditionally stable at any operating frequency above a critical frequency (f_k). Unconditionally stable means that the transistor will not begin to oscillate independently from the value of the signal source and load impedances from any additional passive termination networks at the transistor's input (gate terminal) and output (drain terminal) [16]. At operating frequency below f_k, however, the transistor is conditionally stable and certain termination conditions can cause oscillation. Hence, device must satisfy the condition $k > 1$ to be unconditionally stable [17]. The stability factor is calculated using Y-parameters at different frequencies of operation for the FinFET. The stability factor in terms of Y-parameter can be expressed as [18],

$$k = \frac{2R_e(Y_{11})R_e(Y_{22}) - R_e(Y_{12}Y_{21})}{|Y_{12}.Y_{21}|} \tag{1}$$

The Y-parameters which include all of the small-signal parameters that dominates device behavior of SOI-FinFET can be expressed as [19],

$$Y_{11} = \omega^2\left(R_{gd}C_{gd}^2 + R_{gs}C_{gs}^2\right) + j\omega(C_{gd} + C_{gs}) \tag{2}$$

$$Y_{12} = -\omega^2 R_{gd}C_{gd}^2 - \ j\omega C_{gd} \tag{3}$$

$$Y_{21} = g_m - \omega^2 R_{gd} C_{gd}^2 - j\omega(C_{gd} + g_m \tau_m) \quad (4)$$

$$Y_{22} = g_{ds} + \omega^2 R_{gd} C_{gd}^2 + j\omega\big(C_{sdx} + C_{gd} - L_{sd} g_{ds}^2\big) \quad (5)$$

These Y parameters can be used in Eq. (1) to simplify further as

$$k = \frac{[\omega^2 A + \omega^4 B]^2}{[\omega^4 C - \omega^2 D]^2 + [\omega^3 E - \omega F]^2} \quad (6)$$

where, $A = R_{gd} C_{gd}^2 g_{ds} + R_{gs} C_{gs}^2 g_{ds} - R_{gd} C_{gd}^2 g_m - C_{gd}^2 + C_{gd} g_m \tau_m$, $B = R_{gd} C_{gd}^2 + R_{gd}^2 C_{gd}^4$, $C = R_{gd}^2 C_{gd}^4$, $D = R_{gd} C_{gd}^2 g_m + C_{gd}^2 + C_{gd} g_m \tau_m$, $E = R_{gd} C_{gd}^3 + g_m \tau_m R_{gd} C_{gd}^2$, $F = g_m C_{gd}$, C_{gs} is total gate-to-source, C_{gd} is total gate-to-drain and C_{gg} is total gate capacitance ($C_{gg} = C_{gs} + C_{gd}$), g_m is transconductance, g_{ds} drain to source conductance, R_{gs} is gate-to-source resistance and R_{gd} is gate-to-drain resistance.

Substituting $k = 1$ and solving Eq. (6) by considering the approximation $\omega^2 R_{gd}^2 C_{gd}^2 \ll 1$, $\omega^2 R_{gs}^2 C_{gs}^2 \ll 1$, $\omega^2 g_{ds}^2 L_{sd}^2 \ll 1$ and $\omega^2 \tau_m^2 \ll 1$, we obtain f_k as

$$f_k \cong \frac{f_t}{N\sqrt{g_m(R_{gs}^2 + R_{gd}^2)M + \mathrm{NM}(g_{ds} R_{gs} + g_m R_{gd} + 1)}} \quad (7)$$

where $M = \frac{C_{gs}}{C_{gg}}$, $N = \frac{C_{gd}}{C_{gg}}$, and $f_t = \frac{g_m}{2\pi C_{gg}}$.

The total (intrinsic + extrinsic) gate-to-source (C_{gs})and gate-to-drain (C_{gd}) capacitances without considering overlap capacitance can be calculated as [20],

$$C_{gs} = C_{\mathrm{gsi}} + C_{\mathrm{fext}} + C_{\mathrm{fint}} \quad (8)$$

$$C_{gd} = C_{\mathrm{gdi}} + C_{\mathrm{fext}} + C_{\mathrm{fint}} \quad (9)$$

The internal and external fringing capacitances can be expressed as [21]

$$C_{\mathrm{fint}} = \left[\frac{W\varepsilon_{\mathrm{si}}}{3\pi} \ln\left(1 + \frac{t_{\mathrm{si}}}{2t_{\mathrm{ox}}} \sin\left(\frac{\pi}{2}\frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{si}}}\right)\right)\right] \times e^{-((V_{gs}-V_{FB}-2\varphi_f-V_{ds})/(3/2)\varphi_f)2} \quad (10)$$

$$C_{\mathrm{fext}} = \left[\frac{2W\varepsilon_{\mathrm{ox}}}{3\pi} \ln\left(1 + \frac{t_g}{t_{\mathrm{ox}}}\right)\right] \quad (11)$$

where $\varepsilon_{\mathrm{si}}$ and $\varepsilon_{\mathrm{ox}}$ are dielectric constant of silicon and oxide material; W, t_{si}, t_g and t_{ox} are the width, thickness of silicon body, gate contact and gate oxide respectively. V_{FB} and φ_f are the flat band voltage and Fermi potential respectively. Equation (7) describes the relation between f_k, intrinsic small signal parameters and f_t which help to optimize the device.

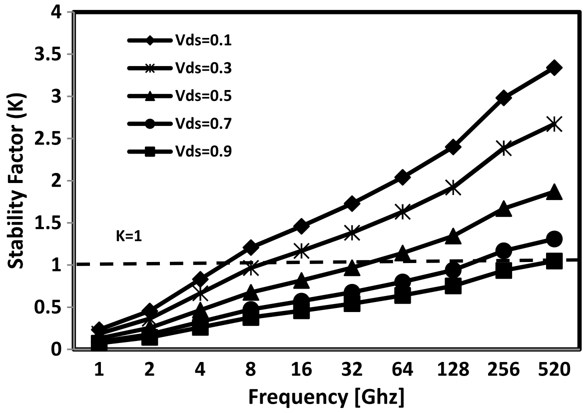


Fig. 2 Extracted stability factor for different V_{ds} at $V_{gs} = 1.5$ V

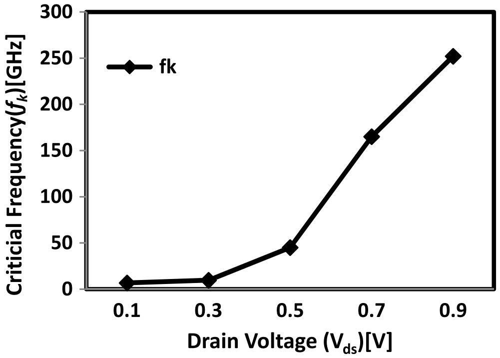


Fig. 3 Critical frequency as a function of drain voltage at $V_{gs} = 1.5$ V

It is evident from Eq. (7) that M and N values can be adjusted to decrease f_k without f_t degradation. The optimization of the FinFET structure lies in study of factors related to M and N, especially C_{gs} and C_{gd}. Equations (8)–(11) shows the bias and geometry dependence on C_{gs} and C_{gd} of FinFET. By adjusting the applied gate and drain bias and geometrical parameters such as aspect ratio (AR), gate spacer length (L_{spac}), along with gate material work function (Φ_m), the FinFET can be optimized for good stability performance.

4 Results and discussion

The stability factor is calculated from extracted Y-parameters for various applied drain (V_{ds}) bias with gate (V_{gs}) bias of 1.5 V which are shown in Fig. 2. It is evident from Fig. 2, FinFET attains unconditionally stable condition at lower V_{ds} since C_{gs} dominates C_{gd} at higher drain bias. Figure 3 shows the extracted f_k for various V_{ds} at $V_{gs} = 1.5$ V. As V_{ds} increases the stability performance degrades since Drain Induced Barrier Lowering (DIBL) affects the device performance at higher V_{ds} and degrades C_{gd}.

It is observed from Fig. 3 that at lower drain bias f_k reaches 6.5 GHz as compared to higher drain bias with f_k greater than 250 GHz. Hence smaller drain bias is preferred to operate the FinFET in RF range with good stability.

Figure 4 shows the extracted stability factor for different gate voltages (V_{gs}) at $V_{ds} = 0.1$ V. It is evident from Fig. 4 for higher V_{gs} FinFET reaches unconditionally stable at earlier frequency as compared to smaller V_{gs}. Further increase in V_{gs}, C_{gs} gets saturates and also affect the parasitic resistance which degrades the RF performance.

It is observed from Fig. 5 that at higher gate bias f_k reaches 32 GHz as compared to smaller gate bias with f_k greater than 450 GHz. Hence higher gate bias is preferred to operate the FinFET in RF range.

Figure 6 shows the extracted stability factor, C_{gd} and C_{gs} (inset) for different gate spacer lengths (L_{spac}). The L_{spac} is given as length of the spacer region covered on either side of silicon fin (source and drain region) adjacent to the gate. The gate spacer improves device sub-threshold characteristics and reduces I_{off}. The reduction in L_{spac} leads to increase in SCEs and has impact on RF stability performance of FinFET. The fringing capacitance increases with smaller L_{spac} but cause oscillation at higher frequency. The FinFET reaches stability at $f_k = 48$ GHz for L_{spac} of 10 nm as C_{gd} and C_{gs} increases with L_{spac}. The increase in L_{spac} shifts the source/drain doping away from the gate edge result in reduced fringing capacitance. Further increase in L_{spac} will not have effect on stability because C_{gd} and C_{gs} saturates for larger L_{spac}, which is due to outer fringing capacitance decrease exponentially with increase in L_{spac} and also has limitations with source and drain region lengths.

Figure 7 shows the extracted stability factor and C_{gd} (inset) for different Φ_m. In FinFET devices the threshold voltage can be tuned by adjusting work function of gate material. The gate material work function can be varied based on gate material with nitrogen implantation dose and energy [22]. C_{gd} increases at lower Φ_m due to capacitive coupling between drain and gate electrodes. At $\Phi_m = 4.5$, FinFET reaches stability at $f_k = 50$ GHz as compared to $\Phi_m = 4.9$ the value of f_k is greater than 100 GHz. C_{gd} decreases with

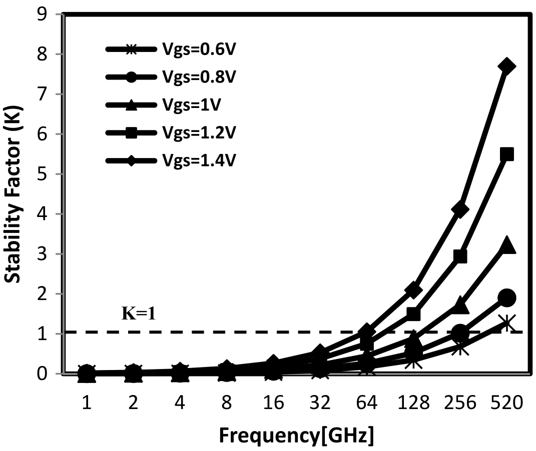


Fig. 4 Extracted stability factor for different V_{gs} at $V_{ds} = 0.1$ V

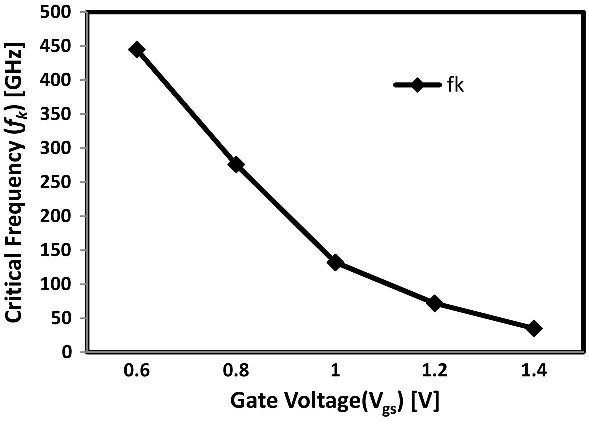


Fig. 5 Critical frequency as a function of gate voltage for $V_{ds} = 0.1$ V

Fig. 6 Extracted stability factor, C_{gs} and C_{gd} (*inset*) for different gate spacer length

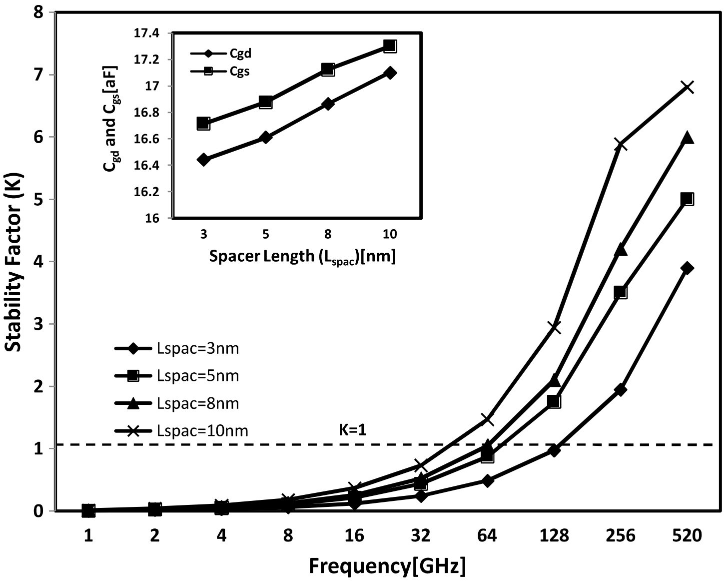


Fig. 7 Extracted stability factor and C_{gd} (*inset*) for different gate work function

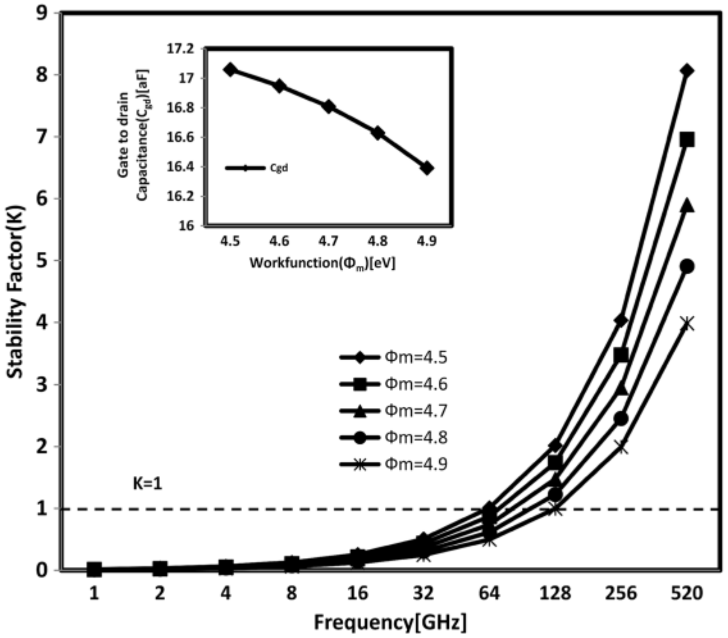
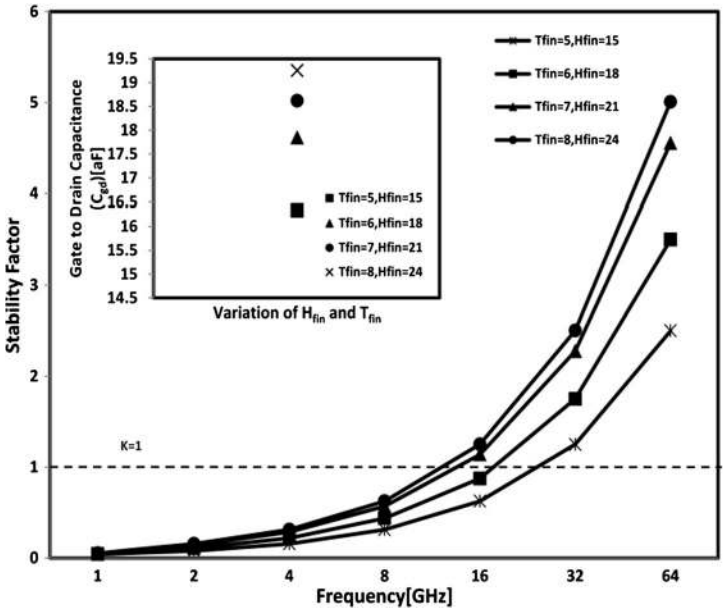


Fig. 8 Extracted stability factor and C_{gd} (*inset*) for different T_{fin} and H_{fin} with AR = 3



increase in Φ_m which leads to increase in f_k. Hence smaller Φ_m is preferred to operate FinFET under RF range

Figure 8 shows the extracted stability factor and C_{gd} (inset) for AR of 3 with three different H_{fin} and T_{fin} values. The aspect ratio (AR), which is given as ratio of H_{fin} to T_{fin} of 3 exhibits better RF Performance [9]. We have assumed three different H_{fin} and T_{fin} values with AR = 3 and result shows better stability performance at $T_{\mathrm{fin}} = 8$ nm and $H_{\mathrm{fin}} = 24$ nm. FinFET has advantage of varying silicon thickness in vertical plane i.e. freedom of varying H_{fin} than T_{fin} to improve device performance. It is observed that as H_{fin} increases, C_{gd} increases which lead to better stability performances. But, further increase in H_{fin} leads to increase in AR which changes device architecture from quasi triple gate to double gate. The FinFET reaches stability at $f_k = 14$ GHz for $T_{\mathrm{fin}} = 8$ nm and $H_{\mathrm{fin}} = 24$ nm.

The FinFET exhibits better stability performance at $H_{\mathrm{fin}} = 24$ nm, $T_{\mathrm{fin}} = 8$ nm, $\Phi_m = 4.5$ and $L_{\mathrm{spac}} = 10$ nm. Figure 9 shows the extracted stability factor for the optimized FinFET structure. It is evident that k reaches to 1 at 10 GHz which shows that the device can be operated unconditionally stable from 10 GHz onwards. It indicates that FinFET does not require additional circuit when operated from 10 GHz onwards for RF applications.

It is necessary to observe f_t and f_{max} to understand the capability of FinFET under RF range. The cut-off frequency

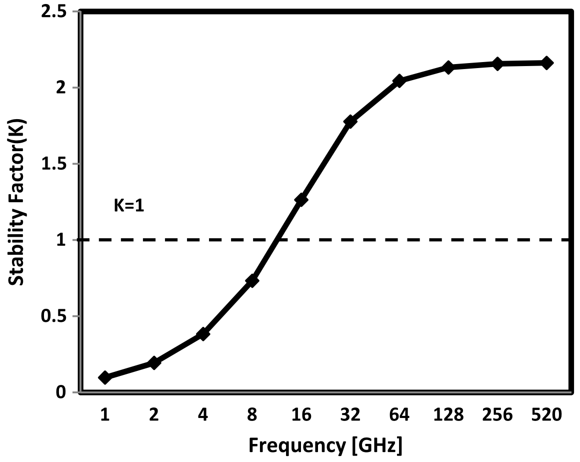


Fig. 9 Extracted stability factor for optimized FinFET at $V_{gs} = 1.5$ V and $V_{ds} = 0.1$ V

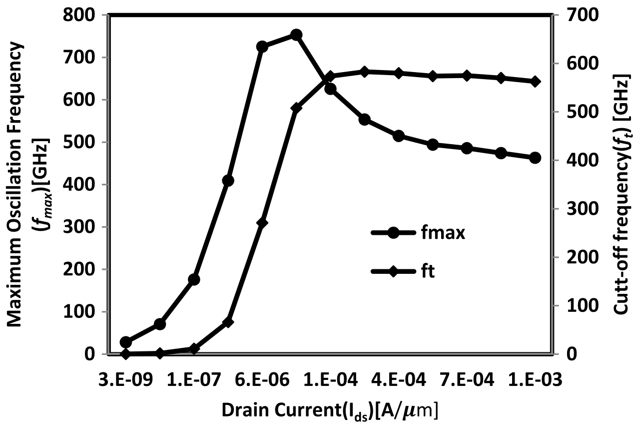


Fig. 10 f_t and $f_{\max}$ as function of drain current for optimized FinFET at $V_{gs} = 1.5$ V and $V_{ds} = 0.1$ V

f_t is evaluated as the frequency for which magnitude of short circuit gain drops to unity which can be expressed as $f_t = g_m/2\pi C_{gg}$. The f_{max} is related to the capability of the device to provide power gain at large frequencies, and is defined as the frequency at which the magnitude of the maximum available power gain drops to unity and can be given by $f_{max} = f_t/\sqrt{4(R_s + R_g + R_i)(g_{ds} + 2\pi f_t C_{gd})}$ where g_{ds} is drain to source conductance and R_g, R_s and R_i are gate, source and channel resistances respectively. The gate resistance is obtained from the extrinsic parasitic model which can be expressed as $\mathrm{Re}(Z_{12}) = \mathrm{Re}(Z_{21}) = R_g$.

Figure 10 shows the calculated f_t and f_{max} using the extracted intrinsic and extrinsic parameters as function of drain current for the optimized FinFET. The bias and geometry optimized structure has maximum f_t of 675 GHz due to the improved g_m and f_{max} of 780 GHz, which shows that the proposed FinFET structure is suitable for high frequency application and can be operated with better stability from 10 GHz onwards.

5 Conclusion

The RF stability performance of FinFET is studied at optimized bias and geometry conditions. The bias conditions such as gate and drain bias and geometrical parameters, such as gate spacer length, and silicon body aspect ratio along with gate material work function are analyzed using numerical simulation. We observed that C_{gd} is responsible for degradation in f_k. The proposed device geometry and optimized bias conditions show excellent RF stability performance. Hence there is no additional circuit required for the proposed FinFET as device is unconditionally stable from 10 GHz onwards when operating in RF range.

References

1. Wong, H.S.P.: Beyond the conventional transistor. IBM J. Res. Dev. **46**, 133–168 (2003)
2. Colinge, J.P.: Multiple-gate SOI MOSFETs. Solid-State Electron. **48**, 897–905 (2004)
3. Kedzierski, J., Ieong, M., Kanarsky, T., Zhang, Y., Wong, H.S.P.: Fabrication of metal gated FinFETs through complete gate silicidation with Ni. IEEE Trans. Electron Devices **51**, 2115–2120 (2004)
4. Tsormpatzoglou, A., Dimitriadis, C.A., Mouis, M., Ghibaudo, G., Collaert, N.: Experimental characterization of the subthreshold leakage current in triple-gate FinFETs. Solid-State Electron. **53**, 359–363 (2009)
5. Lederer, D., Kilchytska, V., Rudenko, T., Collaert, N., Flandre, D., Dixit, A., et al.: FinFET analogue characterization from DC to 110 GHz. Solid-State Electron. **49**, 1488–1496 (2005)
6. Kilchytska, V., Collaert, N., Rooyackers, R., Lederer, D., Raskin, J.P., Flandre, D.: Perspective of FinFETs for analog applications. In: Proc. European Solid-State Device Research Conference, pp. 65–68 (2004)
7. Guillorn, M., Chang, J., et al.: FinFET performance advantage at 22 nm: an AC perspective. In: Proc. Symposium on VLSI Technology Digest, pp. 12–13 (2008)
8. Wu, W., Chan, M.: Analysis of geometry-dependent parasitics in multifin double-gate FinFETs. IEEE Trans. Electron Devices **54**, 692–698 (2007)
9. Kranti, A., Raskin, J.-P., Armstrong, A.G.: Optimizing FinFET geometry and parasitics for RF applications. In: Proc. IEEE International SOI Conference, pp. 123–124 (2008)
10. Tinoco, J.C., Alvarado, J., Martinez-Lopez, A.G., Raskin, J.P.: Impact of extrinsic capacitances on FinFETs RF performance. IEEE Trans. Microw. Theory Tech. **61**, 833–840 (2013)
11. Sivasankaran, K., Kannadassan, D., Seetaram, K., Mallick, P.S.: Bias and geometry optimization of silicon nanowire transistor: radio frequency stability perspective. Microw. Opt. Technol. Lett. **54**, 2114–2117 (2012)
12. Sivasankaran, K., Mallick, P.S.: Stability performance of optimized symmetric DG-MOSFET. J. Semicond. **34**, ??–?? (2013) (accepted)
13. International Technology Roadmaps for Semiconductor (ITRS) (2010)
14. Dastjerdy, E., Ghayour, R., Sarvari, H.: 3D quantum mechanical simulation of square nanowire MOSFETs by using NEGF method. Cent. Eur. J. Phys. **9**, 472–481 (2011)
15. Device simulator ATLAS User Manual, Silvaco Int., Santa Clara, CA, 2012 [Online]. Available: http://silvaco.com

16. Schwierz, F., Liou, J.J.: Semiconductor devices for RF applications: evolution and current status. Microelectron. Reliab. **41**, 145–168 (2001)
17. Gonzales, G.: Microwave Transistor Amplifiers—Analysis and Design, 2nd edn. Prentice-Hall, New York (1997)
18. Rollet, J.M.: Stability and power gain invariants of linear two ports. IRE Trans. Circuit Theory **9**, 29–32 (1962)
19. Kang, I.M., Shin, H.: Non-quasi-static small-signal modeling and analytical parameter extraction of SOI FinFETs. IEEE Trans. Nanotechnol. **5**, 205–210 (2006)
20. Sarkar, A., Das, K.A., De, S., Sarkar, K.C.: Effect of gate engineering in double-gate MOSFETs for analog/RF applications. Microelectron. J. **43**, 873–882 (2012)
21. Enz, C.C., Vittoz, E.A.: Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design. Wiley, New York (2006)
22. Tawfik, S.A., Kursun, V.: Work-function engineering for reduced power and higher integration density: an alternative to sizing for stability in FinFET memory circuits. In: Proc. IEEE International Symposium on Circuit and Systems, pp. 788–791 (2008)