**TABLE 3 The Frequency Ranges Where *Re* is Larger than 377 Ω**

| | |
|---|---|
| $R_2 < 377\ \Omega$ | No solutions |
| $R_2 > 377\ \Omega$<br>$R_2 + R_3 < 377\ \Omega$ | $f > \frac{1}{2\cdot\pi\cdot C_n\cdot R_3}\cdot\sqrt{\frac{(R_2+R_3)\cdot[377-(R_2+R_3)]}{R_2\cdot(R_2-377)}}$ |
| $R_2 > 377\ \Omega$<br>$R_2 + R_3 < 377\ \Omega$ | The entire frequency band |

As $R_2$ and $R_2 + R_3$ are required to be positive for stability considerations, $R_e$ is always positive. In Table 3, the frequency ranges where $R_e$ is larger than 377 Ω are presented.

From Eqs. (8), (9) and Table 3, a tradeoff among $C_{ne}$, $f_t$, and $R_e$ can be observed. $R_2$ needs to be high enough to increase $R_e$ and $f_t$, and the absolute value of $R_3$ needs to be reduced to increase the $f_t$ and $f_{tmax}$. As a result the value of $C_{ne}$ is dropped dramatically which offsets bandwidth enhancement.

## 3. CONCLUSION

In this article, AMC and AMC absorber structures loading with negative elements realized by a floating NIC circuit are analyzed. Only for the idealized NIC case can arbitrary ultra-wide bandwidth be achieved. Under more realistic NIC circumstances it is shown that if both a negative inductance and a negative capacitance are required simultaneously then stability is unlikely to be realized. Whereas if only a negative capacitance is required stability within an NIC operation frequency band can in principle be obtained. The work presented here suggests that the use of floating NICs to form non-Foster AMC bandwidth enhancement is likely to be problematical unless practical circuits can be made to behave more like their idealized counterparts.


## ACKNOWLEDGMENT

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# BIAS AND GEOMETRY OPTIMIZATION OF SILICON NANOWIRE TRANSISTOR: RADIO FREQUENCY STABILITY PERSPECTIVE


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**ABSTRACT:** *This article presents structure and bias optimization techniques for the radio frequency (RF) stability of silicon nanowire transistor. The RF parameters are extracted using device simulation. The device stability is obtained for various bias conditions and geometry, and observed that the proposed device structure shows good stability response.* © 2012 Wiley Periodicals, Inc. Microwave Opt Technol Lett 54:2114–2117, 2012; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.27016



**Key words:** *silicon nanowire transistors; radio frequency; stability factor; device simulation*


## 1. INTRODUCTION

Gate-all-around structure becomes one of the promising solutions for the short channel device, with improved transport property, and better compatibility with CMOS technologies. Many investigations are reported on the compact modeling, DC characteristics, and fabrication process issues of silicon nanowire transistor (SNWT) [1–3], but the radio frequency (RF) studies and small signal modeling have not received much attention.

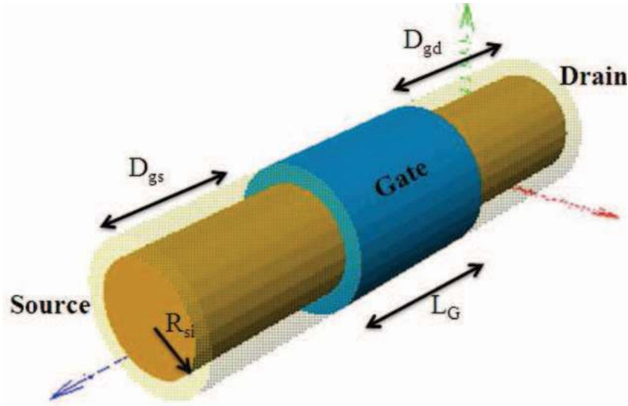


**Figure 1** Structure of silicon nanowire FET. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

In the design of RF amplifiers or oscillators, the selection of transistor depends on its power gain, DC bias, noise, impedance matching, and stability. Many works were carried out to improve RF properties of MOS devices, such as double-gate MOSFETs, FinFETs, and SNWT, the RF parasitic optimization has been done to improve the maximum stable gain, maximum power gain, maximum oscillation frequency ($f_{max}$), cutoff frequency ($f_T$), and reduced noise figure [4–7]. However, none of these literatures has studied RF stability which is one of the important selection components for the design of RF amplifiers.

There are two possible cases for stability, namely, unconditionally stable and potentially stable [8]. An unconditionally stable device is generally preferred for the RF amplifier design as its stability is independent of port impedances. However, the potentially stable devices can also be used in amplifiers with additional stabilization network, which degrades the performance and increase the noise level.

In this article, the RF stability on 60 nm channel length SNWT has been studied using TCAD simulation for various bias conditions and geometries. Relation between stability factor and parasitic elements is derived using intrinsic small signal model and RF parameters are extracted using device simulation. It is observed that the field coupling between drain and gate is responsible for the instability of transistor. Finally, the geometry and bias optimization are carried out with the limiting factors, power gain, and $f_T$. The optimized device shows good stability performance from 2 GHz onward. The optimized SNWTs can be a promising structure for the future mm-wave radio-wave integrated circuits (RFIC) and microwave monolithic integrated circuits (MMIC) designs with reduced circuit complexity and noise level.

## 2. DEVICE STRUCTURE

Figure 1 shows structure of a cylindrical SNWT. The radius of silicon region ($R_{si}$) is varied from 3–5 nm with oxide thickness of 1 nm and the gate length of 60 nm. The source and drain (S/D) are doped uniformly at $2 \times 10^{20}$ cm$^{-3}$ with the uniform channel doping of $1 \times 10^{15}$ cm$^{-3}$. The distance between gate and source ($D_{gs}$), between gate and drain ($D_{gd}$) is 20 nm. Density gradient (potential correction) quantum corrected three dimensional drift diffusion model was calibrated and adopted to simulate the confinement of SNWTs using Atlas Silvaco TCAD device simulation [9].The AC solution is performed to extract RF Parameters which is used to calculate $f_T$ and $f_{max}$.

## 3. MODELING

### 3.1 Stability Factor

The stability factor describes the instable oscillations due to input or output impedance of the transistor which has negative real part, the negative resistance yield $G_{in}$ 1 and $G_{out}1 > 1$ [10]. Therefore, the instability also depends on the input and output matching properties of the circuit. The transistor will be unconditionally stable if it has $G_{in} < 1$ and $G_{out}1 < 1$ at a particular frequency. On the other hand, the conditional stability determines the stable operation at a range of impedance values on source or load matching. The conditions for unconditionally stable transistors are

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \quad (1)$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \quad (2)$$

Here, $G_S$ and $G_L$ are reflection coefficients at the source and load, respectively. A stability factor $K$ was proposed with an auxiliary factor $\Delta$ to ensure these conditions

$$K = \left( \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \right) > 1 \quad (3)$$

where,

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (4)$$

Here, $S_{ij}$ (for i, j =1, 2) are scattering parameters of transistor.

### 3.2. Stability Model

A stability model can help to optimize the device geometry for RF and microwave active circuits. The stability model is developed based on the conditions mentioned in Eqs. (3) and (4). The stability factor in terms of $Y$ parameters is,

$$K = \frac{\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12}Y_{21})}{|Y_{12}.Y_{21}|} \quad (5)$$

The $Y$ parameters are considered with intrinsic small signal parameters of SNWTs as [11],

$$\begin{aligned} Y_{11} &\cong \omega^2\left(R_{gs}C_{gs}^2 + R_{gd}C_{gd}^2\right) + j\omega\left(C_{gs} + C_{gd}\right) \\ Y_{12} &\cong -\left(\omega^2 R_{gd}C_{gd}^2 + j\omega C_{gd}\right) \\ Y_{21} &\cong g_m - \omega^2 R_{gd}C_{gd}^2 - j\omega C_{gd} + (\tau.g_m) \\ Y_{22} &\cong g_{ds} + \omega^2 R_{gd}C_{gd}^2 + j\omega C_{gd} \end{aligned}$$

These $Y$ parameters can be used in Eq. (5) to simplify further as

$$K \cong \frac{\omega\left(R_{gs}g_{ds}C_{gg}^2 + 2R_{gd}g_m C_{gg}C_{gd} + C_{gg}^2\right)}{C_{gd}\sqrt{2\omega^2 g_m C_{gg}^2 + g_m^2}} \quad (6)$$

where,

$$C_{gg} = C_{gs} + C_{gd}$$

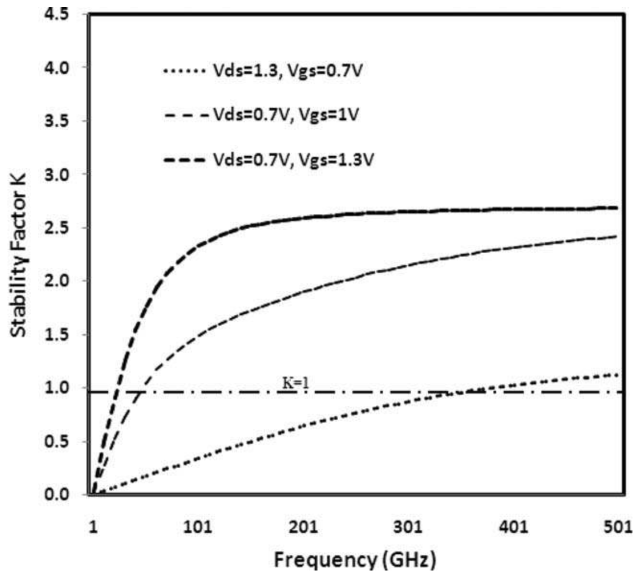


**Figure 2** Extracted stability factor at different bias conditions

The Eq. (6) is extended to obtain $f_k$ by putting $K = 1$,

$$f_k \cong \frac{g_{\rm m}.N}{2\pi C_{\rm gg}\sqrt{g_{\rm ds}g_{\rm m}R_{\rm gs}M^2 + NM(g_{\rm m}R_{\rm gd}+1)}} \tag{7}$$

where

$$M = {C_{\rm gs}}/{C_{\rm gg'}} \quad \text{and} \quad N = {C_{\rm gd}}/{C_{\rm gg}}$$

which can be related to $f_{\rm T}$ as,

$$f_k \cong \frac{f_{\rm T}.N}{\sqrt{g_{\rm ds}g_{\rm m}R_{\rm gs}M^2 + NM(g_{\rm m}R_{\rm gd}+1)}} \tag{8}$$

where,

$$f_{\rm T} \cong {g_{\rm m}}/{2\pi C_{\rm gg}}$$

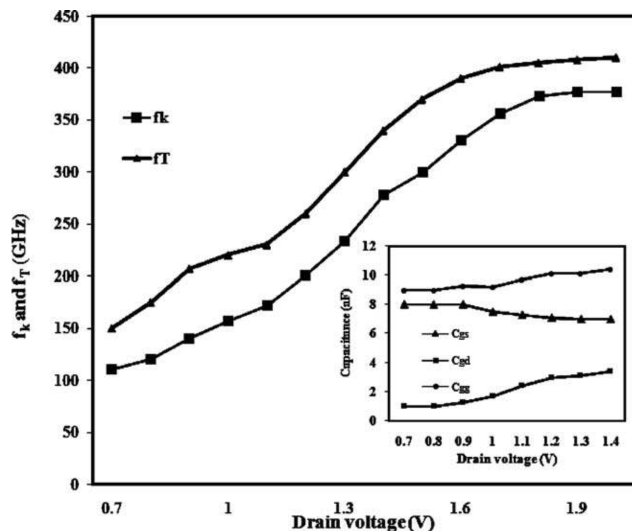


**Figure 3** Variation of $f_k$ and $f_{\rm T}$ for the sweep of $V_{\rm ds}$ and extracted capacitances for the sweep of $V_{\rm ds}$ and $V_{\rm gs}$= 0.7 V(inset)

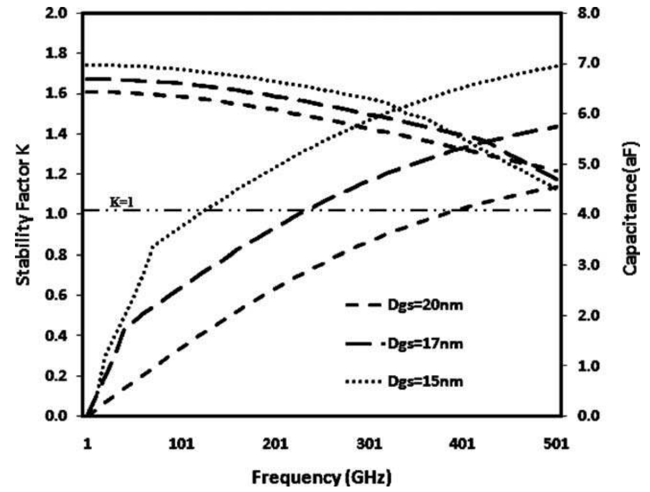


**Figure 4** Extracted stability factor and $C_{\rm gs}$ for different $D_{\rm gs}$ at $V_{\rm gs}$=0.7 V and $V_{\rm ds}$=1.3 V

This stability model describes the relation between $f_k$, intrinsic small signal parameters and $f_T$ which also gives hints for optimization. It is clear from Eq. (8) that $M$ and $N$ values can be adjusted to reduce $f_k$ as $f_{\rm T}$ should not be degraded. But $N$ is almost independent parameter on stability model with respect to $f_{\rm T}$. So the optimization begins with the study of factors related to $M$ and $N$, especially $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm gg}$.

#### 4. BIAS AND GEOMETRY OPTIMIZATION

The stability factor is calculated from extracted $S$ parameters for various applied voltage and is shown in Figure 2, which exhibits $f_k$ = 370 GHz for $V_{\rm GS}$ = 0.7 and $V_{\rm DS}$ = 1.3 V. We have obtained, $f_k$ = 21 GHz and 45 GHz for $V_{\rm GS}$ = 1 V and 1.3 V, respectively at $V_{\rm DS}$ =0.7 V. This shows the improved stability performance at higher $V_{\rm GS}$, as $C_{\rm gd}$ dominates $C_{\rm gs}$ which leads to higher $f_k$ and is shown in Figure 3.

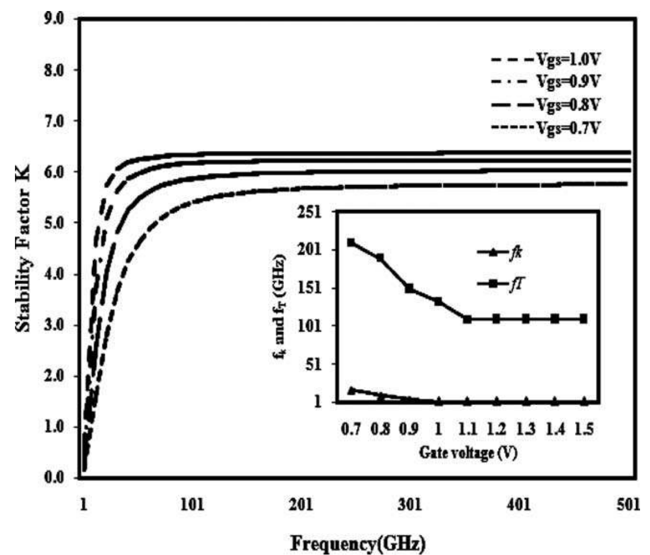


**Figure 5** Extracted stability factor for the optimized structure at different gate bias voltages and extracted $f_{\rm T}$ and $f_k$ for sweep of $V_{\rm gs}$ and $V_{\rm ds}$ = 1 V(inset)

The position of the gate plays an important role to get higher $C_{gs}$ and lower $C_{gd}$. The stability factor and $C_{gs}$ are extracted for various $D_{gs}$, and shown in Figure 4. It is found that the stability has been improved as gate moves toward source. The distance cannot be further reduced because of limitations during fabrication. The optimal geometry of the device has $D_{gs}$ of 15 nm, $t_{ox}$ of 1 nm, and $R_{si}$ of 3 nm.

Figure 5 shows the extracted stability factor for various biases of $V_{GS}$. It is observed that the stability response is improved and $f_k = 29$ GHz at $V_{GS} = 1$ V. The $f_k$ is extracted along $f_T$ at higher $V_{GS}$ and is shown in inset of Figure 5. When $V_{GS} > 1$ V, the values of $f_k$ and $f_T$ are saturated, this indicates that the effect of capacitor at higher $V_{GS}$ is negligible. For the optimal geometry and biasing conditions, the device shows unconditionally stable performance from 2 GHz onwards with $f_T = 100$ GHz.

## 5. CONCLUSION

The RF characteristics of 60 nm SNWT are performed through TCAD simulation. The device stability is studied for various bias and geometry conditions, and observed that feedback capacitance $C_{gd}$ from drain to gate is responsible for degradation in $f_k$ and $f_T$. The proposed optimized geometry and bias condition show excellent stability performance with optimal gain and $f_T$. There is no need of any additional stabilization network as the device is unconditionally stable from 2 GHz. The device has shown improved RF performance, reduced noise, and circuit complexity.

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# INTEGRATION OF MINIATURIZED BALUN AND LOW-NOISE AMPLIFIER FOR SINGLE-IN DIFFERENTIAL-OUT APPLICATIONS

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**ABSTRACT:** *A low-noise module comprises a low-noise amplifier and a new type of passive balun, which consists of two λ/8 broadside-coupled lines and a short redundant line, is presented. The on-chip balun is not only low lossy and compact size but also provides good amplitude and phase balances at output ports over a quite wide frequency range. The method of designing the new-type balun fabricated with CMOS IC technology is proposed. An experimental prototype operated at K-band was designed and fabricated with a commercial 0.18-μm CMOS technology to verify the effectiveness of the proposed design method. The measured results show the single-to-differential gain is about 9 dB, the amplitude imbalance of the output ports is less than 1.0 dB associated with the phase difference of 181 ± 3° over the frequency range of 20–40 GHz. The area of the prototype including the RF probe pads is about 0.73 × 1.28 mm$^2$.* © 2012 Wiley Periodicals, Inc. Microwave Opt Technol Lett 54:2117–2121, 2012; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.26987

**Key words:** *miniature balun; distributed balun; low-noise amplifier; MMIC; CMOS*

## 1. INTRODUCTION

The continuing demands for high data rate and compact wireless communication systems have attracted a great attention to construct wireless modules using popular CMOS technologies due to its capabilities of fast evolution, high-level, and mixed-mode integrations. To avoid latch-up problem, however, the resistivity of silicon substrate has to be kept in low (∼ 10 S/m), which also results the common mode noise conducted through the substrate to significantly affect the performances of CMOS RF circuits. To eliminate such a drawback, differential inputs are usually adopted by the CMOS transceiver and a circuit namely balun is commonly required to transfer the signal received from antenna into the differential signals for entering the CMOS receiver. Recently, some amplifying circuits for K-band single-in differential-out applications have been developed [1–4]. First type of these active baluns is constructed by connecting two different topologies of amplifiers that have inverse phases of output ports relative to the common input port. Although such a balun circuit is compact in size, however, it shows poor characteristics in power gain and noise figure at high frequency band. Second kind of the baluns is implemented by connecting a passive transformer to the output of a low-noise amplifier (LNA) so as to transfer the single-end signal into differential type. The experimental results of such an active balun have demonstrated that the size of the balun is not only compact, because of adopting passive lumped components, but also provides high flexibility in achieving desired noise figure and power gain. However, the lumped-element transformers still suffer from their low $Q$ factor caused by metal conductors and low-resistivity silicon substrate and usually exhibit the higher insertion losses than the distributed-type components. It is well understood that the conventional distributed balun, such as Marchand balun, usually