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Coupled inductor-based DC–DC converter with high voltage conversion ratio and smooth input current

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Abstract: In this study, a coupled inductor (CI)-based high step-up DC–DC converter is presented. The proposed topology is developed from a primitive quadratic boost converter (QBC) structure. A two-phase interleaved QBC structure is obtained by employing multi-winding CIs instead of discrete inductors as the energy storage magnetic element. The voltage gain is further extended by using (i) voltage lift capacitor, (ii) CIs and (iii) voltage multiplier cells. Consequently, the voltage stress on the main switches is reduced to 18.9% of the output voltage. Moreover, interleaving mechanism helps in achieving a smooth input current profile; the input current ripple is only 4.59% of the total input current magnitude. To validate the proposed concept, 18 V/380 V, 150 W prototype converter is constructed and experimented. Under experimentation, the converter delivers the required power to the load at 95% full-load efficiency. Further, under closed-loop condition, the output voltage from the converter is regulated to the required standard value of 380 V DC.

1 Introduction

Renewable energy sources (RES) like photovoltaic (PV), wind, fuel cell, etc. have proved to be a viable alternative to fossil fuel-based electrical energy conversion. RES easily overcome the twin challenges of meeting the ever-increasing electrical energy demand and stringent environmental concerns [1].

Generally, PV panels yield very low output voltage which is insufficient to meet the load requirements. For connecting the input PV source to the regular loads and/or common DC bus, a high gain DC–DC converter is the most preferred and widely adopted power converter interface solution [2].

The voltage conversion ratio of a conventional boost converter (CBC) is enhanced by adopting one or more of the techniques (like coupled inductor (CI), voltage multiplier cells (VMCs), switched capacitor, etc.) outlined in [3, 4]. The converters presented in [5–7] employ gain extension cells based on diodes and capacitors. However, the achievable voltage gain value, voltage stress on the switch and power conversion efficiency are strongly dependent on the number of gain extension cells that are employed.

The basic flyback converter structure is modified and presented in [8, 9]. However, the novel changes yielded only lower voltage conversion values of <10. In CI-based non-isolated power converters, the voltage gain is easily enhanced by adjusting the turns ratio without affecting the switch stress [10–14]. Some gain extension mechanisms are also combined with CIs to achieve voltage conversion ratios >10 [15–18].

The quadratic boost converter (QBC) presented in [19] operates with wide DC conversion ratios ranging from 3.42 to 6.85. In [20], a cascaded synchronous boost converter is presented. The converter offers a good voltage gain of about 8.33 and soft-switching is employed to reduce the switching losses.

The voltage gain obtainable from QBC is enhanced by incorporating suitable gain extension mechanisms within the QBC structure [21–24]. In [21], a VMC is incorporated to achieve a voltage gain of about 10 and reduce the switch stress. In [22], a CI-based QBC with voltage doubler is employed. The voltage stress magnitude of the CI-based QBC presented in [23] is reduced by using a snubber circuit. The converter discussed in [24] is obtained by judiciously stacking the voltage gain cells and integrating them with the QBC structure.

Some single switch QBC-based high gain converters are presented in [25–28]. The voltage conversion ratio values are increased by using CI–multiplier cell combination [25, 26], dual CIs [27] and stacked switching cells [28]. The maximum voltage conversion ratio is about 16.66 for the converter presented in [26]. Moreover, the input current contains ripple in all the QBC-based converters that are reported in literature.

Generally, a smooth input current is mostly preferred for PV application so as to easily implement maximum power point tracking algorithms. An interleaved mechanism is widely employed to reduce the input current ripple [16]. The converter reported in [29] eliminates the input current ripple by operating the switches at selected duty ratio values. By adjusting the inductance value and switching frequency, the input current ripple for the converter presented in [30] is controlled. In [31, 32], a third winding is added in series with the capacitor at the input side to cancel the input current ripple.

This paper proposes a CI-based high gain interleaved QBC (CI-IQBC) which employs two multi-winding CIs, voltage lift technique and VMCs to achieve a practical voltage gain of 21.11. The paper is described through the following sections: Section 1 presents the evolution of the proposed converter while Section 2 details the circuit synthesis. In Section 3, the principle of operation and switching profile of the proposed CI-IQBC are discussed. The power circuit analysis under steady-state condition and design equations of the proposed CI-IQBC are derived in Section 4. Experimental results obtained from a prototype converter are elaborated in Section 5; detailed results are presented for open and closed-loop conditions. In Section 6, the benefits of the proposed CI-IQBC are brought out by comparing it with few state-of-art converters while the concluding remarks are presented in Section 7.

2 Evolution and description of the power circuit

Fig. 1*a* shows the circuit arrangement of basic QBC. Since the switch is located very close to the output terminals, its voltage stress is extremely high, especially, in high-gain applications. Considering the additional loss due to increased switch stress, the voltage conversion ratio is practically limited. Fig. 1*b* shows an improved variant of the basic QBC. By interleaving two QBC structures and cascading them through a lift capacitor (C_{Lift}), the voltage gain of the developed structure is doubled as compared to QBC. Moreover, replacing the discrete energy storage inductors by CIs facilitates in achieving a compact and light magnetic element.

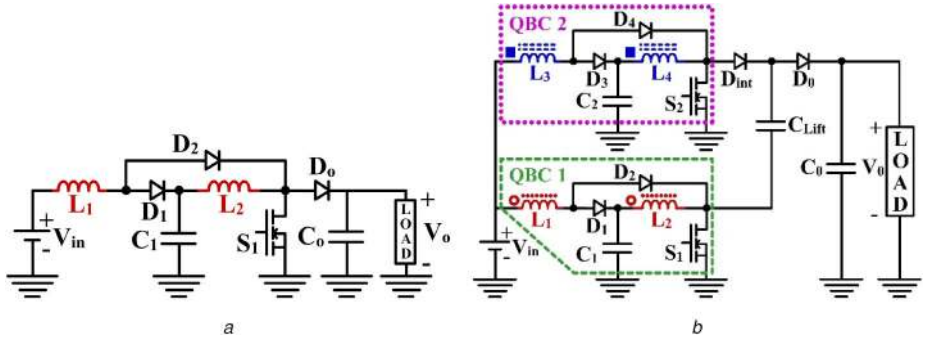


Fig. 1 *Circuit diagrams demonstrating the development of the proposed CI-IQBC*
(a) Circuit showing the basic QBC presented in [19],
(b) Improved variant of QBC consisting of two-phase interleaved QBC and voltage lift capacitor, referred to as IQBC henceforth

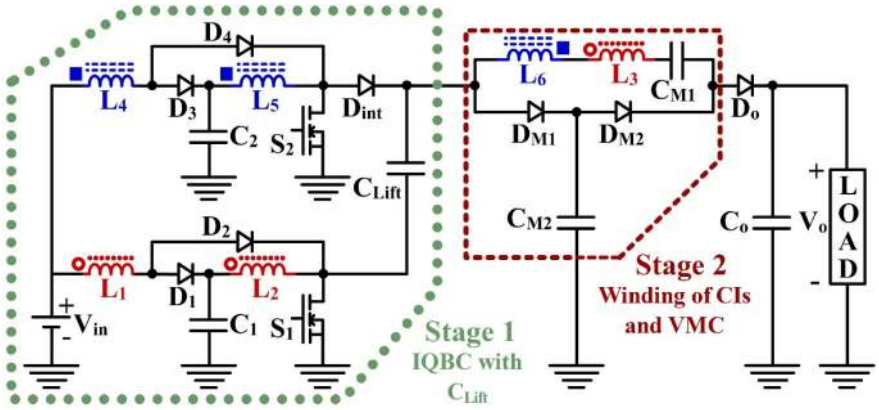


Fig. 2 *Power circuit of the proposed CI-IQBC*

For the interleaved QBC (IQBC) developed and shown in Fig. 1*b*, as the voltage gain is enhanced by introducing C_{Lift}, the switch voltage stress level is only half of the output voltage.

The circuit diagram of the proposed high-gain CI-IQBC is presented in Fig. 2. The proposed CI-IQBC is derived from the two-phase IQBC and visualised using two stages for easier understanding. Stage 1 is formed by incorporating multi-winding CIs in the IQBC structure. The voltage gain of the structure is already enhanced using voltage lift capacitor C_{Lift}. Stage 2 of the proposed converter comprises of the tertiary windings (L_3 and L_6) along with VMC network (D_{M1}, D_{M2}, C_{M1} and C_{M2}). The output obtained from stage 1 is cascaded with stage 2 to further enhance the net obtainable voltage gain. Diode D_0 is the usual output diode rectifier while capacitor C_0 serves as the output filter capacitor. The detailed operating principle is discussed subsequently.

3 Principle of operation of the proposed CI-IQBC

The operating principle is explained using two modes that occur during one complete switching cycle. Since the switches S_1 and S_2 are located in the interleaved phases, they are switched with 180° phase shift. Further, as the switches are operated at a duty ratio of $D = 0.5$, the complete operating principle is explained using two modes through the below-mentioned valid assumptions.

(i) All the circuit elements are ideal.
(ii) The converter is designed to operate in continuous conduction mode (CCM).
(iii) The energy storage inductors are precharged before the switches are gated ON.

Mode 1, (t_0–t_1): Mode 1 commences at t_0 when switch S_1 is turned ON and switch S_2 is turned OFF. As S_1 is ON, L_1 linearly charges towards V_{in} through S_1 and diode D_2. Consequently, energy stored in L_1 increases. As D_2 and S_1 conduct, the potential across C_1 reverse biases D_1. Further, C_1 transfers its stored energy to L_2 through S_1; induced voltage across L_2 builds up towards V_{C_1}. In the other interleaved phase, as S_2 is OFF, stored energy in L_5 forward biases D_{int} and aids in transferring its stored energy to C_{Lift}. During the energy transfer process, D_4 is reverse biased. Further, stored energy in L_4 forward biases D_3 and charges C_2.

In stage 2, based on the state of L_1–L_2, L_4–L_5 pairs of inductors, L_3 and L_6 discharge and charge, respectively. The voltage developed across C_{M2} reverse biases D_{M1} and forward biases D_{M2} while charging C_{M1} through L_3, L_6, C_{Lift} and S_1. Hence, the output diode D_0 is reverse biased and the load demand is met by the output capacitor C_0. Mode 1 ends at time $t = t_1$ when the inductors L_1 and L_2 are charged to their respective maximum values while L_4 and L_5 are discharged and current through them reach their respective minimum values. Simultaneously, in stage 2, C_{M1} is fully charged and current through L_3 reaches its maximum value.

The equations governing mode 1 are given by

$$i_{L_1}(t) = I_{L_{1,\min}} + \frac{1}{L_1} v_{L_1} t \text{ and } i_{L_2}(t) = I_{L_{2,\min}} + \frac{1}{L_2} v_{L_2} t \tag{1}$$

$$i_{L_4}(t) = I_{L_{4,\max}} - \frac{(V_{\text{in}} - v_{C_2})}{L_4} t \text{ and } i_{L_5}(t) = I_{L_{5,\max}} - \frac{(v_{C_2} - v_{C_{\text{Lift}}})}{L_5} t \tag{2}$$

Mode 2, (t_1–t_2): Mode 2 begins at time $t = t_1$ when S_1 is turned OFF and S_2 is turned ON. The inductors L_4 and L_5 start charging, the voltage across them builds up towards V_{in} and V_{C_2}, respectively. As C_2 charges L_5 through S_2, diode D_3 is reverse biased and D_4 is forward biased. As S_2 is ON, D_{int} is reverse biased. Since S_1 is OFF, the energy stored in L_1 charges C_1 through D_1 while reverse biasing D_2. Further, energy stored in CI_1 (L_1, L_2 and L_3), C_{Lift}, L_6 and C_{M1} charges C_0 through D_0 and takes care of the load demand. In the VMC network, due to the energy transfer process, diode D_{M1}

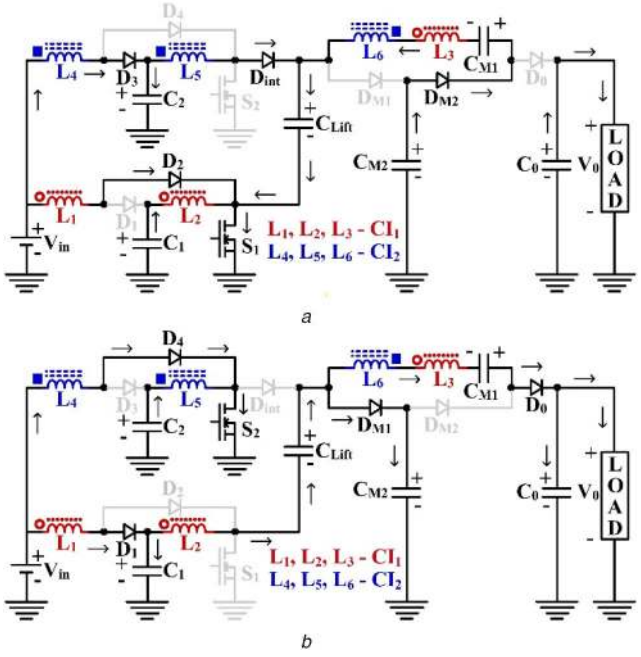


Fig. 3 *Equivalent circuit when the CI-IQBC operates in*
(a) Mode 1,
(b) Mode 2

is forward biased and charges C_{M2} while D_{M2} is reverse biased. Mode 2 ends at time $t = t_2$ when C_{M2} is completely charged and D_{M1} turns OFF. In stage 1, current through L_4 and L_5 reach their respective maximum values while current through L_1 and L_2 reach their minimum values. Turning ON of S_1 marks the beginning of next switching cycle. The equations governing Mode 2 are given by

$$i_{L_3}(t) = I_{L_{3,\min}} + \frac{v_{L_3}}{L_3}t = I_{L_{3,\min}} + \frac{(v_{C_{\text{Lift}}} + v_{C_{M1}} - v_{C_{M2}} - v_{L_6})}{L_3}t \quad (3)$$

$$i_{L_6}(t) = I_{L_{6,\max}} - \frac{v_{L_6}}{L_6}t = I_{L_{6,\max}} - \frac{(v_{C_{\text{Lift}}} + v_{C_{M1}} - v_{C_{M2}} - v_{L_3})}{L_6}t \quad (4)$$

$$v_{C_x}(t) = V_{C_x} + \frac{i_{c_x}(t)}{C_x}t \quad \text{where } x = 1, 2, \text{Lift} \quad (5)$$

$$i_{L_1}(t) = I_{L_{1,\max}} - \frac{1}{L_1}v_{L_1}t \text{ and } i_{L_2}(t) = I_{L_{2,\max}} - \frac{1}{L_2}v_{L_2}t \quad (6)$$

$$i_{L_4}(t) = I_{L_{4,\min}} + \frac{(V_{\text{in}} - v_{C_2})}{L_4}t \text{ and } i_{L_5}(t) = I_{L_{5,\min}} + \frac{(v_{C_2} - v_{C_{\text{Lift}}})}{L_5}t \quad (7)$$

Figs. 3*a* and *b* depict the equivalent circuit during the operating modes. Fig. 4 presents the switching profile of the key circuit parameters for one complete operating cycle.

4 Analysis under steady-state and design details

4.1 Voltage conversion ratio

The overall voltage conversion ratio of the proposed CI-IQBC is obtained by applying volt-second balance. Alternatively, the overall voltage gain is also obtained by intuitively determining the voltage gain contributed by stages 1 and 2. The voltage gain contributed by individual QBC structures employed in stage 1 is derived in [19] and given by

$$M_{\text{QBC}} = \frac{1}{(1-D)^2} \quad (8)$$

where D is the duty ratio of the switch.

In stage 1, since C_{Lift} is employed, the voltage gain of stage 1 is given by

$$M_{\text{Stage 1}} = \frac{V_{\text{Stage 1}}}{V_{\text{in}}} = \frac{2}{(1-D)^2} \quad (9)$$

In stage 2, input to the VMC network is obtained from the energy storage inductors located in QBC structures. The VMC is embedded across the windings of the CIs. Further, the windings are additively coupled. Consequently, the voltage gain obtainable from stage 2 is deduced as

$$M_{\text{Stage 2}} = \frac{V_{\text{Stage 2}}}{V_{\text{in}}} = \frac{2nk}{(1-D)^2} \quad (10)$$

where k is the coefficient of coupling between the CI windings and n is the turns ratio of CIs.

Therefore, the overall voltage gain (M) is determined by summing up (9) and (10). The voltage gain is expressed as

$$M = \frac{V_0}{V_{in}} = M_{\text{Stage 1}} + M_{\text{Stage 2}} = \frac{2 + 2nk}{(1-D)^2} \quad (11)$$

4.2 Voltage rating of the switches

The switches in the proposed CI-IQBC are located in the two interleaved QBC stages. Hence, they are subjected to a voltage stress magnitude which is equal to that of a QBC. Therefore, the voltage rating of S_1 and S_2 is determined by

$$V_{S_1} = V_{S_2} = \frac{1}{(1-D)^2}V_{\text{in}} \quad (12)$$

In terms of output voltage, the switch stress is expressed as

$$V_{S_1} = V_{S_2} = \frac{V_0}{2 + 2nk} \quad (13)$$

4.3 Voltage rating of diodes

To obtain the voltage stress on the diodes, the reverse voltage impressed across them is determined. In stage 1, D_1 and D_4 are reverse biased during mode 1. The voltage stress of D_1 is same as the voltage developed across C_1; cathode of D_1 is clamped at V_{C_1} while the anode terminal is grounded through D_2–S_1. Therefore, voltage rating of D_1 is given by

$$V_{D_1} = \frac{1}{1-D}V_{\text{in}} = \frac{(1-D)}{2 + 2nk}V_0 \quad (14)$$

The cathode terminal of D_4 is clamped at a potential developed between the positive plate of C_{Lift} and ground while the anode terminal is clamped at V_{C_2} (through D_3). Hence, the voltage stress on D_4 is given by

$$V_{D_4} = \frac{D}{(1-D)^2}V_{\text{in}} = \frac{D}{2 + 2nk}V_0 \quad (15)$$

Due to structural symmetry, the voltage rating of D_2 and D_3 is similar to (14) and (15), respectively.

Diode D_{int} is the intermediate element between stages 1 and 2; its cathode terminal is clamped to a voltage level obtained in stage 1 while the anode terminal is grounded. Therefore, voltage stress on D_{int} is derived as

$$V_{D_{\text{int}}} = \frac{2}{(1-D)^2}V_{\text{in}} = \frac{2}{2 + 2nk}V_0 \quad (16)$$

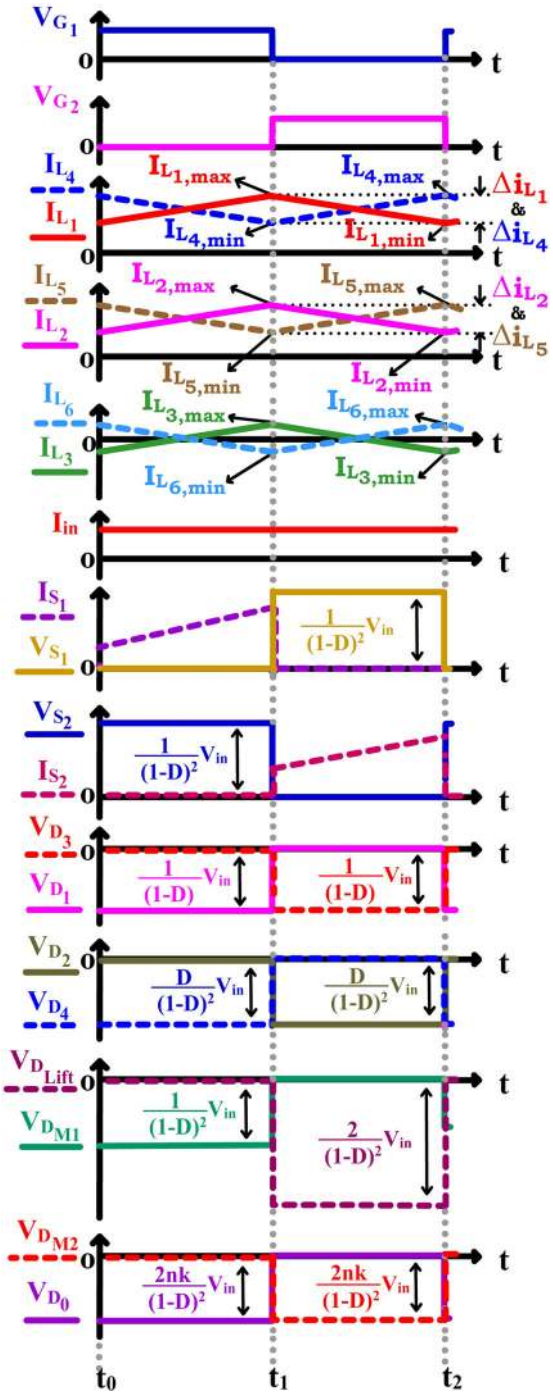


Fig. 4 *Switching profile of the key circuit parameters for one complete switching cycle*

In stage 2, multiplier capacitor C_{M2} charges to a voltage level which is obtained in stage 1. Cathode of D_{M1} is held at $V_{C_{M1}}$ while the anode is held at $V_{C_{Lift}}$. Thus,

$$V_{D_{M1}} = \frac{1}{(1-D)^2}V_{in} = \frac{1}{2+2nk}V_0 \tag{17}$$

The voltage rating of D_{M2} and D_0 is given by

$$V_{D_{M2}} = V_{D_0} = \frac{2nk}{(1-D)^2}V_{in} = \frac{nk}{1+nk}V_0 \tag{18}$$

4.4 Current rating of switches and diodes

The proposed converter is developed from an interleaved QBC structure. When S_1 is in ON state, the inductors L_1 and L_2 charge through S_1. Hence, the current stress on the switch is given by

$$I_{S_1} = I_{L_1} + I_{L_2} = \frac{I_{in}}{2} + \frac{I_{in}(1-D)}{2} \tag{19}$$

Similarly, the current stress on S_2 is expressed as

$$I_{S_2} = I_{L_4} + I_{L_5} = \frac{I_{in}}{2} + \frac{I_{in}(1-D)}{2} \tag{20}$$

The current stress on diodes D_1–D_4 is the same as the current through the respective interleaved phases. Hence,

$$I_{D_x} = \frac{I_{in}}{2}, \quad x = 1,2,3,4 \tag{21}$$

Based on the gain extension, the current through the diodes D_{int}, D_{M1} and D_{M2} is expressed as

$$I_{D_{int}} = I_{in}\frac{(1-D)^2}{2} \tag{22}$$

$$I_{D_{M1}} = I_{D_{M2}} = I_{in}\frac{(1-D)^2}{2nk} \tag{23}$$

The current through D_0 is equal to load current and given by

$$I_{D_0} = I_o \tag{24}$$

4.5 Design of energy storage elements

The values of the inductors in the two interleaved phases are determined from their respective current ripple magnitudes. The inductance values are designed using

$$L_1 = L_4 = \frac{V_{in}D}{2f\Delta i_{in}} \tag{25}$$

$$L_2 = \frac{V_{C_1}D}{f\Delta i_{L_2}} \text{ and } L_5 = \frac{V_{C_2}D}{f\Delta i_{L_5}} \tag{26}$$

where f is the switching frequency and Δi is the current ripple in individual inductors.

In the proposed converter, inductors L_3 and L_4 are determined from the turns ratio of CIs using (27) and (28)

$$n = \frac{M(1-D)^2 - 2}{2k} \tag{27}$$

$$L_3 = n^2L_2 \text{ and } L_6 = n^2L_5 \tag{28}$$

Since the proposed CI-IQBC is synthesised from an interleaved structure, operating the switches at $D = 0.5$ results in zero input current ripple. A practical voltage gain of 21.11 is required for 18–380 V application. Fig. 5*a* shows the ideal voltage gain plot when turns ratio n is varied from $n = 1.5$ to 3.0. Moreover, the practical value of k tends to be <1 due to leakage inductance. To appreciate the impact of k on voltage gain, M versus D is plotted and presented in Fig. 5*b*. The experimental value of k is determined to be $k = 0.85$. Fortunately, the reduction in voltage conversion ratio value is negligible at $k = 0.85$ when compared to $k = 1$. Thus, the practical operating point is obtained when the switches are operated at $D = 0.5$ and the CIs of the converter are manufactured with $n = 2$; the coefficient of coupling is $k = 0.85$.

The capacitors C_1 and C_2 are regular output capacitors of a CBC. Hence their values are obtained using

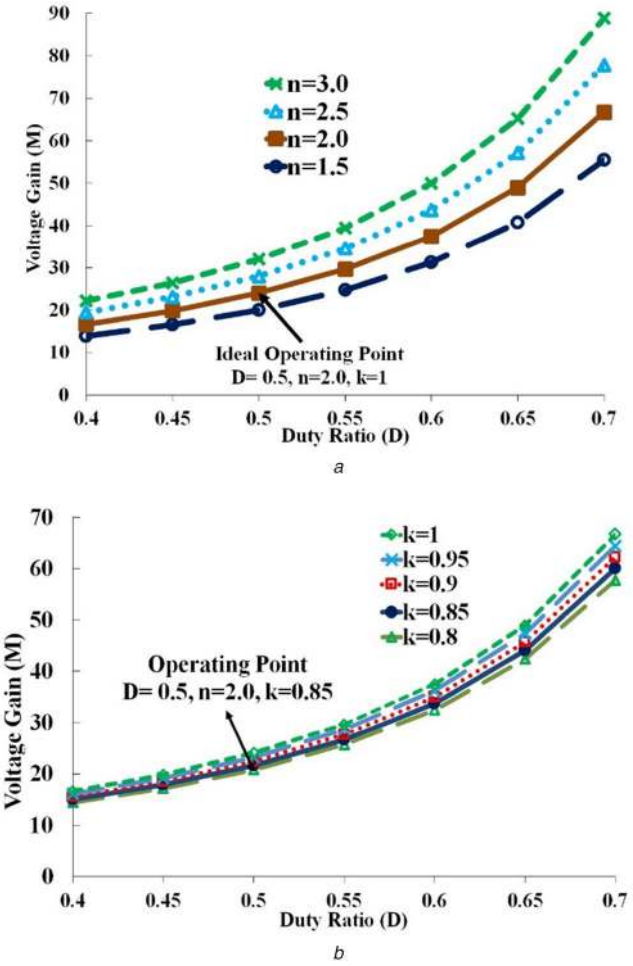


Fig. 5 *Voltage gain plots showing the*
(a) Ideal voltage gain plot when turns ratio n varies,
(b) Actual voltage gain with $n = 2.0$ when coupling coefficient k varies

Table 1 Proposed converter specifications

Parameter	Value
input voltage (V_{in})	18 V
output voltage (V_0)	380 V
output power (P_0)	150 W
switching frequency (f)	50 kHz
inductance value of CI windings (L_1: L_2: L_3) and (L_4: L_5: L_6)	50:100:400 μH
coupling coefficient (k)	0.85
turns ratio (n)	2.0
duty ratio (D)	0.5

$$C_1 = \frac{I_{L_2} D}{f \Delta v_{c_1}} \text{ and } C_2 = \frac{I_{L_5} D}{f \Delta v_{c_2}} \tag{29}$$

C_0 is the output capacitor of the CI-IQBC. The value of output capacitance is calculated based on the load current and output voltage ripple as presented in

$$C_0 = \frac{I_0 D}{f \Delta v_0} \tag{30}$$

5 Experimental results and inferences

The proposed gain extension concept is validated by carrying out experiments on a laboratory prototype version of the CI-IQBC with the specifications and components detailed in Tables 1 and 2, respectively. STM32F411RE microcontroller is suitably programmed and the gate pulses to switches S_1 and S_2 are obtained.

Table 2 Components employed in the prototype CI-IQBC along with their ratings

Circuit element	Device type	Part No. (ratings)
switches (S_1, S_2)	MOSFET	IRFB4228 (150 V, 83 A, 12 mΩ)
diodes (D_1–D_4)	fast recovery diode	MBR1645 (45 V, 16 A, 0.57 V)
diode (D_{int})	fast recovery diode	MBR20200CT (200 V, 20 A, 0.8 V)
diodes (D_{M1}, D_{M2}, D_0)	fast recovery diode	MUR420 (200 V, 4 A, 0.71 V)
capacitor (C_1, C_2)	electrolytic capacitor	ESL107M063AG8AA (100 μF, 63 V)
capacitor (C_{Lift})	polypropylene capacitor	ECW-F2155JA (1.5 μF, 250 V)
capacitor (C_{M1})	polypropylene capacitor	ECW-FD2W475J (4.7 μF/450 V)
capacitor (C_{M2})	electrolytic capacitor	EKXG251ELL100MJ20S (10 μF, 250 V)
capacitor (C_0)	electrolytic capacitor	ESH476M450AM7AA (47 μF, 450 V)

IR25600 dual MOSFET driver provides the required interface between the microcontroller and the power switches. The required voltage and current waveforms are captured using a Tektronix (TPS2024B) 4-channel digital storage oscilloscope. By clamping standard accessories like high voltage (P5210) and current probes (A622) at appropriate test points, the required oscillograms are obtained.

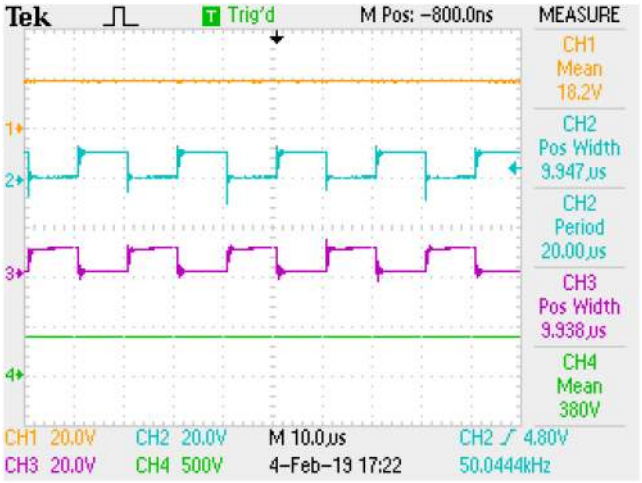
Fig. 6*a* portrays the experimental waveforms that are captured to validate the voltage gain capability of the proposed CI-IQBC. The waveforms represent voltage at the input port (CH1), gate pulses applied to S_1, S_2 (CH2, CH3) and the voltage obtained across the output terminals (CH4) obtained during experimentation. For 18 V DC input, when S_1 and S_2 are operated with $D = 0.5$ at 50 kHz, the desired 380 V is obtained across the output terminals of the proposed CI-IQBC. Thus, the practical voltage gain value is verified to be 21.11. Since hybrid combinations of gain extension concepts like CIs, voltage lift capacitor and VMC are adopted, the required high voltage gain value is obtained by operating the switches at a safe duty ratio of $D = 0.5$.

Fig. 6*b* validates the proper operation of the proposed gain extension network which is employed through stages 1 and 2. Since voltage lift technique is adopted, the voltage obtained across C_{Lift} (top plate) and ground depends on the state of S_1 and S_2.

When S_1 is ON, the bottom plate of C_{Lift} is grounded. However, when S_1 is OFF (and S_2 is ON), the bottom plate of C_{Lift} is held at a potential which is same as the voltage gain of a conventional QBC. Therefore, the voltage across C_{Lift} swings periodically as depicted through the experimental waveform (CH1). The multiplier capacitors (C_{M1}, C_{M2}) are located in stage 2 of the proposed CI-IQBC.

The output voltage obtained from the QBC cells serves as input to the multiplier cells. Therefore, they are charged to a voltage level which is determined by the value of n (turns ratio) combined with the gain obtained from the QBC. The experimental value of voltage developed across C_{M1} and C_{M2} confirms the proper operation of the gain extension technique using VMC network.

Fig. 7*a* demonstrates the voltage stress experienced by the switches S_1 and S_2 and their complementary operation. In the proposed CI-IQBC, the switches are employed in stage 1 which is obtained by interleaving two QBC structures. Resultantly, the switches are operated with 180° phase-shift between them. Therefore, S_1 and S_2 operate in a complementary manner as depicted in the oscillogram (CH2 and CH3) presented in Fig. 7*a*.



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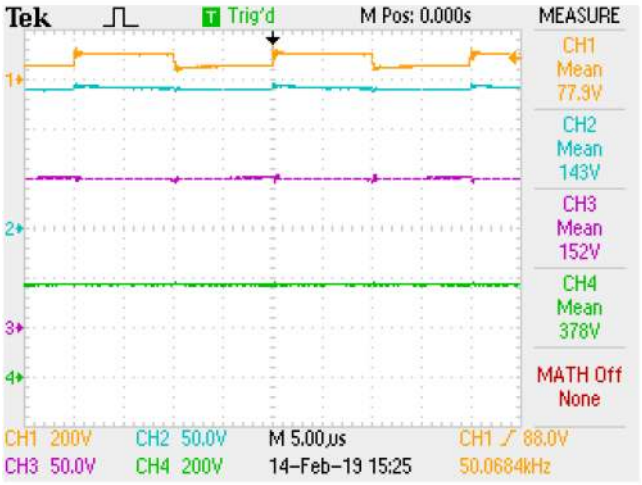
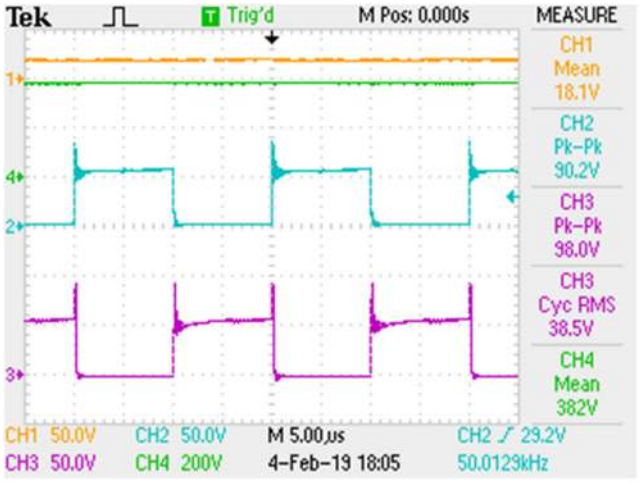


b

Fig. 6 *Test results obtained by carrying out experiments on the prototype converter to demonstrate*

(a) Voltage gain, CH1: voltage at the input; CH2, CH3: triggering pulse of S_1, S_2, respectively and CH4: voltage at output port,

(b) Voltage developed in stages 1 and 2; voltage across C_{Lift} (top plate and ground) (CH1), VMC capacitors C_{M1} and C_{M2} (CH2 and CH3, respectively) and C_0 (CH4)



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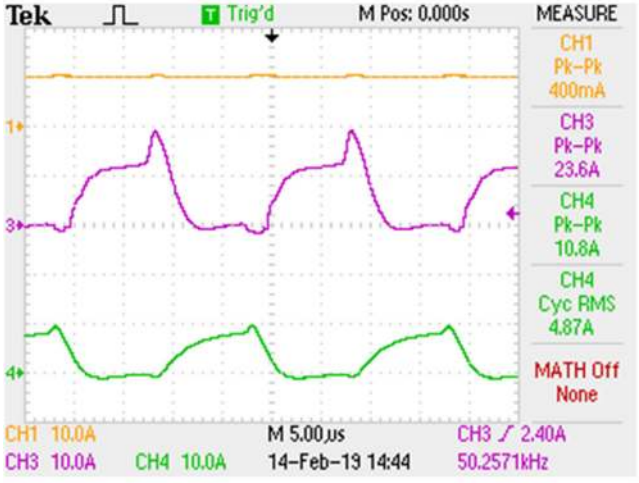


b

Fig. 7 *Practical results obtained from the prototype CI-IQBC to validate voltage and current stress of the switches*

(a) Voltage at the input (CH1), voltage across S_1, S_2 (CH2, CH3, respectively) and output voltage (CH4),

(b) Current through the input (CH1) and switches S_1 (CH3) and S_2 (CH4)

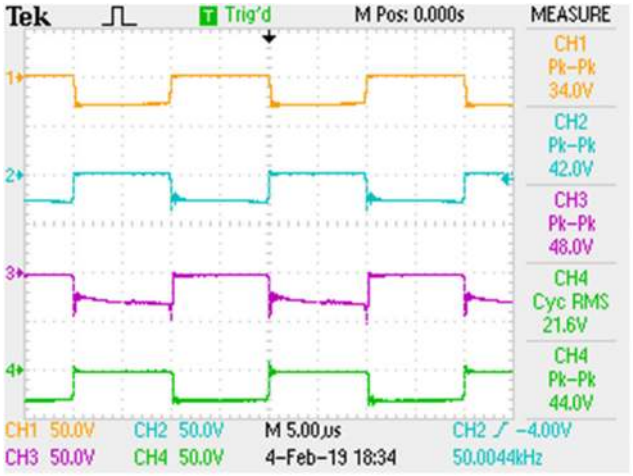
In the proposed CI-IQBC, gain extension is judiciously obtained by adopting two stages; the voltage gain expression (11) is a clear testimony to the fact. Stage 2 contributes to a higher voltage when compared to stage 1. Consequently, S_1 and S_2 experience reduced voltage stress level. Hence, as observed from the experimental waveforms, the practical voltage stress impressed on S_1 and S_2 is only about 18.9% of the output voltage. Moreover, the voltage stress value is in agreement with the value predicted through (12). The spikes are caused by the leakage inductance of the CIs. However, the voltage spike magnitudes are within safe limits. Although the proposed CI-IQBC yields a practical voltage gain of 21.11, the switches are subjected to low voltage stress level which is just a fraction (18.9%) of the output voltage.

Fig. 7*b* depicts the current stress experienced by S_1 and S_2. Due to the interleaving mechanism, the total input current is shared by the switches. Resultantly, the individual current stress value is significantly reduced. The current stress values are in accordance with the theoretical computations. Due to the voltage lift technique, the current through S_1 and S_2 is asymmetrical. However, the overall performance of the proposed CI-IQBC remains unaffected.

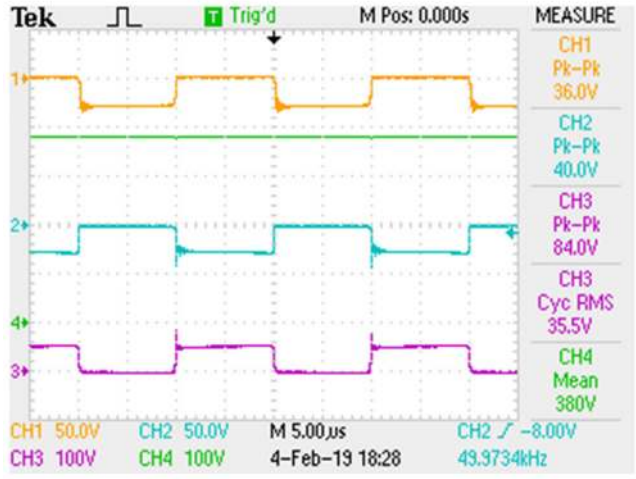
From Fig. 8*a*, the operation of diodes in stage 1 (D_1–D_4) is clearly observed. In each interleaved phase, the diodes operate in a complementary manner; when D_1 is ON, D_2 is OFF and vice versa. Thus, the odd-numbered diodes D_1 and D_3 always operate complimentary to their even-numbered counterparts D_2 and D_4, respectively. Moreover, their voltage rating depends on the nodes at which they are connected and the consequent anode to cathode potential difference.

The odd-numbered diodes (D_1, D_3) serve as the conventional boost rectifier diode and they are located closer to the input port. The reverse voltage impressed across D_1 and D_3 is determined by the potential developed across C_1 and C_2, respectively. Since C_1 and C_2 are the output capacitors of a CBC, D_1 and D_3 are subjected to a reverse voltage which is similar to that of the voltage obtained from a CBC. In addition, the reverse voltage impressed across D_2 and D_4 is derived and presented in (15). Thus, the experimental values of the voltage stress on all the diodes employed in stage 1 clearly validate the correctness of the adopted design procedure.

Fig. 8*b* portrays the precise operation of diodes D_1, D_2 and correlated to S_1. As discussed earlier, D_1 and D_2 operate complementary to one another. Further, when S_1 is turned ON, inductor L_1 begins to store energy and forward biases diode D_2. Thus, the operating states of S_1 and D_2 are similar; both are ON and OFF at the same time intervals. Consequently, S_1 and D_1 operate complimentary to one another. Moreover, as observed from Fig. 8*b*, the magnitude of the voltage stress experienced by the diodes is only about 9.47% of V_0; the experimental value matches very closely with its analytical counterpart derived in (14) and (15). Interestingly, all the semiconductor devices experience reduced stress magnitude due to the judicious employment of gain extension techniques.



a



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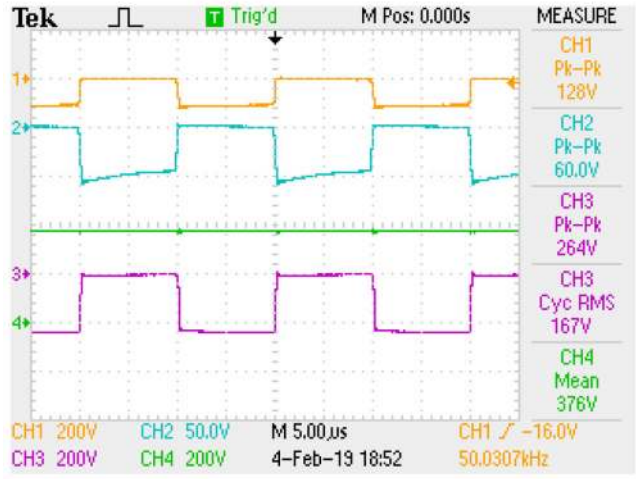


c

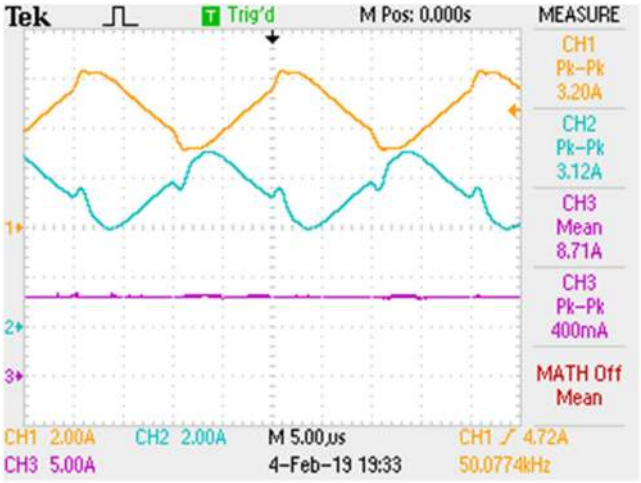
Fig. 8 *Experimental results to validate the voltage stress experienced by the diodes located in stage 1*

(a) Reverse voltage impressed across D_1 (CH1), D_2 (CH2), D_4 (CH3) and D_3 (CH4),

(b) Reverse voltage on D_1 (CH1), D_2 (CH2) compared with voltage across S_1 (CH3) and output voltage (CH4),

(c) Voltage stress on D_{int} (CH1), D_{M1} (CH2) and D_{M2} (CH3) compared with V_0 (CH4)

Fig. 8*c* depicts the voltage stress on the intermediate diode D_{int} and the multiplier diodes D_{M1} and D_{M2}. Diode D_{int} is located between Stage 2 and one QBC structure while the multiplier diodes are placed in stage 2 along with one of the windings of the CIs. Obviously, the multiplier diodes operate complementary to each other. As C_{M2} charges through D_{M1} (and discharges through D_{M2}) when D_{int} is OFF, D_{int} and D_{M1} also operate in a complementary manner. Further, D_{M2} is subjected to the highest voltage stress since it is located closer to the output port; its voltage stress is about 64% of V_0. Nevertheless, as C_{M2} charges, the voltage stress on D_{M2} is reasonably reduced and is lesser than V_0. The oscilloscope waveforms presented in Fig. 8*c* clearly validate the design details and the desired operation of the proposed CI-IQBC.



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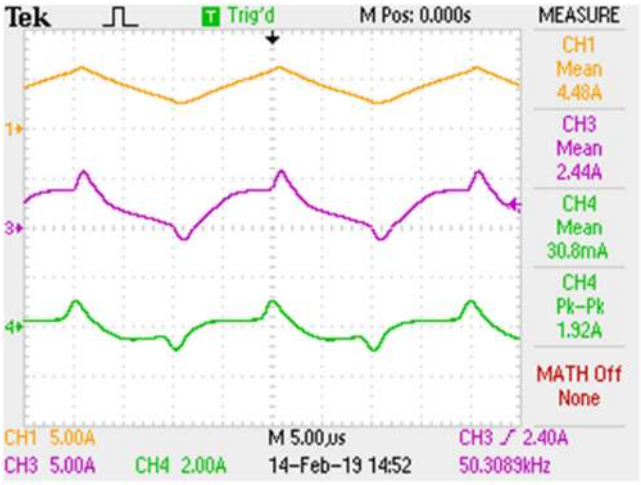

b

Fig. 9 *Experimental results depicting current through the inductors and at the input side*

(a) L_1 (CH1), L_4 (CH2) and I_{in} (CH3),

(b) L_1 (CH1), L_2 (CH3) and L_3 (CH4)

Figs. 9*a* and *b* depict the inductor and input current behaviour. The energy storage inductors L_1 and L_4 charge and discharge linearly. The peak value of both the inductor currents is very close to each other and in accordance with the design values. Further, the phase-shifted operation of the interleaved phases is also validated through the complimentary charging and discharging pattern of L_1 and L_4. Due to phase-shifted operation of the CI-IQBC, the input current is smooth and ripple free. In fact, the ripple magnitude is only 4.5% of the total source current.

The experimental waveforms representing the current through L_1, L_2 and L_3 is presented in Fig. 9*b*. Inductors L_1 and L_2 which are located in stage 1 charge and discharge simultaneously depending upon the state of S_1 while L_3 discharges and charges, respectively. Further, the voltage gain value determines the current magnitude; current through L_2 is almost half of current through L_1. In stage 2, as L_3 transfers its stored energy to C_{M2} and C_{M1} back and forth, its current direction oscillates accordingly as observed in Fig. 9*b*.

Fig. 10*a* shows the experimental waveforms which are obtained from the prototype CI-IQBC operating under full-load condition. The CI-IQBC delivers 150 W at 94.96% efficiency. As discussed,

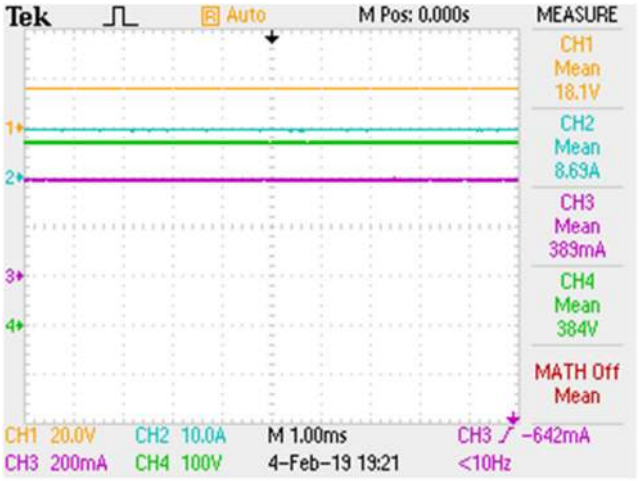

Fig. 10 *Practical results obtained from the prototype CI-IQBC to obtain efficiency under*
(a) Full-load condition – voltage and current at the input side (CH1 and CH2, respectively), load current and voltage (CH3 and CH4, respectively),
(b) Light load condition (132 W) – voltage and current at input (CH1 and CH2, respectively) and output ports (CH3 and CH4, respectively)

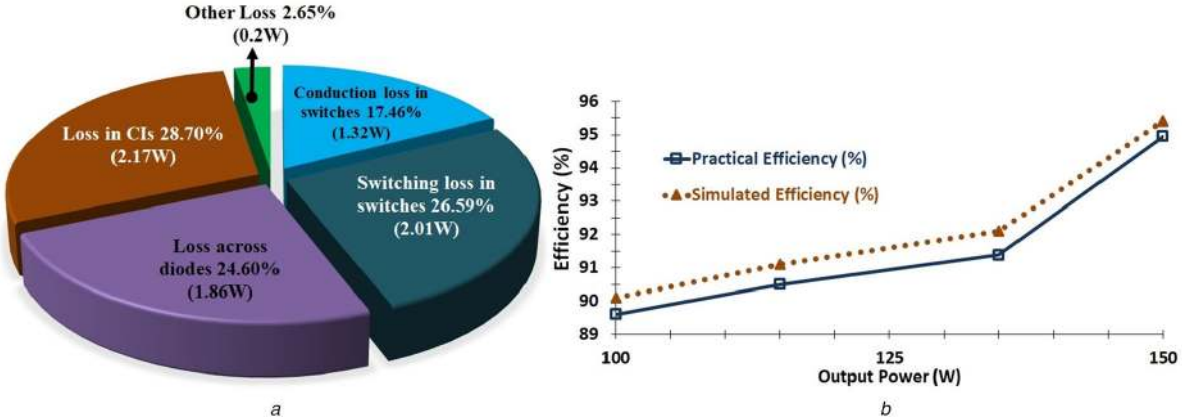

Fig. 11 *Distribution of losses occurring in various components under full-load and efficiency curve*
(a) Power loss dissipated in various elements of the CI-IQBC,
(b) Simulated and experimented efficiency curves

the judicious combination of gain extension mechanisms aid in reducing the voltage rating of the switches. Further, the interleaving mechanism reduces the switch current stress value. Hence, the use of switches with low voltage and current ratings results in good efficiency value. At lightly loaded condition, the proposed converter delivers about 132 W to the load at an efficiency of 91.38% as depicted in Fig. 10*b*. Since the magnetic loss in CIs is independent of the load conditions, the efficiency value is slightly decreased at light load.

The loss distribution profile of various components employed in the proposed CI-IQBC is obtained using the equations presented in [16]. Fig. 11*a* portrays the distribution of various losses occurring in the proposed high-gain CI-IQBC under full-load condition.

Fig. 11*b* depicts the efficiency values obtained while simulating and experimenting the prototype CI-IQBC at various output power levels. The simulated values are in close agreement with the practical values.

The load voltage is regulated against line voltage and load current perturbations to obtain constant output voltage. Figs. 12*a*

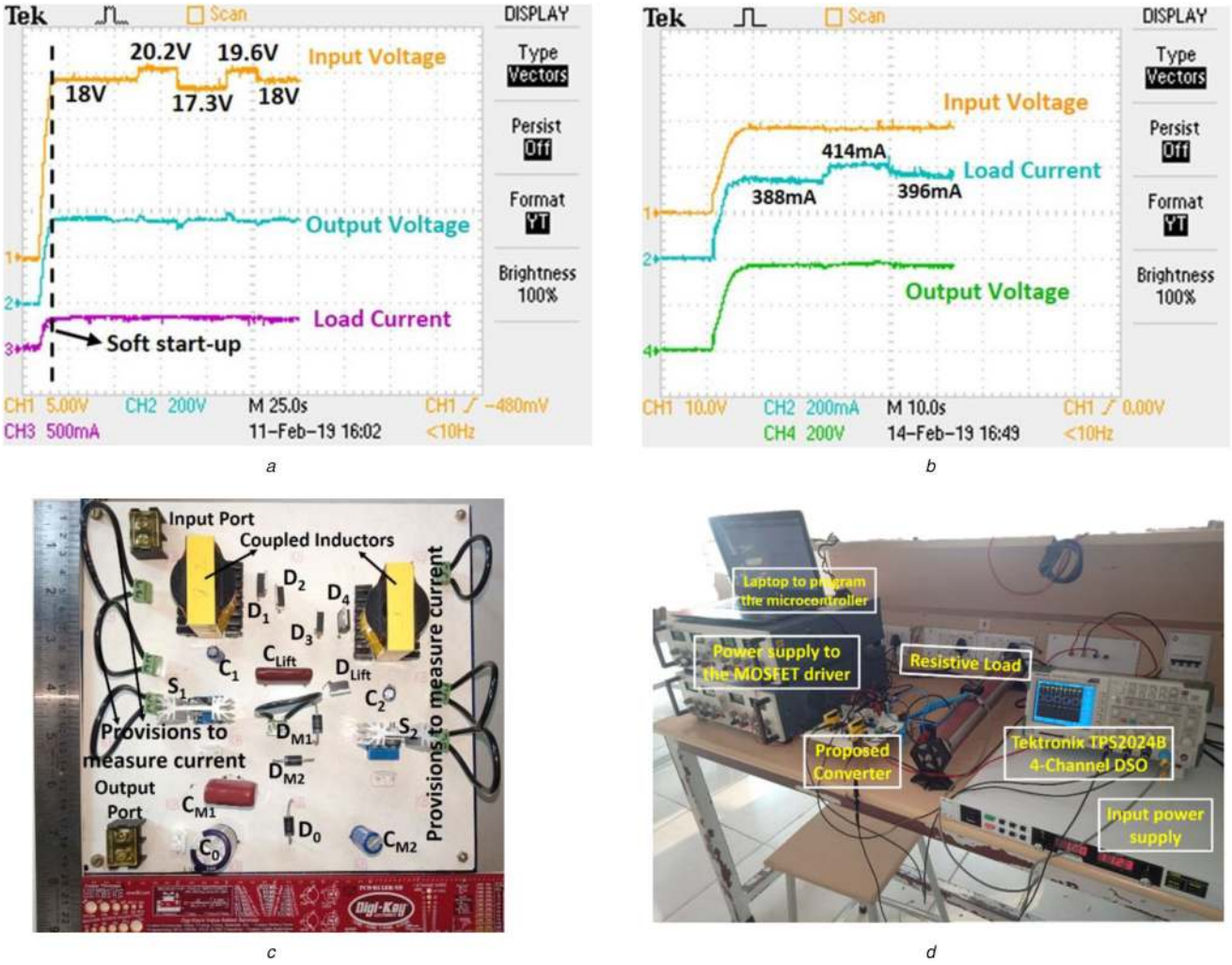

Fig. 12 *Practical oscillograms and photographs of the proposed CI-IQBC*

(a) Demonstration of closed-loop response; load voltage (CH2) is regulated to a constant value when line voltage (CH1) varies,

(b) Dynamic response when load current (CH2) is varied; load voltage (CH3) swiftly settles down to the desired magnitude of 380 V with minimal undershoot and overshoot,

(c) Photograph of the CI-IQBC prototype,

(d) Snapshot of the laboratory test set-up

Table 3 Comparison of the proposed CI-IQBC with basic QBC and its derivatives at $D = 0.5$

Attributes	Basic QBC	QBC in [19]	IQBC with C_{Lift} (Fig. 1*b*)	Proposed CI-IQBC
voltage gain (M)	4	4	8	21.1
switch stress (% of V_0)	100	100	50	18.9
TCC	8	8	14	18
M/TCC	0.5	0.5	0.57	1.17

and *b* portray the load voltage profile. The load voltage is regulated when the line voltage and load current changes in a stepped manner. A simple proportional controller is used to regulate the output voltage. Hence, the load voltage swiftly returns to its desired and nominal value of 380 V. Figs. 12*c* shows the photograph of the laboratory prototype CI-IQBC while the setup used during experimentation is shown in Fig. 12*d*.

6 Some performance indices to benchmark the proposed CI-IQBC

In this section, some key performance indices are benchmarked with few similar and recent converters to appreciate the salient features of the proposed CI-IQBC. Table 3 provides a brief comparison between QBC, its derivatives and the proposed CI-IQBC. Evidently, the proposed converter is superior in terms of voltage gain capability which is achieved with a lower voltage rating of the switches. Table 4 provides a detailed comparison between few converters and the proposed CI-IQBC. Since the modern converters presented in [25–28] are similar to the proposed CI-IQBC, they are compared.

6.1 Voltage gain (M)

The proposed CI-IQBC delivers the highest voltage gain among all the converters which are compared. Converter presented in [26] uses CI alone to achieve a voltage gain of 16.66. The converter in [28] uses stackable QBC structure and provides a voltage gain of only 5. In the proposed CI-IQBC, voltage lift technique, CIs and VMC contribute in obtaining the highest voltage gain of 21.11 at a safe duty ratio value of $D = 0.5$. Fig. 13*a* demonstrates the superior voltage gain capability of the proposed CI-IQBC.

6.2 Voltage stress experienced by the switches

The proposed CI-IQBC employs a couple of switches and is constructed from a two-phase interleaved QBC structure. Resultantly, the voltage magnitude impressed across the switch is similar to the voltage stress experienced by the switch employed in

Table 4 Comparison of the proposed converter with existing converters

Attributes	Converters presented in references				
	[25]	[26]	[27]	[28]	Proposed
voltage gain (M)	10.9	16.67	14.52	5	21.1
duty ratio (D)	0.47	0.4	0.54	0.4	0.50
no. of magnetic elements	2 (1 simple inductor and 1 CI)	2 (1 simple inductor and 1 CI)	2 (1 simple inductor and 1 CI)	2 (simple inductor)	2 CI
turns ratio of CIs (n)	0.81	2	2	—	2
voltage stress on switches as percentage of V_0 (V_{sw})	32.6	20	33.3	100	18.9
M/V_{sw}	0.33	0.83	0.42	0.05	1.11
voltage stress on diodes as percentage of V_0 (V_{diode})	59	33	66.7	33	64.4
M/V_{diode}	0.18	0.50	0.21	0.15	0.32
TCC	14	16	14	8	18
M/TCC	0.77	1.035	0.98	0.625	1.17
gain extension technique	CI and voltage multiplier	CI	CI and voltage multiplier	stackable QBC cells	voltage lift, CI and DCM

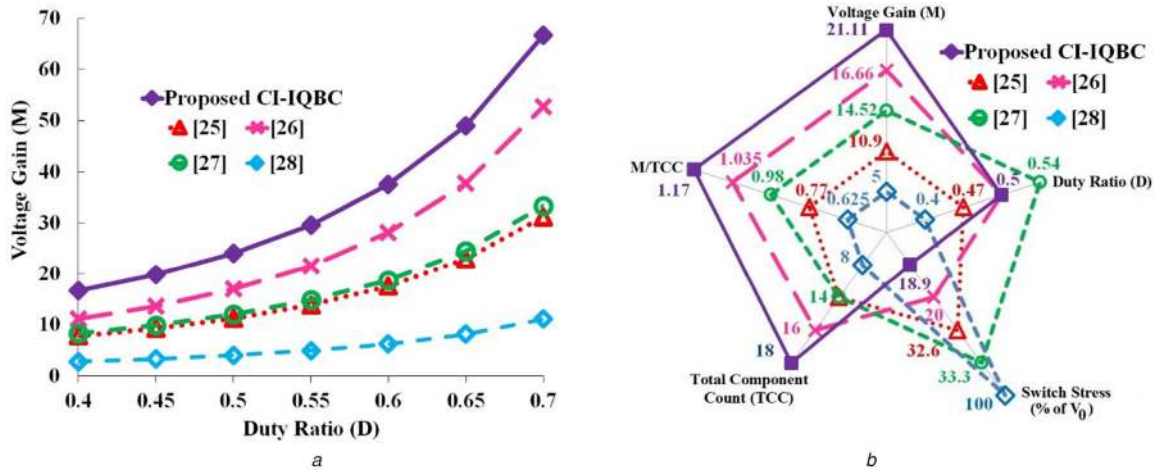

Fig. 13 *Performance plots of the proposed CI-IQBC*
(a) Voltage gain comparison,
(b) Radial chart to demonstrate the advantageous features of proposed converter as compared to some existing state of the converters

QBC. Hence, though the output terminal is at 380 V, the switch is subjected to a voltage stress level which is just about 19% of V_0. Incidentally, all the other converters that are compared (except [28]) also use CIs. Hence, their switch stress magnitude is also less.

The enormous reduction in the switch stress magnitude is well understood by computing the ratio of voltage gain (M) to the switch stress (V_{sw} expressed as the percentage of V_0) and denoted as M/V_{sw}. The proposed CI-IQBC operates with the highest M/V_{sw} value of 1.11. In other words, the proposed CI-IQBC yields the highest voltage conversion ratio by employing switches with lower voltage rating. The second highest M/V_{sw} value of 0.83 is obtained by the converter presented in [26]. Thus, the capability of the proposed CI-IQBC to yield high-voltage gain despite subjecting the switches to lower stress value is clearly highlighted.

6.3 Voltage stress experienced by the diodes

The proposed CI-IQBC uses eight diodes. Diode D_{M2} is subjected to the maximum voltage stress magnitude which is about 64% of V_0. The location of D_{M2} leads to slightly higher voltage stress on it. However, the majority of diodes are subjected to reduced voltage stress levels in the range of 9–37% of V_0. The M/V_{diode} value indicates the reasonably lower voltage stress impressed across the diodes at high-voltage conversion ratios in the proposed CI-IQBC.

6.4 Total component count (TCC) and M/TCC ratio

The TCC value of the proposed CI-IQBC is the highest while it is the least for the converter presented in [28]. However, the proposed converter delivers the highest voltage gain while the converter in [28] the lowest. Resultantly, the M/TCC value is the highest for the proposed converter while it is the lowest for the converter in [28]. The converter presented in [26] uses 16 components which is the second-highest number of components employed; its M/TCC value is also very close to the proposed converter. Each of the other two converters presented in [25, 27] use 14 components and their M/TCC value is also close to one another. The radial chart in Fig. 13*b* highlights the salient features of the proposed CI-IQBC benchmarked against some similar and modern converters.

7 Conclusion

In this paper, a high step-up DC–DC converter which is based on CI is presented. The proposed converter is developed from a simple QBC structure. Voltage lift technique, multi-winding CIs and the VMC network enhance the voltage conversion ratio of the presented CI-IQBC which yields a voltage gain of 21.11 under practical condition. The basic IBC structure helps to reduce the current stress on the switches. Moreover, operating the switches at $D = 0.5$ along with a phase-shift of 180° reduces the current ripple at the input side to 4.59% of I_{in}. Further, as voltage gain is extended by employing hybrid combination of gain extension techniques, the voltage rating of the switches is also only a fraction (18.9%) of V_0. The proposed converter provided a practical voltage

gain of 21.11 and delivered 150 W power to the load 94.96% efficiency. Simple closed-loop control is employed to obtain a constant voltage of 380 V across the load despite step change in the line voltage and load current magnitudes. Some of the salient features of the proposed CI-IQBC are its ability to (i) achieve high-voltage conversion ratio (21.11) at a safe duty ratio value ($D = 0.5$), (ii) provide the required conversion ratio value by employing switches with low-voltage rating (18.9% of V_0) only, (iii) draw a fairly smooth current from the input port with very low ripple content (4.59% of I_{in}) and (iv) provide regulated voltage to the load even when the voltage at the input and current drawn by the load are subjected to a step change. Therefore, the proposed CI-IQBC proves to be a suitable alternative topology for integrating PV source to 380 V DC bus employed in a DC microgrid.

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