IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

Design, analysis, and implementation of a new high step-up DC–DC converter with low input current ripple and ultra-high-voltage conversion ratio

ISSN 1755-4535
Received on 6th March 2020
Revised 14th June 2020
Accepted on 1st July 2020
E-First on 21st September 2020
doi: 10.1049/iet-pel.2020.0256
www.ietdl.org

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Abstract: In this study, the analysis and design of a coupled-inductor (CL)-based ultra-high step-up single-switch DC–DC converter are presented. With the aid of the CL and voltage multiplier cell, the suggested topology can obtain ultra-high-voltage gain without a large turn ratio and extreme duty cycle. A passive clamp circuit is utilised in the structure of the introduced converter for not only alleviating voltage spike on the main switch effectively but also recycle the leakage inductance energy. So low-voltage rating and low on-state resistance metal oxide semiconductor field-effect transistor is allowed to increase efficiency and lower the conduction losses. The input current ripple of the suggested topology is very low due to connecting an inductor to the suggested structure input section, which is very friendly and desirable to the photovoltaic and fuel cell applications. The suggested converter steady-state analysis, operation principle, theoretical efficiency analysis, and design procedure are described comprehensively in this study. Furthermore, the suggested converter superiority is illustrated over various alike recently introduced the most important DC–DC structures in the comparison study. Finally, a laboratory prototype is fabricated with a 225 W output power to confirm the theoretical analysis of the introduced converter.

Nomenclature

V_{in}, V_O	input voltage, output voltage
V_S	voltage across the main power switch
V_C	voltage across capacitor
V_{LNP}	primary side voltage of the coupled-inductor (CL)
V_{LNS}	secondary side voltage of the CL
V_D	voltage of the diode
I_S	current of the main power switch
I_D	current of the diode
I_{Lk}	leakage inductance current
I_{Lm}	magnetising inductance current
I_L	input current or input inductor current
I_O	current of the load
D	duty cycle of the switch
n, k	turn ratio and coupling coefficient of the CL
f_S	switching frequency
M	voltage gain of the converter
ΔIL_{in}	current ripple of the input inductor
ΔIL_m	current ripple of the magnetising inductance
$P_{RDS(on)}$, P_{SW}	conduction and switching loss of the switch
P_{RF-D}, P_{VF-D}	diode forward resistance and voltage losses
P_{rC}	power losses of the capacitor
P_{R-L}	conduction losses of the input inductor
P_{R-CL}	conduction losses of the coupled inductor
P_{core}	inductors core losses
η	efficiency of the converter

1 Introduction

In the past few decades, high step-up DC–DC converters have drawn significant attention in several application areas, especially in renewable energy systems. The clean energy development such as charging stations of electric vehicle or uninterruptable power supply systems, photovoltaic (PV) panels or fuel cells (FCs), and data center DC distribution networks are different instances for the usage of the DC–DC structure [1, 2]. In [3], the usage of the DC–DC topologies for sustainable energy resources integration such as PV and FCs through block diagrams are presented. Commonly, the produced voltage levels of the clean energy systems, for instance, photovoltaic and FCs, are low as making them inappropriate to link them to the grid directly. So, the boost DC–DC structures are required to boost the output DC voltage level of this type of energy source [4–6]. For example, in PV systems, the PV panel output voltage is about 24–40 V. Thus, to connect the PV panel to the grid, the output voltage should be increased at least to 300 V [7, 8]. So, a high step-up DC–DC converter with significant high-voltage gain is needed to connect PV panels to the grid. Also, power regulations and output voltage of FCs are other issues that should be considered. In [9], most of the converters with high-step-up, high-efficiency, and low-cost performance are covered and classified into several categories. Moreover, the disadvantages and advantages of these topologies are discussed too.

It is worth noting that having a characteristic of the meagre input current ripple is another significant property for high step-up DC–DC converters. In PV systems, maximum power point tracking is essential and vital. So, to track the maximum power point in PV systems, the high-boost DC–DC topologies must have a continuous input current [10, 11]. Also, the continuous input current high step-up converters may track the maximum power point with lower oscillation. Moreover, the DC–DC converters with continuous input current are favourable for the operation of FCs too [12].

In [13, 14], topologies with high-voltage gain that have current ripple cancellation ability at a preselected duty cycle have been proposed. The proposed proportional strategy in these topologies is an optimised method for minimising input current ripple at other operating duty cycles. Removing the input current ripple by preselected duty cycle results in having a higher voltage gain.

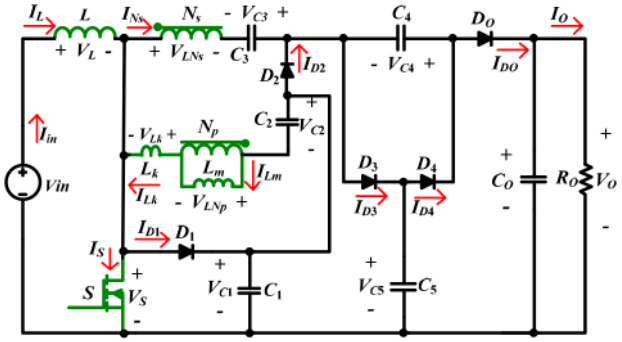

Fig. 1 *Introduced topology equivalent circuit*

Furthermore, in such DC–DC converters, common ground among load and input source is considered as an essential property so that its inexistence restricts converters implementation for grid-tied transformer-less PV applications [15].

How to design DC–DC converters to have a continuous input current and how to increase voltage conversion ratio, decline the voltage stress of the semiconductors, and increase high-boost DC–DC topologies conversion efficiency are the main and important issues in designing converters. The enhancement of some of these parameters and satisfying the others in an appropriate value are the main goals of the researchers.

Recently, several high step-up DC–DC converters have been suggested in the literature. The conventional converters such as Zeta, boost, Cuk, and primary-inductor single-ended converter have been extensively utilised due to their simple structures. However, low-voltage conversion ratio and high-voltage stress amongst switching components are the major disadvantages of these converters. It is noteworthy that, in very large duty cycles, these converters can have a high-voltage conversion ratio; however, their efficiency declines remarkably [16, 17].

In the isolated converters, by applying transformers with a large turn ratio, a high-voltage gain can be obtained. However, having a great turn's ratio results in a considerable coupled-inductor (CL) leakage inductance that enhances the switch voltage stress and declines the topology efficiency [18]. The boost converters based on the switched capacitor and switched inductor are other types of high step-up DC–DC converters for increasing the voltage conversion ratio [19–21]. These types of converters have been used extensively to achieve a high-voltage conversion ratio. Nevertheless, in the topologies with the switched capacitors, the high-current stress on the semiconductors is the main problem, and in the switched inductor converters, the switches and diodes voltage stress is high. In [22], a few simple structures of switching, formed by either two inductors and two–three diodes (L-switching), or two capacitors and two-three diodes (C-switching) are proposed.

A new structure for a step-up DC–DC converter with a high-voltage transfer gain with a lower duty cycle is proposed in [23]. Low-voltage stress and low current on the switch, the input filter, and reduced inductors size are the main advantages of the converter. Nevertheless, the voltage gain of that is not high enough and can be increased more.

Another type of boost converter that is very popular among researchers is coupled inductor (CL)-based boost converters [24, 25]. However, in the converters based on CL, the CL leakage inductance remained energy must be recovered. Otherwise, this causes severe voltage spikes and electromagnetic interface problems. To overcome this problem, structures such as passive and active clamps circuits have been proposed. It worth noting that in the structures with CL and with clamp circuits, the switching element voltage stress is low. Thus, switching components with light conduction losses and small $R_{DS(on)}$ may be applied. The proposed topology voltage stress on the power switch can be reduced, and the efficiency can be enhanced by using a passive clamp circuit. Moreover, due to the secondary leakage inductance of these converters, the output diode has low reverse recovery ringing [26, 27].

Besides, it should be noticed that when high-turn ratio and large duty cycle are applied to obtain a large conversion ratio, converter power losses increase [28–30]. To decrease the ripple of the input current in the coupled inductor-based DC–DC converters, an inductor is connected in series to the input section of the converter [31]. Also, continuity of the input current causes the root-mean-square value of the input inductor and the switch currents to be reduced, which increases the efficiency [32–34]. Nevertheless, the conversion ratio of these converters is still low that can be improved.

Recently, different high-gain CL-based DC–DC topologies with three windings have been introduced in [35, 36], which results in owing voltage stress and voltage gain rather flexible regulation. In three winding CL-based converters, three degrees of freedom are utilised to adjust the voltage conversion ratio of the converters, i.e. the turn ratios of CL, the number of the windings of CL, and the duty ratio of switches [37–39]. However, the voltage conversion ratio is still not high enough and should be increased.

To solve the problems as mentioned above, in this paper, a new ultra-high step-up DC–DC converter with a single-switch based on voltage multiplier cell (VMC) and the CL is proposed. The integration of a VMC with CL in the introduced structure configuration leads to owning a very ultra-high voltage conversion ratio. For declining the presented topology input current ripple significantly, an inductor is applied in the proposed topology input section. Furthermore, to decrease the voltage stress across the main power switch and recycle the leakage inductance energy, a passive voltage clamp circuit in the presented topology configuration is applied. This leads to choosing a low on-state resistance and voltage-rating switching element in the suggested configuration to decrease the conduction loss. Achieving ultra-large voltage conversion ratio in very proper duty cycles by applying light coupled inductor turn ratio, continuous input current, low-voltage stress across semiconductors, and high efficiency are the main features of the introduced converter. Moreover, the suggested converter has other merits such as elimination of diodes reverse recovery issue because of operating in low-duty cycles, leakage inductance energy recovery, having smaller leakage inductance because of the low-number of turns and applying of only one power switch. The aforementioned features of the proposed converter makes it very proper for applying it in renewable energy systems such as FCs and PVs.

The rest of the paper is organised as follows: the suggested topology operation principle and steady-state analysis in continuous conduction mode (CCM) are studied and analysed entirely in Section 2. In Section 3, the design guidelines of the suggested converter are discussed. In Section 4, the efficiency analysis of the introduced topology is presented in detail, and in Section 5 comparison of the introduced converter with various alike configurations is given. Section 6 presents the experimental measurement results of a laboratory prototype of the converter, and finally, conclusions are given in Section 7.

2 Steady-state analysis and operation principle of the suggested DC–DC converter

The introduced ultra-high-voltage gain single switch DC–DC converter equivalent power circuit based on CL and VMC with continuous input current is illustrated in Fig. 1. As depicted in Fig. 1, the suggested structure includes one inductor, a power switch S, one coupled inductor, five capacitors C_1–C_5, four diodes D_1–D_4, an output filter capacitor C_O, and an output diode D_O. In the structure of the proposed topology utilising one power switch is a merit for the converter. Also, in the input stage of the converter, an inductor is applied that results in a very low ripple input current that is very good for renewable energy resources. The CL is modelled as an ideal transformer with a turn ratio N_p:N_s, a magnetising inductance, L_m, and leakage inductance, L_k. The ideal transformer primary and secondary windings turn numbers are N_p and N_s, respectively. Besides, the turn's ratio of the coupled inductor is considered as $n = N_s/N_p$. The capacitor C_1 and diode D_1 operate as passive clamp circuit components to recycle the energy

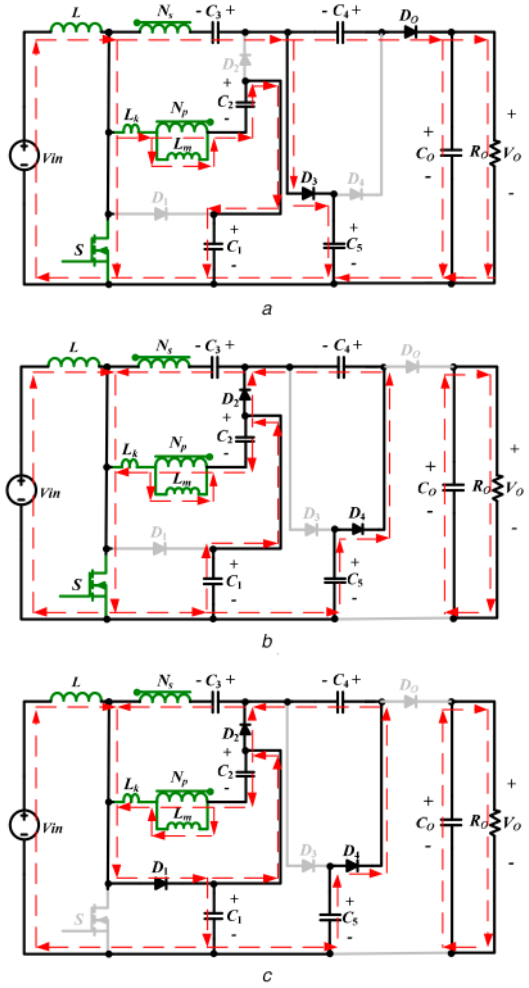

Fig. 2 *Current flow paths of introduced topology at CCM operation in one period*
(a) State 1, ***(b)*** State 2, ***(c)*** State 3

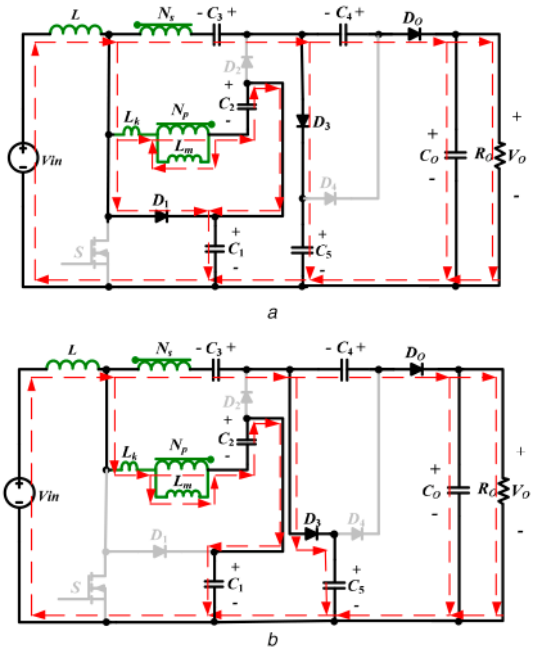

Fig. 3 *Current flow paths of introduced topology at CCM operation in one period*
(a) State 4, ***(b)*** State 5

of the leakage inductance and clamps the voltage across switch S. This leads to utilising a low on-state resistance switch in the converter structure to decrease the conduction loss. The diodes D_3 and D_4 and capacitors C_4 and C_5 work as a VMC network to further enhance the voltage gain of the presented configuration.

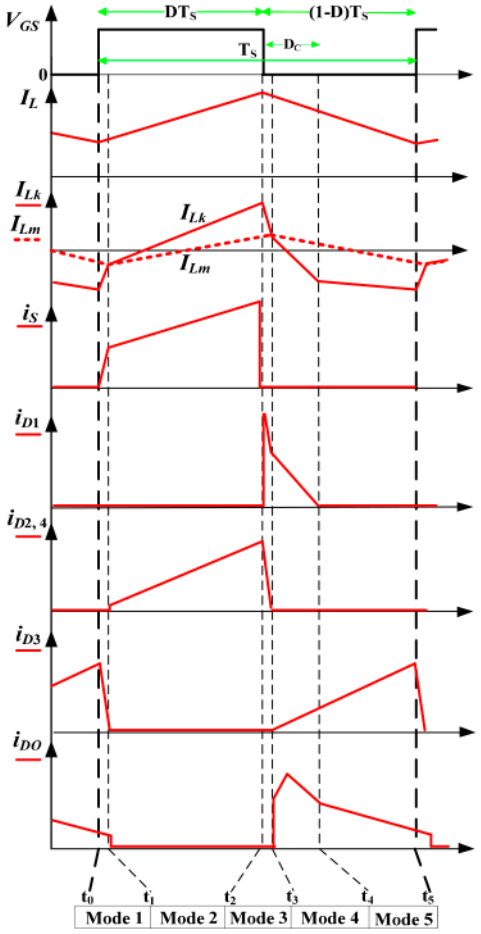

Fig. 4 *Key waveforms of the introduced topology in CCM*

To simplify the theoretical analysis of the introduced configuration, some assumptions are considered as presented below:

(i) All components are considered to be ideal, but the leakage inductance of CL is considered.
(ii) All capacitors are considered large enough; so, their voltage ripple is negligible.
(iii) The inductors $L_{\rm m}$ and $L_{\rm in}$ are considered large enough; thus, their current ripple is negligible.
(iv) The CL coupling coefficient, k, is equal to (1).

$$k = \frac{L_{\rm m}}{(L_{\rm m} + L_k)} \tag{1}$$

The operation principle of the presented structure in CCM includes five states. Figs. 2 and 3 illustrate the presented topology current flow path at different operating states, and in addition, the general waveforms of the CCM operation of the suggested topology are indicated in Fig. 4. The relevant states are expressed below:

Mode 1 [t_0, t_1]: In this time transition, the main switching element S starts to conduct. In this short time interval, the input inductor is charged by the input DC voltage. Moreover, according to the ideal transformer principle, since the current of the leakage inductance, I_{Lk}, increases linearly, the CL secondary side current, I_{Ns}, decreases linearly. According to Fig. 2*a*, capacitors C_2, C_3, and C_4 are discharged, and the energies of C_3 and C_4 are delivered to the C_O and load, and the C_5 capacitor is charged too. When I_{Lm} equals the I_{Lk}, this stage will end.

Mode 2 [t_1, t_2]: In this time interval, the power switch S is still conducting, as depicted in Fig. 2*b*. The input inductor is magnetised via input DC voltage too. During this time interval, the

magnetising and leakage inductances are energised via the input DC voltage, and the I_{Lm} and I_{Lk} enhance linearly. The charging of the C_4 capacitor is continued too. Also, the L_{NS} charges capacitor C_3 too. Moreover, in this state, the load is supplied by C_O. When the main switching element S is turned off, this stage finishes.

Mode 3 [t_2, t_3]: In the third mode, as indicated in Fig. 2*c*, the main switching element S is blocked. In this mode, the leakage inductance energy is recycled to C_1 and charges it by D_1. Also, L_k is demagnetised until the current of that equals to the current of L_m. The winding N_s also charges capacitor C_3 in the third mode. Moreover, capacitor C_4 is still charged. In addition, the output load received energy from the output capacitor. With I_{Lk} and I_{Lm} being identical, the third mode will finish too.

Mode 4 [t_3, t_4]: In the fourth mode (as shown in Fig. 3*a*), switch S is becoming blocked too. In this stage, according to the principle of the ideal transformer, since I_{Lm} and I_{Lk} decline linearly, the I_{Ns} is increased linearly. The energy of L_k is continued to recycle in the fourth mode, and the capacitor C_1 is charged by D_1 too. Furthermore, the input inductor, L, and capacitors C_3 and C_4 energy is transferred to the output.

Mode 5 [t_4, t_5]: As demonstrated in Fig. 3*b*, in the last time interval, the main switching element S is blocked. In the last mode, I_{Lk} and I_{Lm} decline linearly, and the C_5 capacitor is continued to charging too. Also, the input inductor, L, and capacitors C_3 and C_4 energy are transferred to the output too. After this state, the next switching cycle begins to start.

The steady-state analysis of the converter is necessary for evaluating the introduced topology performance. Moreover, according to the operation principle of the introduced configuration, the time intervals of the modes 1 and 3 are very short. So, they can be neglected in the steady-state analysis.

In mode 2, the main power switch is ON and by applying Kirchhoff's voltage law on the circuit, the inductors voltage can be calculated as

$$V_L = V_{in} \tag{2}$$

$$\begin{aligned} V_{Lm} &= \left(\frac{L_m}{(L_m + L_k)}\right)(-V_{C2} + V_{C1}) \\ &= k(-V_{C2} + V_{C1}) \end{aligned} \tag{3}$$

$$\begin{aligned} V_{Lk} &= \left(\frac{L_k}{(L_m + L_k)}\right)(-V_{C2} + V_{C1}) \\ &= (1-k)(-V_{C2} + V_{C1}) \end{aligned} \tag{4}$$

$$V_{LNs} = V_{C3} - V_{C1} = nk(-V_{C2} + V_{C1}) \tag{5}$$

Also, the voltage across capacitor C_4 is as follows:

$$V_{C4} = V_{C5} - V_{C1} \tag{6}$$

The main switching element S is in off-state, and the magnetic inductor is discharged in the time intervals of 4 and 5. By using the following equations, the voltage of inductors is determined:

$$V_L = V_{in} - V_{C1} \tag{7}$$

$$V_{Lm} = k(-V_{C2}) \tag{8}$$

Furthermore, the equation of the output voltage is determined as

$$V_O = V_{C4} + V_{C5} \tag{9}$$

Also, the voltage of the capacitor C_5 is determined as presented below

$$\begin{aligned} V_{C5} &= V_{C3} - V_{LNs} - V_L + V_{in} \\ &= V_{C3} + nkV_{C2} + V_{C1} \end{aligned} \tag{10}$$

By utilising the voltage-second balance principle for inductors, the voltages of the capacitors can be obtained. So, by applying this principle to the input inductor, L, and magnetising inductor, L_m, the equations of capacitor C_1 and C_2 are determined

$$V_{C1} \simeq \frac{V_{in}}{(1-D)} \tag{11}$$

$$V_{C2} = DV_{C1} = D\left(\frac{V_{in}}{(1-D)}\right) \tag{12}$$

By substituting (11) and (12) into (5) and simplifying the equations, the voltage equation of capacitor C_3 is achieved as follows:

$$V_{C3} = \frac{(nk - nkD + 1)}{(1-D)}V_{in} \tag{13}$$

Moreover, by using (11), (12), (13), and (10) the voltage of capacitor C_5, V_{C5}, is achieved as follow:

$$V_{C5} = \frac{(kn + 1 + k + (1-k)(1-D))}{(1-D)}V_{in} \tag{14}$$

From (6) and also, by using (13) and (11), the capacitor C_4 voltage is obtained as

$$V_{C4} = \frac{(kn + k + (1-k)(1-D))}{(1-D)}V_{in} \tag{15}$$

Finally, from (14), (15), and (9), the introduced converter voltage conversion ratio in CCM, M_{CCM}, is obtained as follows:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{(2kn + 2k + 1 + 2(1-k)(1-D))}{(1-D)} \tag{16}$$

Fig. 5*a* shows the voltage conversion ratio against D by considering the effect of the leakage inductance under several k, and by considering $n = 2$. It is obvious that the existence of the leakage inductor of the CL does not have an impressive effect on the voltage conversion ratio; thus it can be ignored. So, if the leakage inductance of the CL is ignored, i.e. the coupling coefficient k is identical to 1, the ideal voltage conversion ratio of the presented topology and capacitors voltage is obtained as follows:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{(2n+3)}{(1-D)} \tag{17}$$

$$V_{C3} = \frac{(n - nD + 1)}{(1-D)}V_{in} \tag{18}$$

$$V_{C5} = \frac{(n+2)}{(1-D)}V_{in} \tag{19}$$

$$V_{C4} = \frac{(n+1)}{(1-D)}V_{in} \tag{20}$$

To simplify the suggested structure analysis in the next sections, considering that the leakage inductance is decidedly smaller than the magnetising inductance, and according to the issue mentioned above, the coupled inductor leakage inductance is neglected, i.e. the coupling coefficient k is assumed to be 1. In addition, the presented topology ideal voltage gain in CCM, M_{CCM}, against the duty cycle of the switch, D, under several coupled inductor turn ratios, n, is illustrated in Fig. 5*b*. It is very clear that the coupled inductor turn ratio, n, can be regulated to achieve a very high-voltage gain without operating at a large turn ratio of the coupled inductor and using a huge duty cycle.

3 Introduced topology design procedure

The design procedure of the suggested topology is a very important issue for operating presented converter in a very optimal condition. So, several requirements are determined for the design of the proposed topology.

Moreover, the design procedure of the suggested topology is presented for a prototype example with 50 kHz switching frequency, 29 V input, and 226 W/382 V output.

As illustrated in Fig. 1, the suggested configuration has five diodes and a power switch. Thus, to select the suitable elements for the suggested configuration, switching components current and voltage stresses should be determined. To withstand the switching devices in the operational conditions, they must be chosen based on the current and voltage stresses on them.

3.1 Current stress analysis

One of the essential factors in choosing appropriate switching devices is the current stress of the semiconductors. The switching components should be chosen to withstand the maximum current flow. With regard to the steady-state analysis, the magnetising inductance current ripple and input current ripple in CCM operation is determined below

$$\Delta I_{\text{in}} = \Delta I_L = \frac{DV_{\text{in}}}{Lf_{\text{s}}} = \frac{DV_{\text{O}}(1-D)}{Lf_{\text{s}}(2n+3)} \tag{21}$$

$$\Delta I_{L\text{m}} = \frac{DV_{\text{in}}}{L_{\text{m}}f_{\text{s}}} = \frac{DV_{\text{O}}(1-D)}{L_{\text{m}}f_{\text{s}}(2n+3)} \tag{22}$$

Furthermore, the average current of the magnetising inductance and input current average value is determined as follows:

$$I_{\text{in}} = I_L = \frac{(2n+3)}{(1-D)}I_{\text{O}} \tag{23}$$

$$I_{L\text{m}} = (n+1)I_{\text{O}} \tag{24}$$

Thus, the peak value of the input inductor and $I_{L\text{m}}$ is equal to (25) and (26)

$$I_L^{(\text{peak})} = I_{\text{in}}^{(\text{peak})} = \frac{(2n+3)}{(1-D)}I_{\text{O}} + \frac{1}{2}\frac{DV_{\text{in}}}{Lf_{\text{s}}} \tag{25}$$

$$I_{L\text{m}}^{(\text{peak})} = (n+1)I_{\text{O}} + \frac{1}{2}\frac{DV_{\text{in}}}{L_{\text{m}}f_{\text{s}}} \tag{26}$$

According to Fig. 4, by applying the ampere-second balance law on all capacitors and in terms of the steady-state analysis of the CCM operation, the diodes average currents are identical to the output current, I_{O}. Thus, the main power switch peak current and the peak current values of the diodes can be calculated as follows:

$$I_{D_2}^{(\text{peak})} = I_{D_4}^{(\text{peak})} = \frac{2I_{\text{O}}}{D} \tag{27}$$

$$I_{D_3}^{(\text{peak})} = I_{D_{\text{O}}}^{(\text{peak})} = \frac{2I_{\text{O}}}{(1-D)} \tag{28}$$

$$I_{\text{S}}^{(\text{peak})} = \left(\frac{4n + D^2(n+1) - D(3n+2) + 4}{D(1-D)}\right)I_{\text{O}} \tag{29}$$

According to Fig. 4, the time transition of mode 4, D_{C} based on capacitors charge balance is obtained as follows:

$$D_{\text{C}} = \frac{2(1-D)}{(2n+2)} \tag{30}$$

Thus, applying (30), the diode D_1 current peak value, $I_{D_1}^{(\text{peak})}$, is achieved as

$$I_{D_1}^{(\text{peak})} = \frac{2(i_{D_1})}{D_{\text{C}}} = \frac{2I_{\text{O}}}{D_{\text{C}}} = \frac{(2n+2)I_{\text{O}}}{(1-D)} \tag{31}$$

3.2 Voltage stress analysis

With regard to the analysis presented in previous sections and according to Figs. 2 and 3, the voltage stresses across the main power switch and diodes can be achieved as follows:

$$V_{\text{stress}-S_1} = \frac{1}{(1-D)}V_{\text{in}} = \frac{1}{(2n+3)}V_{\text{O}} \tag{32}$$

$$V_{\text{stress}-D_1} = -\frac{1}{(1-D)}V_{\text{in}} = -\frac{1}{(2n+3)}V_{\text{O}} \tag{33}$$

$$V_{\text{stress}-D_{2,3}} = -\frac{(n+1)}{(1-D)}V_{\text{in}} = -\frac{(n+1)}{(2n+3)}V_{\text{O}} \tag{34}$$

$$V_{\text{stress}-D_{4,\text{O}}} = -\frac{(n+1)}{(1-D)}V_{\text{in}} = -\frac{(n+1)}{(2n+3)}V_{\text{O}} \tag{35}$$

According to (32)–(35), one of the most important advantages of the suggested structure is reduced voltage stress across switching devices that leads to select low-voltage rating components.

3.3 Capacitors design

One of the critical considerations in the capacitor design is the suppression of the capacitor's voltage ripple. Thus, to suppress the voltage ripple of the capacitor, the minimum capacitance must be calculated. Also, the designing of all capacitors is accomplished by considering the same voltage ripple for them. According to (11), (12) and (18)–(20), the capacitors C_1–C_5 voltages are obtained. As long as the charge produced or absorbed via all capacitors are

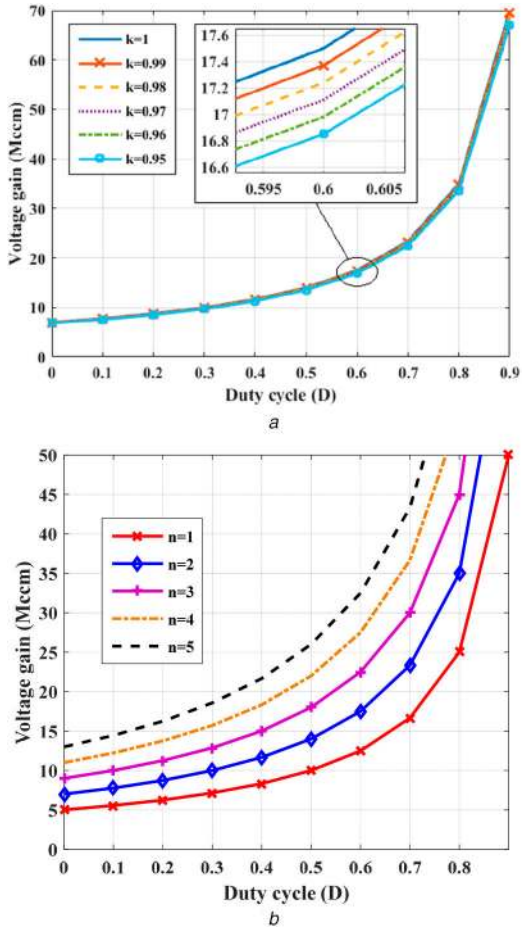

Fig. 5 *Introduced topology voltage gain against duty cycle*
(a) Under several *k*, ***(b)*** Under several CL turn ratios

assumed to be equal, and with regard to $\Delta Q = C\Delta V_C = i_C \Delta T$, the sizes of the capacitors are expressed as follows:

$$C_i \geq \frac{V_O}{\Delta V_{Ci} R_O f_S} \tag{36}$$

$$C_O \geq \frac{DV_O}{\Delta V_{CO} R_O f_S} \tag{37}$$

where $i = 1, 2, 3, 4$, and 5.

A fraction of power will be dissipated with the consideration of the capacitor equivalent series resistance (ESR) when the converter is in operation. It is necessary to note that the ESR of an aluminium electrolytic capacitor will be smaller if it has a great capacitance. Thus, generally, the capacitance should be selected greater than the obtained value. Eventually, the aluminium electrolytic capacitor's values applied in the fabricated archetype convince the equations and conditions as mentioned earlier.

3.4 Input and magnetising inductors design

To verify the performance of the suggested topology for sustainable power resources and, according to high-current ripple detrimental effects from sustainable resources such as short lifetime and high-power losses, it is very good to design the suggested topology in CCM condition with low-input current ripple. So, by considering 20% allowable current ripple, the minimum value of the input inductor, L_{in}, is determined as follows:

$$L_{in} = \frac{V_{in} D}{\Delta I_{in} \cdot f_s} \geq \frac{V_{in} D}{20\% I_{in} \cdot f_s} \tag{38}$$

According to (38), and by considering the implemented prototype specifications, the input inductor must be >166 µH. Therefore, to warranty the CCM operation of the implemented prototype, an input inductor with 320 µH inductance is employed.

The magnetising inductor minimum value should be determined too. To guarantee the converter operation in CCM, the magnetic inductance average current, I_{Lm}, might be more than half of the current ripple of the magnetic inductance, ΔI_{Lm} [39–41]. So, by applying (22) and (24), the L_m minimum value for the proposed topology is achieved as presented below:

$$L_m \geq \frac{D(1-D)^2 R_O}{2 f_s (2n+3)^2} \tag{39}$$

According to (40), L_m should be >15 µH. So, to warranty the implemented prototype CCM operation, a CL that has a magnetising inductance with 100 µH is utilised.

4 Introduced converter efficiency analysis

In practice, the parasitic resistance of the circuit elements causes conduction losses. Thus, the voltage gain and efficiency of the implemented converter is affected by conduction losses. In this section, to analyse the efficiency of the introduced structure, parasitic resistances are presumed and defined as follows: R_{LNs} and R_{LNp} are the secondary and primary sides of the CL ESR, respectively. R_L is the input inductor ESR too. $R_{DS(on)}$ is the main power switch on-state resistance, R_{FD1}–R_{FD4} and R_{FDO} are the diodes D_1–D_4 and D_O forward resistances, respectively, and V_{FD1}-V_{FD4} and V_{FDO} are their threshold voltages. Also, r_{C1}–r_{C5} and r_{CO} are the capacitors C_1–C_5 and C_O ESR, respectively. The power losses of the presented topology can be mainly divided into switch losses, diode losses, capacitors losses, inductor, and coupled inductor losses.

The switch losses consist of conduction loss and turn on and off losses. In the suggested topology, the main switch conduction loss can be achieved as follows:

$$\begin{aligned} P_{R_{DS(on)}} &= R_{DS(on)} \times (I_{rms,S})^2 \\ &= R_{DS(on)} \times \left(\sqrt{D} \left(\frac{(2n)(2-D)+4-D}{D(1-D)} i_O + \frac{DV_{in}}{L_m f_s} \right) \right)^2 \end{aligned} \tag{40}$$

Moreover, the converter switching loss that contains turn on and off losses of the main switch is equal to (41)

$$P_{SW} = \frac{1}{2} f_S I_S V_S (t_{on} + t_{off}) \tag{41}$$

where t_{on} and t_{off} are the switch rise and fall times that are determined via static characteristics of the device provided in datasheet information of the manufacturer, V_S is the maximum voltage stress of the switch, and I_S is the current of the switch during the switching time.

The converter's diodes forward resistance loss can be expressed as follows:

$$\begin{aligned} P_{RF_{(D1-4,O)}} = {} & R_{FD1} \times \left(\frac{\sqrt{D_C}(2n+2) I_O}{(1-D)} \right)^2 \\ & + (R_{FD2} + R_{FD4}) \times \left(\frac{2I_O}{\sqrt{D}} \right)^2 \\ & + (R_{FD3} + R_{FDO}) \times \left(\frac{2I_O}{\sqrt{1-D}} \right)^2 \end{aligned} \tag{42}$$

Also, the diodes forward voltage losses equal to

$$\begin{aligned} P_{VF_{(D1-4,O)}} &= V_{FD1-4,O} \times I_{D1-4,O_{(ave)}} \\ &= I_O (V_{FD1} + V_{FD2} + V_{FD3} + V_{FD4} + V_{FDO}) \end{aligned} \tag{43}$$

The power losses of the capacitors are formulated as

$$P_{r_{C1-5,O}} = r_{C1,2,3,4,5,O} \times \left(I^2_{rms,C1,2,3,4,5,O} \right) \tag{44}$$

The conduction losses of the input inductor can be obtained as follows:

$$P_{R-L} = R_L \times \left(I^2_{rms,L} \right) \tag{45}$$

The conduction losses of the coupled inductor primary, secondary, and tertiary sides can be determined as follows:

$$P_{R-CL} = R_{LNp} \times \left(I^2_{rms,LNp} \right) + R_{LNs} \times \left(I^2_{rms,LNs} \right) \tag{46}$$

The coupled inductor and input inductor core losses can be calculated with the Steinmetz equations and presented as follows:

$$P_{core} = 2K f^{\alpha} (B_{max})^{\beta} A_c l_c \tag{47}$$

where l_c is the core's mean path length, B_{max} is the peak flux density, and A_c is the core cross-sectional area. Generally, values of β, K, and α are given in the manufactures datasheet.

Eventually, the suggested topology theoretical efficiency is formulated as follows:

$$\eta = \left(\frac{P_O}{(P_O + P_{loss})} \right) \times 100 \tag{48}$$

$$\begin{aligned} P_{loss} = {} & P_{R_{DS(on)}} + P_{SW} + P_{RF_{(D1-4,O)}} + P_{VF_{(D1-4,O)}} + P_{r_{C1-4,O}} + P_{R-L} \\ & + P_{R-CL} + P_{core} \end{aligned} \tag{49}$$

Furthermore, the presented topology voltage gain, including the conduction losses, may be achieved as

$$M_{CCM(non-ideal)} = \frac{\eta(2n+3)}{(1-D)} \tag{50}$$

Table 1 Presented DC–DC converter comparison with several other similar converters

References	Component *D C S* CL + *L*	Input current type	C.g	Voltage gain	Voltage stress on main switch	Maximum diode voltage stress
proposed	5 6 1 $1^{2w}+1$	continuous	yes	$\frac{2n+3}{(1-D)}$	$\frac{V_O}{2n+3}$	$\frac{(n+1)V_O}{2n+3}$
[35]	6 6 1 $1^{3w}+0$	discontinuous	yes	$\frac{2+n+n_3(2-D)}{(1-D)}$	$\frac{V_O}{2+n+n_3(2-D)}$	$\frac{(1+n+n_3)V_O}{2+n+n_3(2-D)}$
[36]	5 5 1 $1^{3w}+0$	discontinuous	no	$\frac{3+n+n_3}{(1-D)}$	$\frac{V_O}{3+n+n_3}$	$\frac{(1+n+n_3)V_O}{3+n+n_3}$
[24]	5 5 1 $1^{2w}+0$	discontinuous	yes	$\frac{2+n(2-D)}{(1-D)}$	$\frac{V_O}{2+n(2-D)}$	$\frac{(1+n)V_O}{2+n(2-D)}$
[37]	6 5 2 $2^{3w}+0$	discontinuous	yes	$\frac{2+2n}{(1-D)}$	$\frac{V_O}{2+2n}$	$\frac{(1+2n)V_O}{2+2n}$
[38]	5 5 1 $1^{3w}+0$	discontinuous	yes	$\frac{1+n+n_3D}{(1-D)}$	$\frac{V_O}{1+n+n_3D}$	$\frac{(n)V_O}{1+n+n_3D}$
[29]	8 8 1 $1^{2w}+1$	continuous	yes	$\frac{4+n(2-D)-D}{(1-D)}$	$\frac{V_O}{4+n(2-D)-D}$	$\frac{(n_2(2-D)-D)V_O}{n_2(2-D)-D+4}$
[30]	4 5 1 $1^{2w}+1$	continuous	yes	$\frac{1+n(2-D)+D}{(1-D)}$	$\frac{V_O}{1+n(2-D)+D}$	$\frac{(1+n)V_O}{1+n(2-D)+D}$
[11]	4 5 1 $1^{2w}+1$	continuous	yes	$\frac{2+n+(n+1)D}{(1-D)}$	$\frac{V_O}{2+n+(n+1)D}$	$\frac{(1+n)V_O}{2+n+(n+1)D}$
[31]	4 5 1 $1^{2w}+1$	continuous	yes	$\frac{2+n+D}{(1-D)}$	$\frac{V_O}{2+n+D}$	$\frac{(1+n)V_O}{2+n+D}$
[25, 26]	6 6 1 $1^{2w}+0$	discontinuous	yes	$\frac{1+2n+nD}{(1-D)}$	$\frac{V_O}{1+2n+nD}$	$\frac{(n)V_O}{1+2n+nD}$
[32]	4 5 1 $1^{2w}+1$	continuous	yes	$\frac{1+n+nD}{(1-D)}$	$\frac{V_O}{1+n+nD}$	$\frac{(n)V_O}{1+n+nD}$
[33]	3 4 1 $1^{2w}+1$	continuous	yes	$\frac{2+n}{(1-D)}$	$\frac{V_O}{2+n}$	$\frac{(1+n)V_O}{2+n}$
[34]	4 5 1 $1^{2w}+1$	continuous	yes	$\frac{1+n+(n+1)D}{(1-D)}$	$\frac{V_O}{1+n+(n+1)D}$	$\frac{(1+n)V_O}{1+n+(n+1)D}$

C.g = common grounded; *C* = capacitor; *L* = inductor; *D* = diode; *S* = switch; 3w = 3-winding; 2w = 2-winding; $n_3 = N_{\text{tertiary}}/N_{\text{primary}}$.

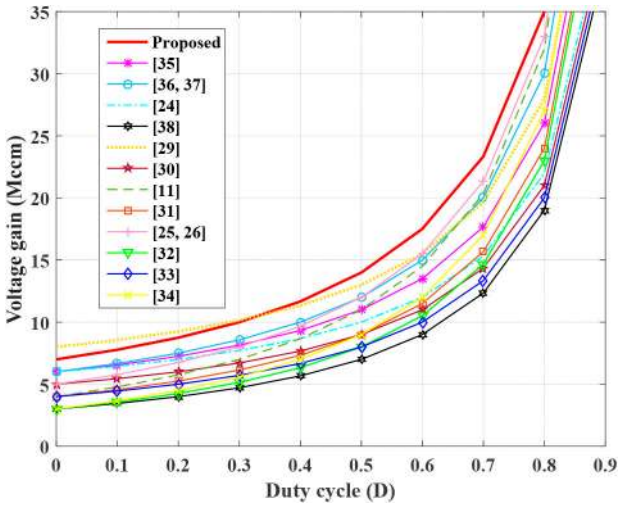

Fig. 6 *Voltage gain comparison of the introduced converter with other most important high-step-up converters*

5 Comparison study

After a full analysis of the proposed topology and to justify the introduced configuration performance and illustrate the superiority of that over other similar developed recently high-boost CL-based DC–DC topologies, some essential comparisons are provided. The proposed configuration has various advantages in comparison with other structures proposed in the latest and most advanced and important papers. The presented topology main features and other alike converters that recently introduced in [11, 24–26, 29–38] are depicted in Table 1. Prior, the presented configuration voltage conversion ratio is depicted and compared with others in Fig. 6. Concerning this figure, the proposed structure voltage gain is higher than the structures proposed in [11, 24–26, 29–38] for all ranges of duty cycle by considering $n = 2$ and $n_3 = 1$. This essential property achieved due to the integration of a VMC network with CL in the structure of the presented topology.

Besides, with regard to Table 1, by considering the voltage gain, although that the suggested configuration component number is equal to the structures proposed in [25, 26, 35], the voltage gain of the proposed configuration is greater than them. Moreover, it is essential to note that the voltage gain of the topologies presented in [11, 37] is lower than the proposed configuration with higher numbers of elements. In addition, the introduced topologies element number presented in [11, 24, 30–34, 36, 38] is lower than the suggested converter. Nevertheless, their voltage gain is remarkably lower than the proposed converter.

Moreover, there is a common ground connection between the input and output of the suggested structure that is a very crucial operator for a front-end boost DC–DC converter of a transformer-less inverter that is connected to the grid.

Another essential advantage of the presented structure that makes it very suitable for clean energy applications is continuous input current property. However, the suggested configurations input currents in [24–26, 35–38] are pulsating and not continuous. In these topologies, the CL appears at the input stage of the structure, and due to this issue, the leakage inductance appears at the input stage too. So, the input current will be discontinuous due to the leakage inductance. Therefore, they are not very appropriate for clean energy systems.

As illustrated in Fig. 7*a*, the normalised voltage stress of the main switching element in the suggested structure is lower than the other converters for every value of *D*. The presented topology distinguishing advantage is steady and reduced voltage stress that does not vary with *D*. This is an essential advantage because a low $R_{DS(on)}$ resistance and voltage rating metal oxide semiconductor field-effect transistor (MOSFET) can be utilised in the fabricated topology to increase the efficiency and decline the cost.

Moreover, Fig. 7*b* shows the high step-up converters normalised maximum diode voltage stress. As depicted in Fig. 7*b*,

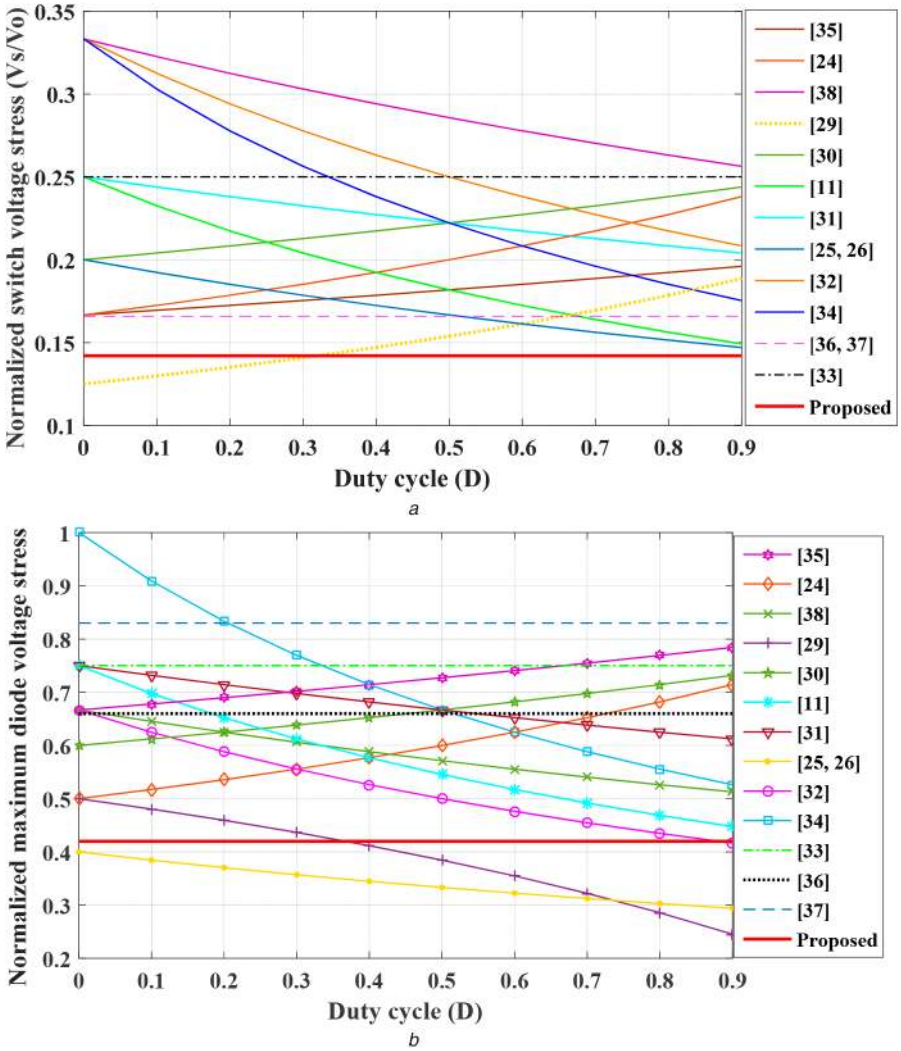

Fig. 7 *Comparison of the introduced topology and other high-step-up topologies*
(a) Normalised voltage stress of the power switch, ***(b)*** Normalised maximum diode voltage stress ($n = 2$, $n_3 = 1$)

the presented converter normalised maximum diode voltage stress is lower than the other converters for every value of D (except for [25, 26, 29]). It is important to note that the converters in [25, 26, 29] have remarkably lower voltage gain and higher switch voltage stress than the suggested converter.

Furthermore, structure extension ability is another advantage of the proposed converter. The voltage gain of the presented topology can be increased more by expanding its configuration without adding extra power switch. It is worth noting that by extending the introduced topology structure, the component count of that will be increased in this state. So, to increase the converter voltage conversion ratio by extending the structure of that a compromise should be considered.

Eventually, with regard to the comparison study section, the introduced topology has a significantly higher voltage conversion ratio over other high step-up topologies because of applying a coupled inductor (CL), and VMC network (C_4, C_5, D_3, and D_4). Owing to an ultra-large voltage gain causes to operate the suggested structure in very appropriate duty cycles. Furthermore, it is illustrated that the introduced topology main switch and output diode normalised voltage stress is lower than the other high step-up topologies. This important property leads to the use of a MOSFET with low-voltage rating and $R_{DS(on)}$ resistance in the suggested structure power circuit to enhance efficiency and decrease the cost. The ripple of the input current of the proposed converter is very low and continuous, which makes it very suitable for renewable energy systems such as photovoltaic systems. Besides, there is a common ground connection between the output and input of the introduced topology, which is an essential property for high step-up DC–DC converters. Utilising many diode components (D_1–D_4 and D_O) in the configuration of the presented topology is its disadvantage. However, the proposed converter has a single-switch (S) that makes the control of the converter very simple. Furthermore, by utilising a passive voltage clamp circuit (C_1 and D_1) in the presented topology circuit, the coupled inductor energy is recycled, and the voltage across the main switching element is decreased.

6 Experimental verification

To clarify the performance of the suggested DC–DC topology and verify the theoretical analysis, a 226 W prototype is designed and fabricated in the laboratory. The photo of the experimental setup of the presented topology is illustrated in Fig. 8.

The main characteristics of the fabricated prototype are presented in Table 2. The presented structure converts 29 V input voltage to 382 V output voltage. The implemented prototype switching frequency is chosen to be 50 kHz. Therefore, the size of passive components is reduced. Ultrafast rectifiers with low forward voltage drop are utilised as power diodes. The main power switch is selected MOSFET IRFP260n with low on-state resistance. The type of coupled inductor core is ferrite EE55/28/21 and the coupled inductor turn ratio is selected as $n = 2$ (15:30).

The proposed topology experimental measurement results in CCM are presented in Fig. 9. The time per division in all of the figures is set to be 10 µs. The output voltage waveform is indicated in Fig. 9*a*. The output voltage is identical to 382 V. In addition, as depicted in Fig. 9*a*, the output voltage ripple with the output capacitor of 220 µF is very low. The power switch S current and voltage are indicated in Fig. 9*b*. It is clear that the power switch

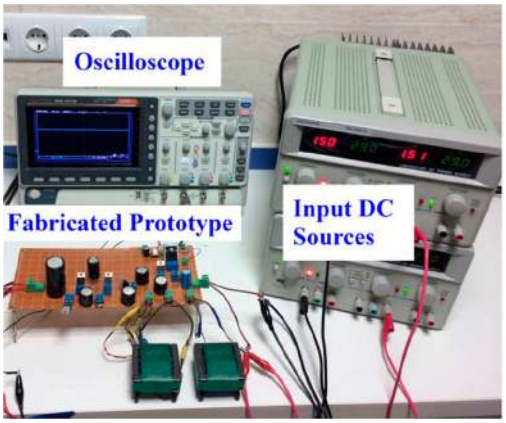

Fig. 8 *Experimental platform of the introduced high-step-up converter*

Table 2 Implemented prototype circuit parameters

Specifications	Values
output voltage	382 V
input voltage	29 V
output power	226 W
switching frequency	50 kHz
input inductor	320 μH
coupled inductor	L_m = 100 μH; L_k = 1.5 μH ferrite core EE-55
turn ratio of the CL (n)	2 (15:30)
capacitors type	electrolytic capacitor
C_1, C_2, C_3, C_4, and C_5	47 μF/ 250 V
C_O	220 μF/ 450 V
power switch, S	IRFP260n
D_1, D_2, D_3, D_4, and D_O	MUR1560

L_m = magnetising inductance; L_k = leakage inductance; n = turn ratio; C = capacitor; S = main power switch; D = diode.

maximum voltage is ∼58 V (about 15% of the output voltage). So, a low $R_{DS(on)}$ resistance switch may be applied. Moreover, according to Fig. 9*b*, as the main power switch turns on, 18 A current flows through the power switch. The capacitors C_1–C_5 voltage waveforms are shown in Figs. 9 *a* and *c*. The voltages across the capacitors C_1, C_2, C_3, C_4, and C_5 are about 59, 28, 110, 168, and 224 V, respectively.

The obtained measured voltages of capacitors are in proper matching with (11), (12), and (18)–(20). The measured input current of the converter that is equal with input inductor current is depicted in Fig. 9*a*. According to this figure, the input current is continuous and has a very low ripple that is very appropriate for sustainable energy resources. Moreover, the leakage inductor current is illustrated in Fig. 9*a*. The obtained waveform is like Fig. 4 that corroborates the theoretical analysis.

Fig. 10 presents the voltage across diodes and currents flow through them. The measured voltage across the diodes D_1, D_2, D_3, and D_O are found to be about 58, 161, 160, and 160 V, respectively. Fig. 10*a* illustrates that the stored energy of the leakage inductance of the CL is recycled to capacitor C_1 through diode D_1 (I_{D1}). The current of diodes D_1, D_2, D_3, and D_O are depicted in Figs. 10*a–d*. The achieved results corroborate theoretical waveforms presented in Fig. 4.

Fig. 11 shows the suggested DC–DC converter measured efficiency for various output powers. The converter maximum efficiency under the 100 W output power is identical to 95%, and for the 226 W output power, the efficiency is identical to 94.4%.

Finally, the analysis and feasibility of the presented topology are confirmed via the experimental measurement results. Various advantages of the introduced DC–DC converter like ultra-high-voltage gain without a large duty cycle, high efficiency, recycled energy of the leakage inductor, and low-voltage stress of switching

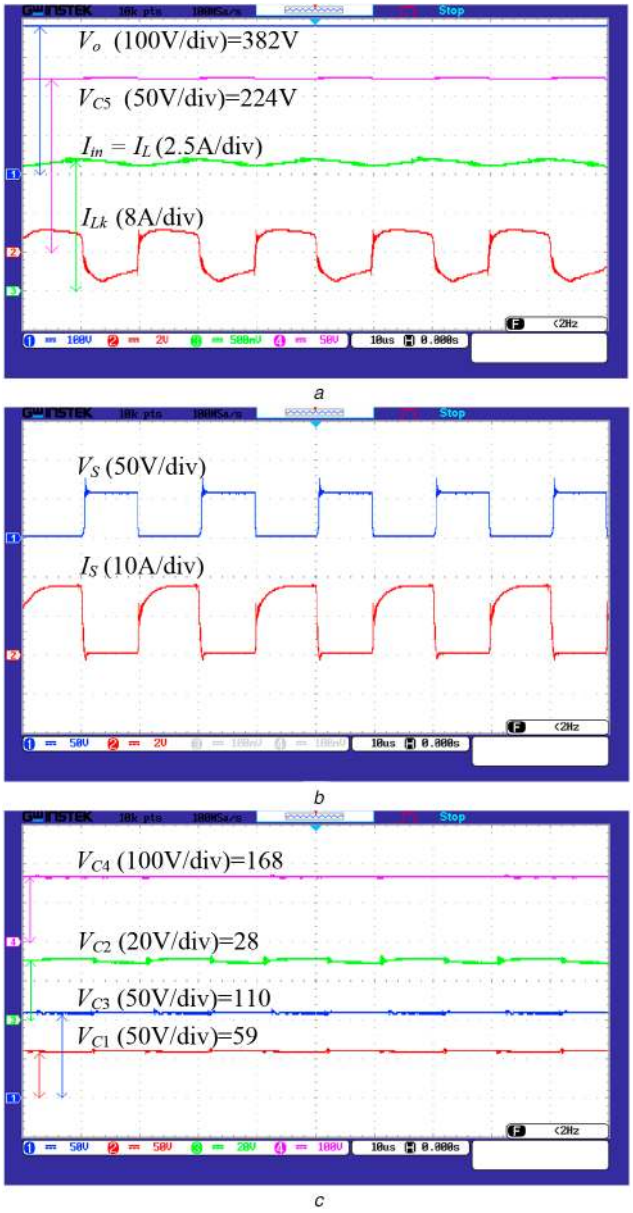

Fig. 9 *Experimental results of the suggested topology*
(a) V_O, V_{in}, V_S, I_S, ***(b)*** V_{C5}, V_{C3}, V_{C2}, V_{C1}, ***(c)*** $I_{in} = I_L$, I_{Lk}, V_{C5}

components make it very suitable for sustainable energy applications such as PV power systems.

7 Conclusion

A high step-up DC–DC converter with an ultra-large voltage conversion ratio is proposed in this paper. In the structure of the proposed converter, a CL with VMC is utilised to obtain a very ultra-high-voltage gain. The suggested structure also benefits from a simpler control scheme and structure due to using a single switch. By utilising a passive clamp circuit in the proposed converter, the voltage stress across the main power switch is decreased, and leakage inductance energy is recycled. Moreover, according to Section 5, the presented structure has a significantly greater voltage conversion ratio over other several high-gain topologies. Having an ultra-high-voltage gain results in operating suggested topology at very appropriate duty cycles. So, the conduction losses of the switching elements are decreased, and the efficiency of the converter is increased. Moreover, operating the converter in low-duty cycles causes to alleviate reverse recovery issue of diodes and having a lower number of turns that makes leakage inductance to be minimal. Furthermore, it is illustrated that the main switch normalised voltage stress and maximum diode voltage stress of the presented structure are lower than the other high-gain topologies.

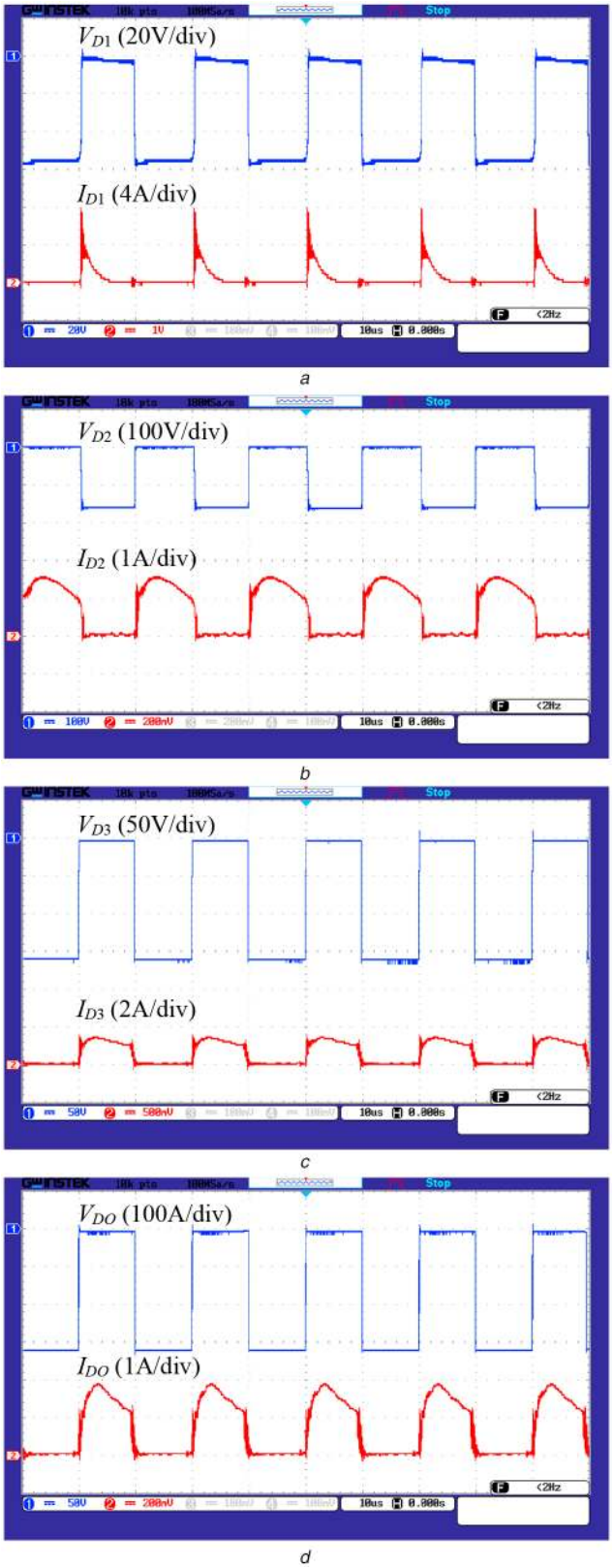

Fig. 10 *Experimental results of the introduced topology*
(a) V_{D1}, I_{D1}, ***(b)*** V_{D2}, I_{D2}, ***(c)*** V_{D3}, I_{D3}, ***(d)*** V_{DO}, I_{DO}

This important property leads to utilising a low $R_{DS(on)}$ resistance power switch in the structure of the presented topology to enhance the efficiency and decline the cost. Furthermore, among the output and input of the presented converter, there is a common ground connection that is attractive merit for a boost DC–DC converter. Also, the extendability of the presented topology causes to achieve high-voltage gains in low-duty cycles. Finally, applying an inductor in the input section of the converter makes the input current ripple very low.

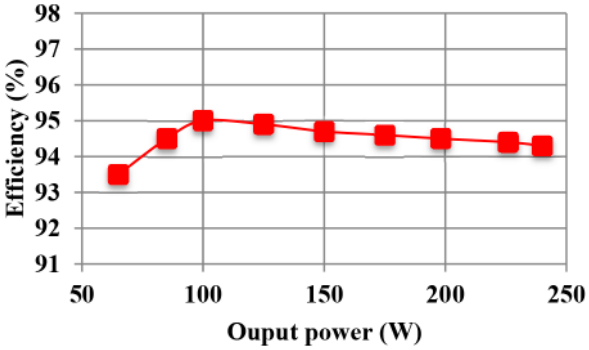

Fig. 11 *Measured efficiency of the suggested structure*

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