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Design and Analysis of Power-Efficient Quasi-Adiabatic Ternary Content Addressable Memory (QATCAM)

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Abstract: Ternary content addressable memory (TCAM) is a high-speed memory employed in network search engines which consume significant power. Many authors have provided efficient power solutions by proposing different match line schemes. This study proposes the use of energy recovering adiabatic logic scheme in the design of power-efficient TCAM. Two different innovative quasi-adiabatic TCAM (QATCAM) core cells are designed. The design is implemented in 180 nm complementary metal-oxide semiconductor technology with a power clock of 1.8 V on Cadence Virtuoso. It is found that the power dissipated by the proposed QATCAM cells is lower than its conventional counterparts. Adiabatic TCAM arrays are designed using adiabatic peripheral circuits. The proposed adiabatic TCAM core cells yield more considerable power savings even at higher frequencies up to 1 GHz.

1 Introduction

Ternary content addressable memory (TCAM) is a type of high-speed memory used in network applications [1–3]. Content addressable memory (CAM) is faster because it allows parallel searching and there are two types of CAMs. They are binary CAM and TCAM. Binary CAM works with 1 and 0s, while TCAM can work with 1s, 0s as well as do not care 'X'. Whenever a do not care value is applied as an input, the appropriate match line (ML) should be enabled irrespective of the stored data. Also, if the stored data is a do not care, the ML should be enabled irrespective of the input data.

Generally, TCAM is a circuit that consumes more power [3, 4]. Various low-power techniques are employed for combating high-power consumption in high-speed TCAM cells. Though many low-power techniques have been proposed to reduce power in ML and search line switching [5–8], the principle of adiabatic logic (AL) works well in the reduction of power dissipation by using the energy recovery process proposed in [9, 10]. The use of AL in the design of binary CAM cells [11–13] has resulted in better power savings. In this paper, the design and implementation of adiabatic TCAM core cells are proposed using efficient charge recovery logic (ECRL) for low-power applications. Sections 2–7 present conventional TCAM designs, various ALs that can be used for power reduction, proposed quasi-adiabatic TCAM (QATCAM) core cells, the proposed adiabatic TCAM array structure along with simulation results, performance improvement in terms of power by using the AL in TCAM, and the conclusion.

2 Background

TCAM is a type of CAM that can have three types of input values for storage and search operations. Therefore, the internal memory cell of TCAM is usually implemented by adding a mask bit ('do not care' bit) to accommodate the third state [4]. TCAM is an integral component in routers to perform match operations. It occupies a larger space in router switches and is also the most expensive component in terms of cost and power consumption [4].

To combat the problem of high-power consumption in TCAM, many authors have made their contributions at the circuit level [5–7, 14–18] and architectural level [7, 19–27]. In this section, a review of different types of TCAM designs is presented.

2.1 Circuit level techniques

Several circuit-level techniques incorporated in the design of low-power TCAMs are briefed in this section. Kostas *et al.* [2] have presented a detailed survey on CAM, which includes the primary TCAM cell with 16 transistors. Arsovski *et al.* have proposed a power-efficient 4 T static storage TCAM with a matching line sense scheme [5], which reduced the density of the TCAM core cell to 12 transistors. Mohan has employed positive-feedback ML sense amplifiers, low-capacitance comparison logic, and low-power ML-segmentation techniques to reduce the ML sensing energy [6]. Huang [14] has described a hybrid type TCAM, which combines the benefits of low-power–low-speed NAND and high-power–high-speed NOR structures and achieves both power and speed efficiency [7, 14]. Though the hybrid type TCAM had the power-delay advantage, it suffers from short circuit current and charge sharing problems. Pai-Sigma ML scheme reduces the compare (search) power of a TCAM by reducing the switching activity of the search lines [7]. This scheme is free of charge sharing and short circuit current issues.

A precharge free CAM has been proposed by Mahendra *et al.* [15], which saves search time and power consumed by the precharge transistor. However, it entails an area overhead. Woo and Yang [16] have proposed an efficient area TCAM which uses do not care diminution scheme. Bypass transistors and decoders are employed to match the mask line. However, it works only up to 330 MHz. Manna and Kanchana Bhaaskaran [17] have proposed an adiabatic static random-access memory in which the power in bit lines, as well as word lines, is recovered; differential cascode, pre-resolved AL are employed in addition to leakage control. The literature surveyed suggests that AL can be the right candidate for energy recovery and reuse at the circuit level for the design of power-efficient TCAM core cell and array.

2.2 Adiabatic logic (AL)

Adiabatic switching is a charge/discharge mechanism that returns accumulated energy to the source using the electric power supply. Dynamic power supply or clocked power plays a significant role in AL because besides being a power supply, it also provides energy recovery [28].

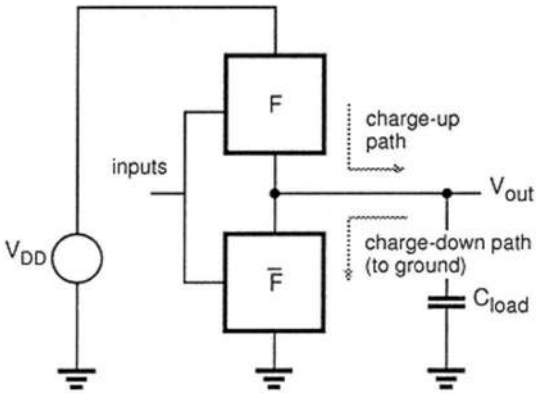

Fig. 1 *Conventional CMOS structure [29]*

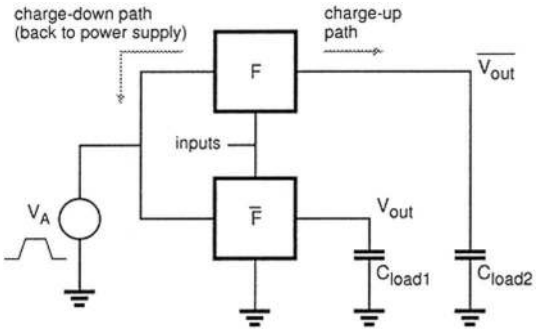

Fig. 2 *AL structure [29]*

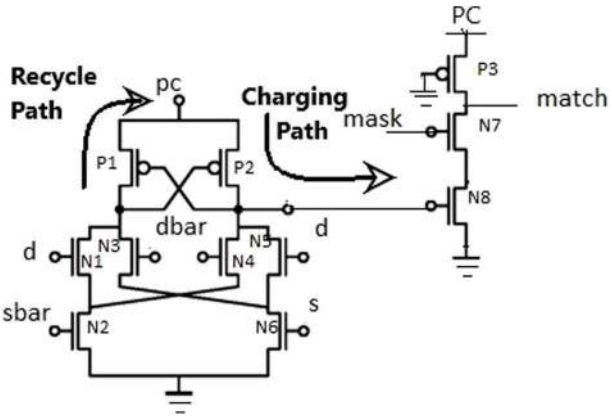

Fig. 3 *Schematic diagram of the QATCAM cell based on ECRL*

Table 1 Write operation in QATCAM

Search line	Data line	Mask line	Data written
0	0	1	0
0	1	1	1
X	X	0	X

The contrast between a traditional complementary metal-oxide semiconductor (CMOS) structure and an AL structure is shown in Figs. 1 and 2, respectively. A traditional CMOS uses a constant voltage supply, whereas, in AL, supply is a power clock. Unlike CMOS, AL recycles dissipated energy and, hence, it works in two phases, namely, a precharge phase and a recovery phase. Most of the adiabatic circuits deliver energy in the precharge phase and recover energy during the recovery phase. This demonstrates that AL can be preferred for low-power solutions [9, 30, 31].

In a static CMOS gate, the energy dissipation of a switching event is expressed as

$$E_{\mathrm{CMOS}} = (1/2)\alpha C V_{\mathrm{DD}}^2 \tag{1}$$

where α is the switching probability, C is the load capacitance, and V_{DD} is the supply voltage. In AL, a voltage ramp is used to charge and recover the energy from the output. A complete cycle consists of charging and recovering. The energy dissipation in AL is expressed as

$$E_{\mathrm{AL}} = 2(RC/T)CV_{\mathrm{DD}}^2 \tag{2}$$

For minimising energy dissipation in AL, R-value in (2) can be reduced. This can be achieved by reducing the size of the transistor and capacitive load, and scaling down supply voltage; alternatively, the circuit speed can be rendered slow. The minimum value of T can be found by comparing (1) and (2)

$$E_{\mathrm{AL}} < E_{\mathrm{CMOS}} \tag{3}$$

Adiabatic circuits have better energy efficiency than the static CMOS circuits, if

$$T > 4RC/\alpha \tag{4}$$

From (4), it is evident that AL can be used for applications with moderate to high switching activities [9]. In this work, it is proposed to use AL for reducing dynamic power dissipation in high-speed TCAM structures.

There are various types of AL design methods, which can be broadly classified as partial AL and fully AL. In partial AL, a part of the charge is allowed to be transferred to the ground. In contrast, in fully AL, all the charges on the load capacitance are recovered by the power supply.

Many authors [9, 11–13, 30] have proved that ECRL is a better adiabatic circuit among the partial AL family because of their simplicity. Thus, the partial AL circuit using ECRL is explored for the analysis and design of QATCAM core cells.

3 Proposed QATCAM core cells

The primary sources of power dissipation in memory are core cell dissipation and peripheral dissipations shown in (5). Peripheral circuitry consists of bit line/search line drivers, address decoders, sense amplifiers, and timing & control circuitry

$$\mathrm{Energy}_{\mathrm{Memory\ array}} = \mathrm{Energy}_{\mathrm{core}} + \mathrm{Energy}_{\mathrm{periphery}} \tag{5}$$

The work presented in this paper aims to reduce the energy dissipation of the core cell by introducing AL in the design of the TCAM core cell. The result is the design of novel adiabatic TCAM core cells exploiting ECRL.

ECRL proposed by Moon and Jeong [32] and Kramer *et al*. [33] for the construction of the XOR-based comparison logic delivers lower energy in comparison with other adiabatic circuits. It is based on cascode voltage switch logic with differential signals, which implement the precharge and evaluation concurrently. This differential structure is constructed with a cross-coupled P-type metal oxide semiconductor (PMOS) pair for latching elements and N-type metal oxide semiconductor (NMOS) transistors for logic blocks.

3.1 QTCAM cell based on ECRL

A QATCAM cell is designed using partial/quasi-AL-ECRL. The schematic diagram of the QATCAM cell is shown in Fig. 3. PMOS pair (P1 and P2) functions as a latch, an NMOS structure (N1–N6) implements compare logic. The output of the compare logic drives transistor N8. An active-low mask is applied through transistor N7. P3 is to precharge the ML. PC is a power clock.

3.1.1 Write operation in QATCAM: To perform a write operation in QATCAM, ML precharge is deactivated, the search line is made low, and the data at the data line is stored at the internal nodes of the latch. To write a do not care, i.e. the ternary state, the mask line is made low, as shown in Table 1.

Table 2 Read operation in QATCAM

Mask line	ML	Read
1	1	0
1	0	1
0	1	x

Table 3 Search operation in QATCAM

Search line	Data line	Mask line	ML
0	0	1	1
0	1	1	0
1	0	1	0
1	1	1	1
X	X	0	1

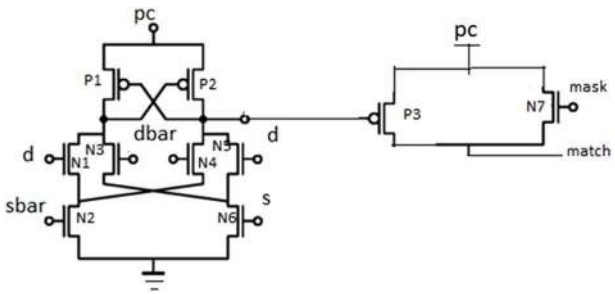

Fig. 4 *Schematic diagram of the QATCAM cell using modified ECRL*

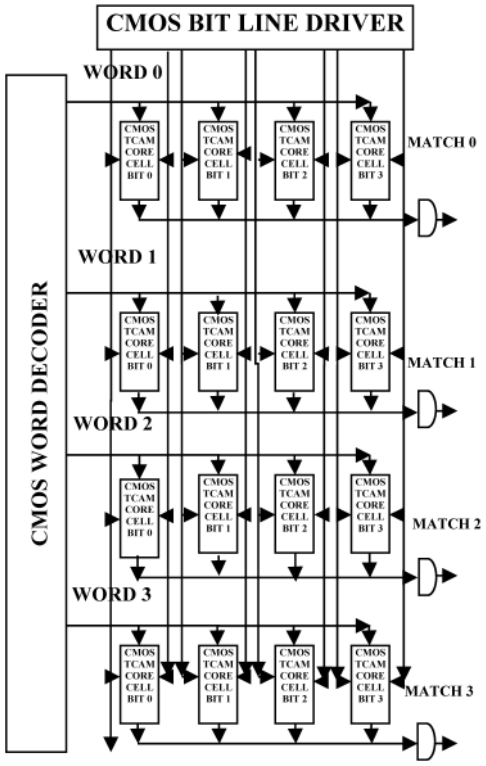

Fig. 5 *TCAM array with conventional TCAM core cells and CMOS peripheral circuits*

3.1.2 Read operation in QATCAM: To perform a read operation in QATCAM, the data stored at the internal node of the latch is read through the ML. If both the ML and the mask line indicate a high and a low, respectively, then it is a do not care state as shown in Table 2.

3.1.3 Search operation in QATCAM: To perform a search operation in QATCAM, the ML precharge is activated. Search data is placed on the search line. If the search data is a do not care, then a 0 is placed on the mask line, and ML is activated as shown in Table 3 in accordance with the status of the mask line and data line

Thus, the designed QATCAM can function effectively to write, to read, and to search for all the three states.

3.2 QATCAM cell based on modified ECRL (MECRL)

Another QATCAM cell based on MECRL is also proposed in this work. This structure is similar to the previous one. However, pass transistor logic is used to apply the mask signal along with the ECRL comparison logic for ML activation.

NMOS and PMOS pass transistors are connected in parallel as shown in Fig. 4. The output of the comparison logic is given as one of the control inputs through the gate of the PMOS transistor (P3), and the mask signal is applied through the gate of the NMOS transistor (N7). PC represents the power clock.

4 Proposed adiabatic TCAM array

According to (5), energy dissipated in a memory array is significantly influenced by the energy dissipated in the peripheral circuits. This work aims to minimise the energy dissipated in the memory by introducing the AL in the bit/search line drivers and the word line drivers. Initially, a 4×4 TCAM array is designed by using a conventional 12 transistor TCAM core cell and CMOS peripheral circuits, as shown in Fig. 5. Since AL results in area overhead for the energy recovery logic, high density-low power 12 transistor TCAM core cell proposed by Igor is chosen as the reference. Adiabatic TCAM array is designed by using a conventional TCAM core cell and adiabatic peripheral circuits. ECRL is employed for the design of the peripheral circuits as shown in Fig. 6. Finally, a complete adiabatic TCAM array is designed using the proposed adiabatic ECRL TCAM core cells and ECRL peripheral circuits as shown in Fig. 7.

The proposed adiabatic TCAM array designs are listed in Table 4.

5 Simulation results

The simulation results of the proposed adiabatic TCAM core cells and adiabatic TCAM array are presented in this section.

5.1 Simulation result of QATCAM cell based on ECRL

The output of the QATCAM cell based on ECRL is shown in Figs. 8 and 9.

To test the match condition, the same data is applied to the data line and search line as depicted in Fig. 8. It is found that the output ML remains high irrespective of the status of the mask line. To test the mismatch condition, different data are applied to the data line and the search line, as shown in Fig. 9. Since an active low-mask line is used in the design, it is found that when the mask line is held high, the ML is pulled down to indicate the mismatch condition. When the mask line is made low, the ML is held high. A trapezoidal signal with a peak voltage of 1.8 V is used as the power clock for the analysis of adiabatic TCAM cell at a frequency of 1 GHz.

5.2 Simulation result of QATCAM cell based on modified ECRL

The match output of the QATCAM cell using modified ECRL is shown in Fig. 10, which is the same as that of the QATCAM using ECRL.

The mismatch output of the QATCAM cell using modified ECRL is shown in Fig. 11.

To test the match condition, the same data is applied to the data line and the search line. It is found that the output ML remains high irrespective of the status of the mask line. To test the mismatch condition, different data are applied to data and search lines, as shown in Fig. 11. Since an active high mask line is used in the design, it is found that when the mask line is held high, the ML is pulled up to indicate the match condition irrespective of the data and search line status. When the mask line is made low, the ML is

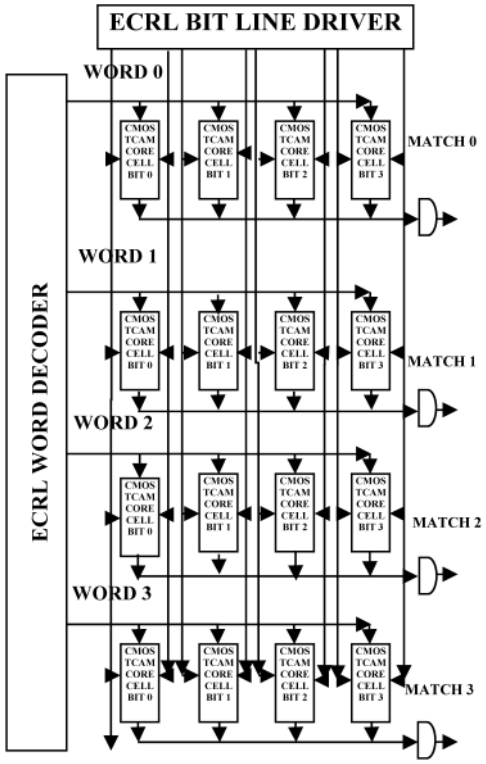

Fig. 6 *TCAM array with conventional TCAM core cells and ECRL (adiabatic) peripheral circuits*

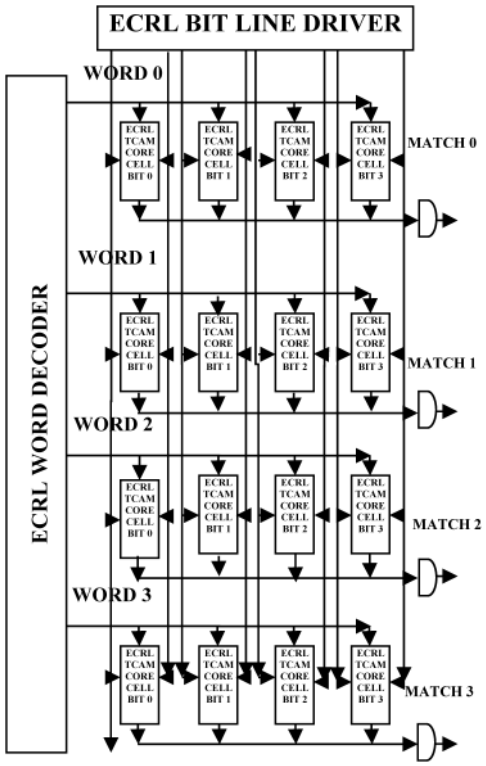

Fig. 7 *TCAM array with the proposed ECRL (adiabatic) TCAM core cells and ECRL (adiabatic) peripheral circuits*

Table 4 Proposed adiabatic TCAM array designs

S.No	TCAM core cell	Peripheral circuit
proposed adiabatic TCAM array 1 (Fig. 6)	conventional 12 T Cell	adiabatic-ECRL
proposed adiabatic TCAM array 2 (Fig. 7)	adiabatic TCAM cell	adiabatic-ECRL

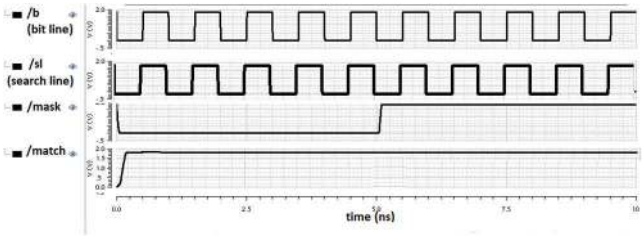

Fig. 8 *Match output of the QATCAM cell based on ECRL*

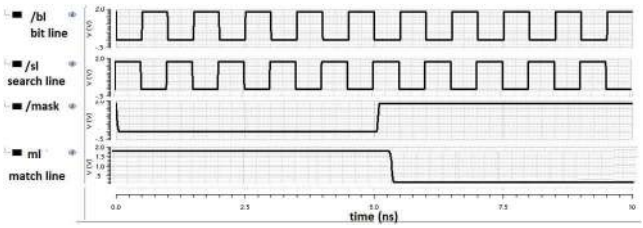

Fig. 9 *Mismatch output of the QATCAM cell based on ECRL*

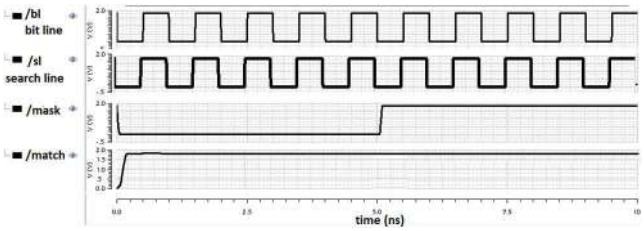

Fig. 10 *Match output of the QATCAM cell based on modified ECRL*

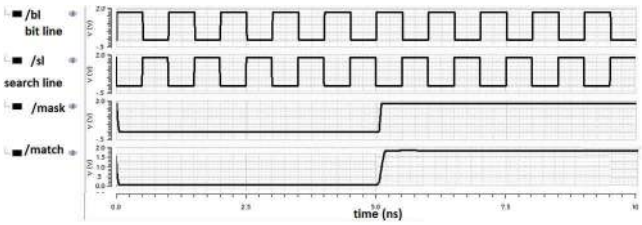

Fig. 11 *Mismatch output of the QATCAM cell based on modified ECRL*

pulled down to indicate the mismatch condition. A trapezoidal signal with a peak voltage of 1.8 V is used as a power clock for the analysis of QATCAM cells using modified ECRL at a frequency of 1 GHz.

5.3 Simulation result of adiabatic TCAM array

The proposed adiabatic TCAM arrays are simulated using Cadence Virtuoso at 180 nm with a peak voltage of 1.8 V. Wide and array logic is used for driving the ML in every row for simplicity.

6 Performance analysis of the proposed adiabatic TCAM structures

The performance of TCAM is usually measured in terms of its speed (data search delay) [34], the power consumed, area, and energy delay product (EDP). In this section, the performance analysis of the proposed adiabatic TCAM structures is carried out, and a comparison with its conventional counterpart is presented.

The measured power and calculated energy consumption of the proposed QATCAM cell, along with the conventional TCAM cell are listed in Table 5. It is found that the matching energy and mismatch energy of the QATCAM using MECRL results in more significant savings. Also, it is found that QATCAM based on ECRL has better savings in match energy, whereas QATCAM based on modified ECRL has optimum power saving in both match and mismatch conditions. In the design of QATCAM based on MECRL, the usage of pass transistor logic to drive the ML has

Table 5 Energy consumption of the proposed QATCAM cell

Types of TCAM cells	Measured power in watts		Energy consumption in joules/bit/search	
	Match power	Mismatch power	Match energy	Mismatch energy
conventional TCAM [5]	495.4μ	120.4μ	3.96p	0.963p
proposed QATCAM-ECRL	338.5p	166.47μ	2.71a	1.332p
proposed QATCAM-MECRL	13.01n	16.75n	0.11f	0.134f

Table 6 Performance analysis of the proposed adiabatic TCAM along with the existing TCAM core cells

Parameters for evaluation	TCAM with 4 T static CAM storage [5]	DPS TCAM [14]	16 transistor-NAND TCAM [2]	16 transistor-NOR TCAM [2]	Proposed QATCAM based on ECRL	Proposed QATCAM based on modified ECRL
energy/bit/search, J	0.9632 pJ	2.0664 pJ	2.578 pJ	1.378 pJ	2.708 aJ–1.3317 pJ	0.104–0.134 fJ
delay, s	0.256 ns	0.2 ns	0.643 ns	0.254 ns	0.2303 ns	0.23 ns
area (no of transistors)	12	9	8	10	11	10
EDP	0.2466×10^{-21}	0.41328×10^{-21}	1.6577×10^{-21}	0.349×10^{-21}	0.624×10^{-27}–0.307×10^{-21}	0.024×10^{-24}–0.031×10^{-24}

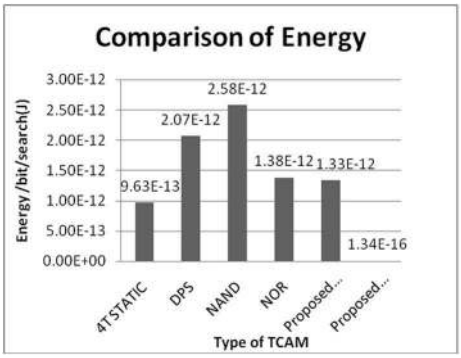

Fig. 12 *Comparison of energy of the proposed TCAM along with its conventional counterparts*

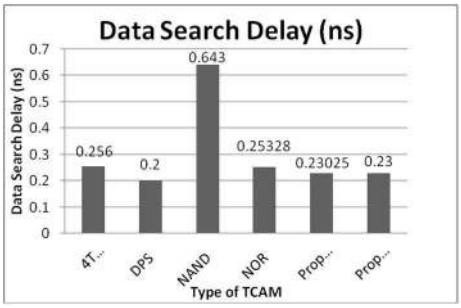

Fig. 13 *Comparison of data search delay of the proposed TCAM along with its conventional counterparts*

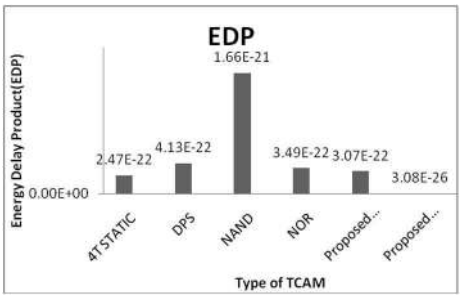

Fig. 14 *Comparison of EDP of the proposed TCAM along with its conventional counterparts*

resulted in maximum swing voltage and good energy recycling, which has led to better energy saving.

To perform a comparative analysis of the proposed TCAM with the existing TCAM, standard TCAM core cells at the circuit level found in the literature [2, 5, 14] are simulated under the same design environment.

Performance analysis in terms of energy/bit/search, delay, area, EDP of the proposed QATCAM made with the existing TCAM structures found in various literature and listed, as shown in Table 6.

From Table 6, it is found that the match energy of the proposed QATCAM based on ECRL is the least among the techniques published in the literature.

However, the mismatch energy of the proposed technique is high. A comparison of the energy/bit/search is depicted in Fig. 12, which shows that proposed QATCAM using modified ECRL can recycle energy and save power.

A comparison of the data search delay is shown in Fig. 13. Dynamic power source (DPS) TCAM [14] has the least delay, followed by the proposed QATCAM core cells. Results demonstrate that the proposed designs can maintain speed-power trade-off.

A comparison of the EDP is depicted in Fig. 14, which proves that the proposed QATCAM using modified ECRL has the least EDP followed by 4 T static storage TCAM. Also, the proposed QATCAM can function effectively up to 1 GHz, consuming almost the same power as shown in Fig. 15.

Performance analysis of the proposed adiabatic TCAM array is made with the existing TCAM structures found in various literature and listed, as shown in Table 7.

Measured power and delay are listed for the different combinations of AL along with the calculated values of energy per bit per search and EDP.

From Table 7, it is found that the proposed adiabatic TCAM array based on ECRL has the least EDP among the tested structures.

7 Conclusion and future work

In this paper, novel QATCAM core cells and adiabatic TCAM array structures are proposed and implemented. The usage of AL has resulted in better power savings compared to the existing techniques. The proposed adiabatic TCAM is designed and simulated using Cadence Virtuoso at 180 nm technology. Power and delay analysis of these cells and arrays is carried out and compared with conventional TCAM cells and structures. Simulation results of the proposed QATCAM cell prove that AL in TCAM is capable of lowering its power requirements to a greater extent. The QATCAMs are highly promising in power saving in the implementation of database accelerators, graphics processing units, and deep learning/machine learning servers used in big-data engineering. Also, AL can work well for a broader range up to 1 GHz. TCAM designs based on emerging technologies [35–38] can also adopt this AL. This design can be further enhanced by the use of specialised power clock generators [39, 40]. However, the

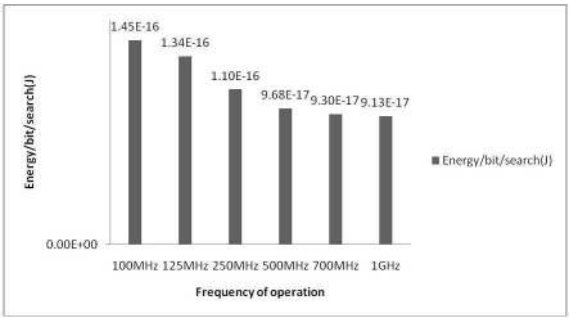

Fig. 15 *Performance analysis of QATCAM cell based on MECRL at different frequencies*

Table 7 Performance analysis of the proposed adiabatic TCAM array along with the existing TCAM structures

Proposed TCAM array types	Power, W	Delay, s	Energy/bit/search, J	EDP, J-s
conventional TCAM array 1 core TCAM cell – CMOS; peripheral – CMOS	9.176m	127.48p	4.588p	$584.87824 \times 10^{-24}$
array 2 core TCAM cell – CMOS; peripheral – ECRL	8.065m	177.54p	4.033p	$715.93005 \times 10^{-24}$
array 3 core TCAM cell – MECRL; peripheral – CMOS	1.511m	161.12p	0.756p	$121.72616 \times 10^{-24}$
array 4 core TCAM cell – MECRL; peripheral – ECRL	63.98µ	200.14p	31.99f	$6.4024786 \times 10^{-24}$

challenge is to design an optimised power clock generator. Further improvement in power saving can be achieved by using power efficient ML sensing schemes. Multi-V_{DD} logic [41] can also be employed between the periphery and the core of the memory array.

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