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Design of a new BUS for low power reversible computation

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ABSTRACT

Optimization of device power can be achieved using reversible logic computation and this technique can be applied to a variety of low power applications such as optical computing, nanotechnology, Complementary Metal Oxide Semiconductor (CMOS), Very Large-Scale Integrated Circuits (VLSI) design and many more. Basic and universal gates are the elementary building blocks of digital system. In this paper, a new reversible Basic, Universal and Special (BUS) gate is proposed that is available as a single gate with multiple functionalities as basic (AND, OR & NOT), universal (NAND & NOR) and special gate (EXOR). The proposed BUS gate is implemented on Field Programmable Gate Array (FPGA) and simulated using 180 nm and 90 nm CMOS process technologies. Manchester adder and C17 circuit of ISCAS'85 (International Symposium on Circuits and Systems-1985) benchmark suite using BUS gate are designed and verified using Electronic Design Automation (EDA) tools. There is a power reduction of about 64.41% and 14.06% at 180 nm and 90 nm CMOS process technologies respectively in reversible BUS gate as compared to conventional CMOS-based designs. Thus, this paper provides a threshold to build more complex arithmetic systems using reversible logic, thus increasing the performance of computing systems with low power dissipation.

1. Introduction

Major thrust is being given in research domain to the design, implementation, and analysis of logic circuits that are reversible. The idea of reversible logic is increasingly employed in the areas of nanotechnology, quantum computing, low power VLSI design, and optical computing. As the complexity in CMOS VLSI circuits increases, the dissipation of power in the circuit becomes a major challenge in the design. Due to loss of the information, there will be dissipation of energy and consumption of power in irreversible logic circuits. It was demonstrated by Landauer [1] that heat energy of kT*log2 joules is dissipated for every bit of information lost, where the absolute temperature is represented by T (Kelvin) and k is the Boltzmann's constant respectively. It was shown in [2] that power dissipated in logic circuits comprising of reversible logic gates is zero. Reversible logic is widely used in the field of quantum computing and all the quantum gate are reversible [3]. A system with reversible computation is possible only when it is built using reversible gates.

The primary requirement for an 'n' input, 'k' output logic network to be reversible is that the values of 'n' and 'k' must be equal. Each output has a one to one mapping with corresponding input and both can be uniquely derived from each other. To make number of inputs equal to outputs, additional inputs and outputs could be added, so that the logic circuit would function as a reversible logic

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Table 1
Preview of available reversible logic gates.

Reversible Gate	Gate Size	Input/output Definition	Functionality	Description	QC
Feynman [7] (FG)	2 × 2	$Iv = (A, B)$ $Ov = P, Q: P = A$ $Q = A \oplus B$	EXOR, Buffer Controlled NOT gate (CNOT)	Control input X is high, the output is complement of Y, else it acts as buffer	1
Toffoli [8] (TG)	3 × 3	$Iv = (A, B, C)$ $Ov = P, Q, R: P = A$ $Q = B, R = AB \oplus C$	Controlled- Controlled NOT gate (C^2NOT)	Inputs X & Y are high, then 3rd output is negation of input Z, remaining output terminals act as buffer.	5
Fredkin [9] (FRG)	3 × 3	$Iv = A, B, C,$ $Ov = P, Q, R: P = A$ $Q = \overline{A}B + AC$ $R = AB + \overline{A}C$	Controlled Swap gate	Outputs M & N are swapped values of inputs Y & Z when X is high	5
Peres [10] (PG)	3 × 3	$Iv = (A, B, C)$ $Ov = P, Q, R: P = A$ $Q = A \oplus B, R = AB \oplus C$	CNOT, C^2NOT, copying gate	When input X is high, output J is negation of Y. When both X & Y are high, output K will be negation of input Z	4
BVF [11]	4 × 4	$Iv = (A, B, C)$ $Ov = P, Q, R, S: P = A$ $Q = A \oplus B, R = C$ $S = C \oplus D$	Copying gate	If B & D are high, output terminals act as buffer	2
DPG [11]	4 × 4	$Iv = (A, B, C, D)$ $Ov = P, Q, R, S: P = A$ $Q = A \oplus B$ $R = A \oplus B \oplus D$ $S = (A \oplus B)D \oplus AB \oplus C$	Full adder	If $C = 0$, D=Cin, full adder output is obtained	6
TRG [12]	3 × 3	$Iv = (A, B, C)$ $Ov = P, Q, R: P = A$ $Q = A \oplus B, R = A\overline{B} \oplus C$	EXOR, NOT	If $B = 0$, P & $Q = A$, $R = A$ exor C, If $B = 1$, Q=complement of A, $R = C$	6
PFAG [13]	4 × 4	$Iv = (A, B, C, D)$ $Ov = P, Q, R, S: P = A$ $Q = A \oplus B,$ $R = A \oplus B \oplus C$ $S = (A \oplus B)C \oplus AB \oplus D$	full adder	If $D = 0$, R & S are sum and carry out for inputs A, B & C	8
HNG [14]	4 × 4	$Iv = (A, B, C, D)$ $Ov = P, Q, R, S: P = A$ $Q = B, R = A \oplus B \oplus C$ $S = (A \oplus B)C \oplus AB \oplus D$	full adder	If $D = 0$, R & S are sum and carry out for inputs A, B & C	6
OTG [14]	4 × 4	$Iv = (A, B, C, D)$ $Ov = P, Q, R, S: P = A$ $Q = A \oplus B, R = A \oplus B \oplus D$ $S = (A \oplus B)D \oplus AB \oplus C$	full adder	If $C = 0$, R & S are sum and carry out for inputs A, B & D	9
TSG [14]	4 × 4	$Iv = (A, B, C, D)$ $Ov = P, Q, R, S: P = A$ $Q = \overline{AC} \oplus \overline{B}$ $R = (\overline{AC} \oplus \overline{B}) \oplus D$ $S = (\overline{AC} \oplus \overline{B})D \oplus (AB \oplus C)$	NOT, EXOR, full adder	If $B = 1$, Q= complement of A; if $C = 0$, Q= EXOR of A & B; If $B = 0$, Q=NOR of A & C	17
R GATE [14]	3 × 3	$Iv = (A, B, C)$ $Ov = P, Q, R: P = A \oplus B$ $Q = A, R = AB \oplus \overline{C}$	Copy, AND, NAND, NOR	If $B = 0$, $P = Q = A$; If $C = 0$, R=AB; If $C = 1$, R=complement of AB;	5
M GATE [15]	3 × 3	$Iv = (X, Y, Z)$ $Ov = I, J, K: I = X$ $J = \overline{X \oplus Y}, K = X\overline{Y} \oplus Z$	EXNOR	J=EXNOR of X & Y	5
L GATE [15]	3 × 3	$Iv = (X, Y, Z)$ $Ov = I, J, K: I = X$ $J = Y, K = \overline{X \oplus Y} \oplus Z$	EXOR, EXNOR	If $Z = 0$, EXNOR of X & Y; If $Z = 1$, EXOR of X & Y	Not applicable
TS-3 [16]	3 × 3	$Iv = (X, Y, Z)$ $Ov = I, J, K: I = X$ $J = Y, K = X \oplus Y \oplus Z$	EXOR, EXNOR	If $Z = 0$, EXOR of X & Y; If $Z = 1$, EXNOR of X & Y	2
DG [17]	3 × 3	$Iv = (X, Y, Z)$ $Ov = I, J, K: I = X$ $J = \overline{X \oplus Y}, K = X\overline{Y} \oplus Z$	EXNOR	J=EXNOR of X & Y	5
MRG [18]	4 × 4	$Iv = (W, X, Y, Z)$ $Ov = D, E, F, G: D = W$ $E = W \oplus X, F = W \oplus X \oplus Y$ $G = (WX \oplus Z) \oplus (W \oplus X) \oplus Y$	OR, NOR, EXOR, EXNOR	Control inputs= C, D and outputs taken at R & S	6
DKG [19]	4 × 4		Full adder/ subtractor		17

(*continued on next page*)

Table 1 (*continued*)

Reversible Gate	Gate Size	Input/output Definition	Functionality	Description	QC
		$Iv = (A, B, C, D)$ $Ov = P, Q, R, S: P = B$ $Q = \overline{A}C + A\overline{D}$ $S = B \oplus C \oplus D$ $R = (A \oplus B)(C \oplus D) \oplus CD$		Functions as full adder/full subtractor with A as control input	
SRK [20]	3 × 3	$Iv = A, B, C,$ $Ov = P, Q, R: P = A$ $Q = A \oplus B \oplus C$ $R = \overline{A}C \oplus AB$	2:1 Multiplexer	If $A = 0$, C input is selected, $A = 1$, B input is selected	4
DKGP [21]	4 × 4	$Iv = (D, E, F, G)$ $Ov = W, X, Y, Z: W = D \oplus F$ $X = E, Y = E \oplus F \oplus G$ $Z = D \oplus (D \oplus F)(D \oplus G) \oplus E(F \oplus G)$	Full adder/ subtractor	Functions as full adder/full subtractor with D as control input	15
SV [22]	2 × 2	$Iv = (A, B)$ $Ov = P, Q: P = A$ $Q = \overline{A \oplus B}$	EXNOR gate	Q gives EXNOR gate output	2
SMG [23]	4 × 4	$Iv = (A, B, C, D)$ $Ov = P, Q, R, S: P = A$ $Q = A \oplus B \oplus D, R = A \oplus B$ $S = (A \oplus B)D \oplus AB \oplus C$	Full adder	$C = 0$ produces full adder outputs	
ALL GATE [24]	4 × 4	$Iv = (A, B, C, D)$ $Ov = P, Q, R, S: P = A$ $Q = AB \oplus C$ $R = (A + B) \oplus B$ $S = (A \oplus B) \oplus D$	Basic & Universal gates	C, B & D act as control inputs to give AND, NAND OR, NOR & EXOR, EXNOR gate outputs respectively	

circuit. Constant Inputs (CI) are the additional inputs added to fulfil this requirement. Similarly, the additional outputs added to make the circuit reversible and not used further in the computation are called the Garbage Outputs (GO). Quantum Cost (QC) of a reversible circuit is referred to the cost of the circuit in terms of the quantity of 1 × 1 and 2 × 2 primitive gates used to realize the circuit. While designing a reversible logic circuit, fan-out and feedback are not permitted [4–6]. CI, GO and QC are the important parameters that need to be minimized for the design of an efficient reversible circuit. Hardware complexity of the reversible logic gates is defined in terms of number of EXOR, AND & NOT gates used to design the circuit. A few of the numerous reversible gates that are available in literature are highlighted in this section with respect to input & output vectors and quantum cost (Table 1).

Reversible basic and universal gate designs using proposed BUS gate is compared to other reversible basic and universal gate designs in this paper that can further be used in any digital circuits. Reversible basic and universal gates are the elementary building blocks in arithmetic circuits. In Section 2, materials and methods are reviewed, which include discussion about the design of proposed BUS gate and concepts of quantum circuit. Results are discussed in the next section. In Section 3, the performance of the BUS gate is evaluated at the gate level and transistor level using CMOS process technologies. Power dissipation and delay of the benchmark circuit implemented using the proposed gate and conventional CMOS circuit design are compared. Additionally, a 4-bit Manchester Adder is designed using the proposed BUS gate and its performance is analysed. This is followed by conclusion in Section 4.

2. Materials and methods

2.1. Preview of basic, universal and special gates

Boolean functions describe the logic operations performed on one or more binary inputs. These are implemented using physical devices called logic gates, that are classified as basic and universal gates. AND, OR, and NOT gates are called the basic gates. NAND and NOR gates are called universal gates, because any other gate can be realized using these gates. NAND and NOR gates are economical and easier to fabricate, hence they are advantageous. EXOR and EXNOR gates are known as special gates. These logic gates are used in arithmetic and encryption circuits, error detecting circuits, which are implemented to detect odd parity or even parity bits in digital data transmission circuits.

All the digital circuits are designed using basic gates or universal gates. Combinational logic circuits such as adders, subtractors, multiplexers, demultiplexers, encoders, decoders, etc. and sequential circuits such as registers, counters, arithmetic logic units (ALUs), computer memory and other more complex digital circuits are designed using logic gates.

If a reversible gate, that functions as basic, universal and special gate, is designed, then any digital circuit can be constructed using the same. This reduces the usage of higher number of gates, thus further reducing power dissipation of the circuit.

There are only 3 reversible gates available in literature that can perform the operations of basic gates (AND, OR, NOT), universal gates (NAND, NOR) and special gates (EXOR) similar to proposed gate, but with different control inputs and garbage outputs. This

means, the outputs of all basic, universal or special gates cannot be generated simultaneously with a single control signal. The available gates that function as basic, universal and special gates are DPG gate [11], SMG gate [23], and 'ALL GATE' [24].

SMG [23] and DPG [11] gates can be used to realize the outputs of basic, universal, and special gates, but with two control signals. Output of NOT gate can be obtained using these gates with 3 control signals. Two constant inputs are required to realize the basic, universal and special gates using SMG or DPG gate and, in this process, 2 garbage outputs are produced that are useless.

ALL GATE [24] is used to realize basic, universal and special gate outputs using two different control signals. Two constant inputs are required, and one garbage output is generated while realizing the basic, universal and special gates. NOT gate output is produced using 3 control inputs.

Proposed BUS gate is used to realize same results using two control signals. However, only one constant input is used to produce the required outputs (either A, B or C inputs depending on the operation performed) and produces only one garbage output. The proposed BUS gate provides a threshold to build more complex arithmetic systems using reversible logic, thus increasing the performance of computing systems with low power dissipation.

2.2. Proposed reversible BUS gate

A 3 × 3 reversible BUS gate is proposed that can work as a reversible basic, universal or a special gate. It has three inputs A, B & C and produces three outputs P, Q and R. One of the inputs acts as a control input and the proposed gate performs the operation of a two-input basic, universal or special gate. The block diagram of BUS gate is shown in Fig. 1.

2.3. Principle of operation

The proposed 3 × 3 reversible BUS gate produces outputs of a 'two-input AND gate and OR gate' when input C= '0'. NAND gate and NOR gate outputs are produced when input C= '1'. Thus, reversible BUS gate acts as basic or universal gate depending on the input given to control input C. Quantum circuit is designed as shown in Fig. 2. The circuit consists of 3 positive-controlled Toffoli or C^2NOT gates (TG) and 5 Feynman or CNOT (FG) gates. Quantum cost of CNOT and C^2NOT gate, obtained from their quantum circuits are 1 and 5 respectively as indicated in Fig. 3. So, the quantum cost of reversible BUS gate is calculated directly as 20.

The reversible BUS gate can be used as AND, OR, NAND, NOR, Copy, EXOR, and NOT gates. One constant input is used to control the functionality of the gate and a maximum of two garbage outputs is produced. Table 2 gives the detailed operation of reversible BUS gate.

2.4. Quantum circuit

Quantum gates [3] are reversible and encode information in terms of qubits (two-level quantum system) rather than normal logic values. A two-dimensional complex Hilbert space describes the qubit. The values 0 and 1 are represented using two orthogonal quantum states. For two pure logic states, the state of a qubit can be expressed as $|\Psi\rangle = \alpha|0\rangle + \beta|1\rangle$ (called superposition), where α and β are complex numbers so that$|\alpha|^2 + |\beta|^2 = 1$.

A specific $2^n x 2^n$ unitary operation can be performed on selected n qubits by an n-qubit quantum gate in a specific period of time. A matrix U is unitary if UU+ = I where U+ is the conjugate transpose of U and I is the identity matrix.

Any reversible gate can be decomposed into a quantum circuit composed of a sequence of elementary quantum gates (Fig. 4) defined as follows:

- NOT gate: The input p is mapped on to the output p ⊕ 1 in NOT gate, where EXOR operation is represented by the symbol ⊕ and the input qubit value is inverted at the output.
- CNOT gate: The Controlled-NOT (CNOT) gate maps two inputs (p, q) to corresponding two outputs (p, q⊕ p), where p is the control input and q is the target input. The target qubit value is inverted at the output by CNOT gate (Feynman gate) if and only if the control qubit value is 1.
- SWAP gate: The SWAP gate maps two inputs (p, q) to corresponding two outputs (q, p). A SWAP gate exchanges the two qubit values at the output.
- Controlled-V gate performs the V operation known as the square root of NOT, since two consecutive V operations are equivalent to an inversion. Controlled-V gate depends on the value on its control line and changes the value on the target line using the transformation given by the matrix.

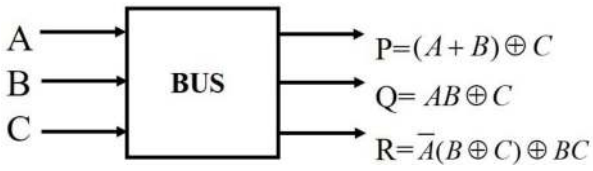

Fig. 1. Reversible BUS gate.

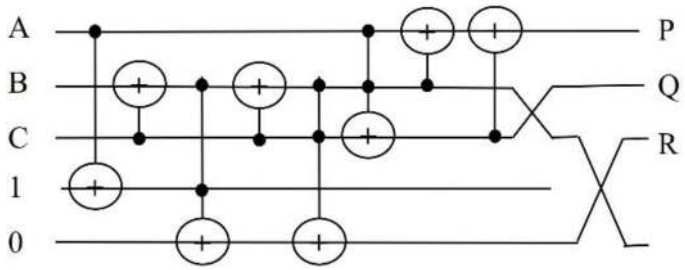

Fig. 2. Quantum circuit of BUS gate.

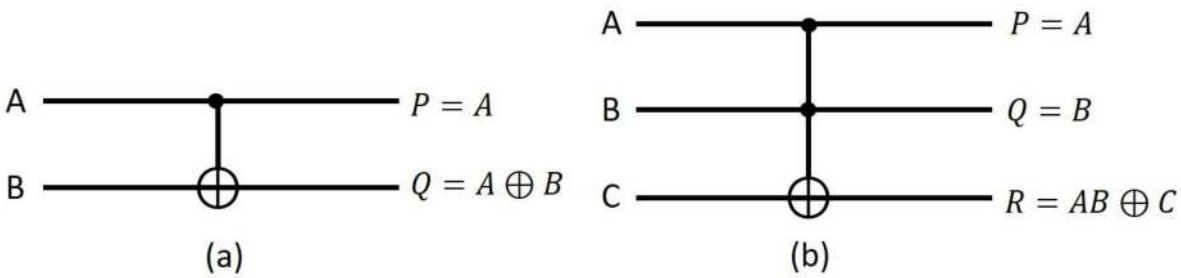

Fig. 3. Quantum circuit of (a) CNOT or FG gate (b) C^2NOT or TG gate.

Table 2
Operation of reversible BUS gate.

A	B	C	Function
0/1	0/1	0	OR (A+B), AND (AB)
0/1	0/1	1	NOR, NAND
0	0/1	0/1	EXOR, COPY (C), OR (B+C)
1	0/1	0/1	NOT, EXOR, AND
0/1	0	0/1	EXOR, COPY (C)
0/1	1	0/1	EXOR (A exor C)

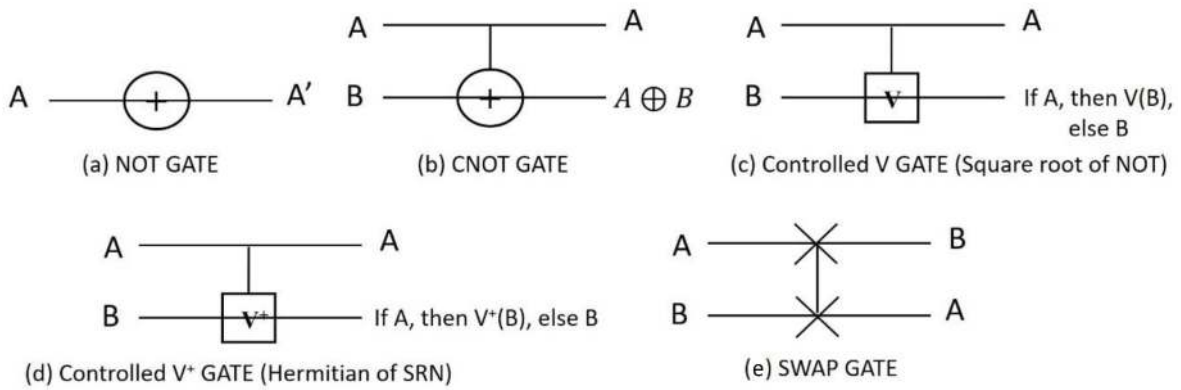

Fig. 4. Elementary quantum gates used to realize reversible gates.

- Controlled-V+ gate performs the inverse of V. In the controlled-V+ gate, the qubit B passes through the controlled part unchanged when the control signal A=0, i.e. Q = B. The unitary operation V+ $=V^{-1}$ is applied to the input B when A=1, i.e. Q=V+ (B). The properties observed in V and V+ quantum gates are V × V = NOT, V × V+ = V+ × V = I, and V+ × V+ = NOT. Thus, it is observed from the above expressions that two V gates in series as well as two V+ gate in series behave as a NOT gate.

Quantum circuit of a reversible logic gate is obtained from the quantum gates described above. Quantum Cost (QC) is obtained by

calculating the total number of primitive 1 × 1 and 2 × 2 quantum gates present in the quantum circuit.

The C^2NOT gate (Toffoli gate (TG)) maps three inputs (p, q, r) to corresponding three outputs (p, q, r ⊕ pq), where the product represents the AND operation. Here, p and q are control inputs while r is the target input. Fig. 3b gives the quantum circuit of TG which is constructed using CNOT, controlled V and controlled $V+$ gates. Total number of elementary quantum gates in the quantum circuit of TG gate is 5 which indicates its quantum cost.

3. Results and discussions

3.1. Logic synthesis and simulation

The proposed design of the reversible BUS gate is synthesized and verified using EDA tools like Xilinx and Model Sim. The design is compiled, RTL circuit tested, and simulated using this tool. The code is written in Verilog language. RTL schematic of reversible BUS gate is shown in Fig. 5 and simulated waveforms are shown in Fig. 6. From the simulation results obtained, the functionality of the proposed design is verified.

It can be seen from the simulation waveforms that OR & AND gate outputs are produced with A & B as inputs and $C = 0$ as control input. When $C = 1$, NOR & NAND gate outputs are produced. The control input $B = 1$ produces EXOR gate output. The control input $A = 1$ produces NOT gate output.

3.2. Implementation using FPGA

An FPGA or Field Programmable Gate Array is an integrated circuit that can be configured by the programmer after the chip is manufactured. The proposed BUS gate is implemented on FPGA Spartan XC3S400–5PQ208 kit (Fig. 7). The functionality of the designed gate is tested and verified by giving different inputs to the programmed FPGA and the outputs obtained. It can be concluded that the proposed BUS gate produces the output of all basic and universal gates based on the input combinations.

3.3. Gate level performance analysis of proposed reversible BUS gate

The key parameters to enhance the efficiency of the reversible logic design is the reduction in the number of constant input (CI) bits, number of garbage outputs (GO) and quantum delay. But the available reversible gates that function as basic, universal and special gates either have large number of constant inputs, or garbage outputs that would cause inefficient performance of the gate. These reversible gates do not provide all the functionalities of basic gates, universal gates or special gates.

In literature, some of the reversible gates such as Fredkin gate (FRG) [9], SMG gate [23], 'ALL GATE' [24], DPG gate [11] can function as basic, universal and special gates.

Comparison of the proposed BUS gate with the existing reversible gates of similar functionality in terms of the garbage outputs, constant inputs and number of reversible gates used is shown in Table 3. The analysis of reversible BUS gate with respect to Table 3 is discussed below.

- All the basic, universal and special gates (Copy, AND, OR, NOT, NAND, NOR, EXOR) can be realized using proposed BUS gate with one constant input. Quantum cost, garbage outputs, reversible logic gates used and constant inputs are 20, 1, 1 and 1 respectively.

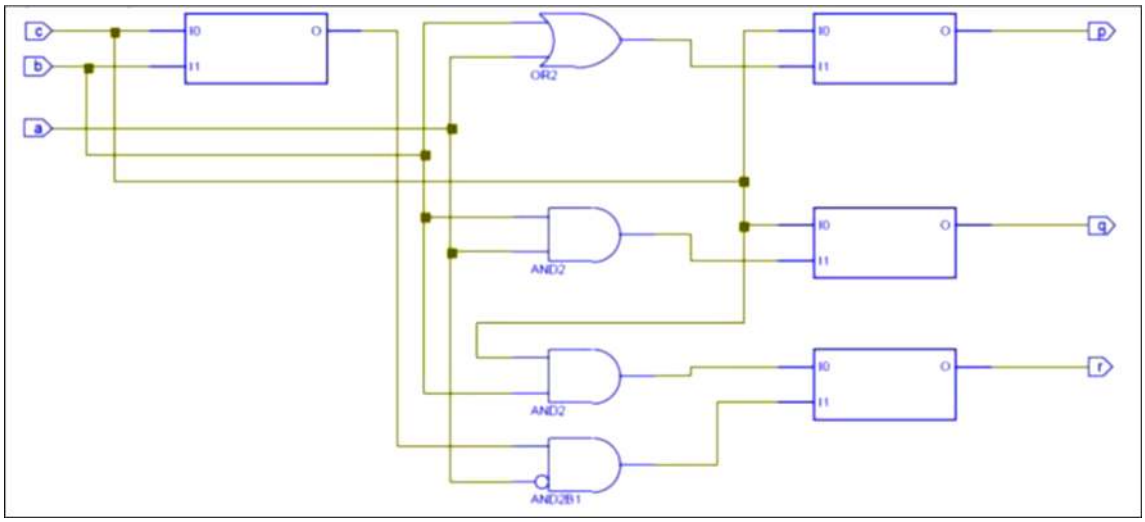

Fig. 5. Synthesis of RTL schematic of reversible BUS gate.

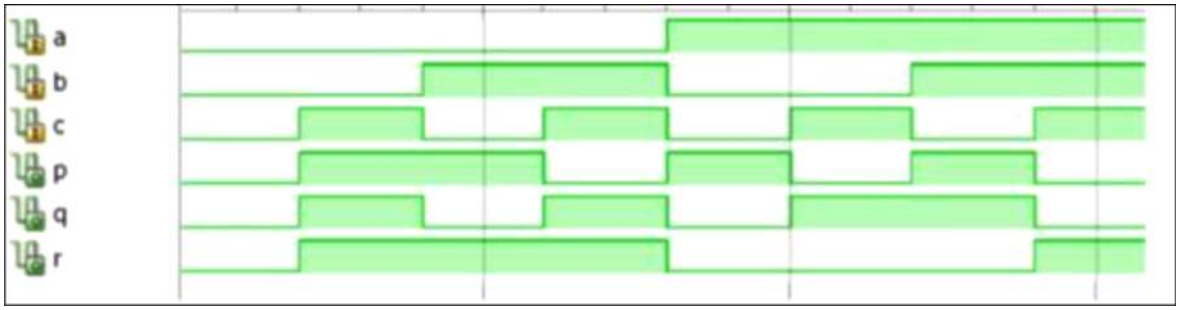

Fig. 6. Simulation results of reversible BUS gate.

Fig. 7. FPGA implementation of proposed reversible BUS gate.

Table 3
Comparison of reversible basic and universal gates.

Reversible Gate	Garbage outputs	Reversible Gates	Constant Inputs	Gates designed
Proposed BUS gate	1	1	1	Copy, AND, OR, NOT, EXOR, NAND, NOR Gates (**One control signal used**)
SMG [23]	2	1	2	Copy, AND, OR, NOT, EXOR, NAND, NOR Gates (**Two control signals used**)
ALL GATE [24]	1	1	2	Copy, AND, OR, NOT, EXOR, NAND, NOR Gates (**Two control signals used**)
DPG [11]	2	1	2	Copy, AND, OR, NOT, EXOR, NAND, NOR Gates (**Two control signals used**)
DKG [19]	1	1	2	Copy, NOT, EXOR, AND, OR and NAND gates (**Two control signals used, NOR o/p not produced**)
DKGP [21]	1	1	2	Copy, NOT, EXOR, AND, OR and NOR gates (**Two control signals used, NAND o/p not produced**)
FRG [9]	2	1	1	Copy, AND, OR, NOT gates
	1	2	1	EXOR gate (FRG+FG)
	2	2	2	NAND, NOR gates (FRG+FG)
SRK [20]	2	1	1	Copy, AND, OR, NOT, EXOR gates
	2	2	2	NAND, NOR gates (SRK+FG)

Quantum cost of reversible BUS gate is higher compared to all other gates given in the table, however, optimization techniques can be applied to further reduce the quantum cost.

- SMG gate [23] and DPG gate [11] can be used to realize Copy, AND, OR, EXOR, NAND and NOR gates with 2 control signals. NOT gate output is produced using 3 control inputs. For any given combination of control inputs, only 2 gates can be realized simultaneously. Quantum cost, garbage outputs, reversible logic gates used and constant inputs are 6, 2, 1 and 2 respectively. Even though quantum cost of SMG and DPG gate is less, higher number garbage outputs (2) are produced while 2 constant inputs are required to realize the basic and universal gates.
- ALL GATE [24] is used to realize Copy, AND, OR, EXOR, NAND and NOR gates using two control signals. Garbage outputs, reversible logic gates used and constant inputs are 1, 1 and 2 respectively. Different control inputs are needed to realize the basic gates or universal gates. NOT gate output is produced using 3 control inputs. Quantum cost is not computed by the authors.

- DKG gate [19] is used to realize Copy, NOT, EXOR, AND, OR and NAND gates using two control signals. Same control inputs do not produce all basic gate or universal gate outputs simultaneously. Different combinations of inputs are used as control inputs. NOR gate output cannot be realized. Quantum cost, garbage outputs, reversible logic gates used and constant inputs are 17, 1, 1 and 2 respectively..
- DKGP gate [21] is used to realize Copy, NOT, EXOR, AND, OR and NOR gates using two control signals. Same constant inputs do not produce all basic gate or universal gate outputs simultaneously. Different combinations of inputs are used as control inputs. NAND gate output cannot be realized. Quantum cost, garbage outputs, reversible logic gates used and constant inputs are 15, 1, 1 and 2 respectively.
- FRG gate [9] can produce outputs of Copy, AND & OR gate using one control signal (QC=5, GO=2, RG=1, CI=1). Output of NOT gate can be produced using 2 control inputs (QC=5, GO=2, RG=1, CI=2). FG gate should be used in addition to FRG gate to produce EXOR gate outputs with one control input (QC=6, GO=1, RG=2, CI=1). NAND & NOR gate outputs can be produced by FRG gate and FG gate (QC=6, GO=2, RG=2, CI=2).
- SRK gate [20] can produce outputs of Copy, AND, OR & EXOR gate using one control signal (QC=4, GO=2, RG=1, CI=1) and output of NOT gate using 2 control signals (QC=4, GO=2, RG=1, CI=2). NAND & NOR gate outputs can be produced by SRK gate in combination of FG gate (QC=5, GO=2, RG=2, CI=2).

Thus, it can be seen that, even though quantum cost of proposed BUS gate is slightly higher than SMG and DPG gates, only one garbage output is produced. Also, only one control signal is sufficient to realize basic, universal or special gates. In contrast, all other gates require 2 control signals. The control inputs given are not constant for all the gates and different control inputs are needed for different gates.

3.4. Performance analysis of the proposed reversible BUS gate at transistor level

The basic, universal and special gate circuits are designed and implemented using reversible BUS gate and conventional CMOS logic separately. The designs are simulated at 180 nm and 90 nm CMOS process technologies. The layout and simulated waveforms of BUS gate at 180 nm CMOS process technology are shown in Figs. 8 and 9. Evaluation of the proposed BUS gate with conventional basic and universal gates using 180 nm and 90 nm CMOS process technologies is given in Table 4. Power dissipations in reversible BUS gate and conventional circuit are found to be 0.184 mW and 0.517 mW respectively at 180 nm CMOS process technology. At 90 nm CMOS process technology, the same is 11.287μW and 13.134μW respectively. Thus, it can be seen that power dissipation in the BUS gate is lesser compared to CMOS circuit and there is a power reduction of 64.41% and 14.06% at 180 nm and 90 nm CMOS process technology respectively. Fig. 10 shows the percentage power reduction in reversible BUS gate w.r.t conventional circuit.

The proposed BUS gate is tested by implementing C17 circuit from IEEE ISCAS' 85 benchmark suite and analyzed with respect to its conventional CMOS design. Reversible Manchester adder as an application is designed and implemented using the BUS gate.

3.5. Benchmark circuit using BUS gate

ISCAS'85 benchmarks are a set digital combinational networks, distributed for researchers during International Symposium on Circuits and Systems (ISCAS) in the year 1985 as a basis for comparing results. The C17 benchmark circuit of ISCAS' 85 benchmark suite is a complicated design example with branching, multiple fan-in and fan-out. The gate level structure of C17 benchmark circuit is shown in Fig. 11. The C17 benchmark circuit is realized using proposed BUS gate. It is further implemented at 180 nm and 90 nm CMOS process technologies and simulated.

Table 5 gives the performance analysis of C17 benchmark circuit realized using BUS gate and conventional CMOS circuit. From the table, it can be seen that power and delay of the C17 circuit implemented with BUS gate gave better results with optimum power-delay product (PDP) than the C17 circuit using conventional CMOS circuit. Fig. 12 shows the percentage power saving in reversible logic circuit of C17 using BUS gate w.r.t conventional C17 circuit. C17 circuit implemented using BUS gate resulted in a power saving of 58.93% at 180 nm CMOS process technology and 64.11% at 90 nm CMOS process technology compared to its conventional

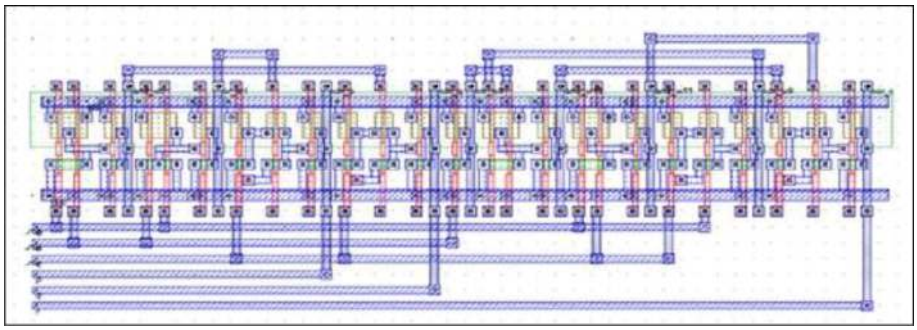

Fig. 8. Layout of proposed reversible BUS gate at 180 nm CMOS process technology.

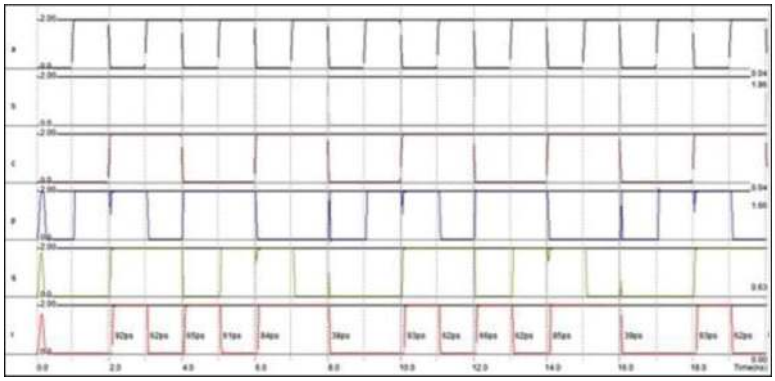

Fig. 9. Simulation waveform of BUS gate using 180 nm CMOS process technology.

Table 4
Evaluation of proposed BUS gate with conventional basic and universal gates using 180 nm and 90 nm CMOS process technologies.

Parameters	BUS gate		Conventional gate	
	180nm	90nm	180nm	90nm
Power dissipation (mW)	0.184	0.011287	0.517	0.013134
Delay (ps)	1.8333	2.625	10.125	10.875
Area (μm)^2	841.3	135.1	851.9	136.9
No. of transistors	74		62	

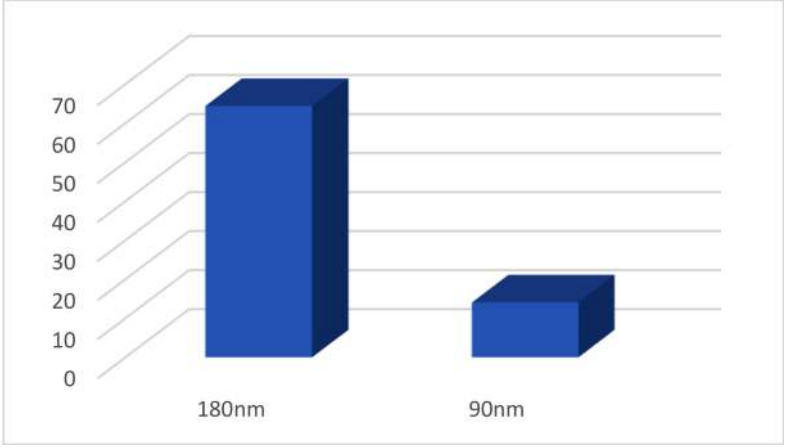

Fig. 10. Percentage of power reduction in reversible BUS gate w.r.t conventional circuit.

counterpart.

3.6. Manchester adder using proposed reversible BUS gate

Manchester adder cell has 3 inputs (x, y, & Cin) and 2 outputs (sum & Cout). If x and y inputs are zero then Cout is low regardless of the value of carry input, thus killing the carry input (i.e. carry kill signal $k=\overline{xy}$). If x and y are high, then Cout is high regardless of carry input, i.e. carry is generated for the next position (carry generate signal g=xy). If one of the inputs, x or y is high and the other is low, then Cout is equal to carry input, thus propagating the carry to next stage (carry propagate signal $p=x\oplus y$). The signals k, g, and p depend on only the input operands at the respective bit positions, so that they can be determined immediately when the operands are applied to the adder. This structure forms Fast Carry Chain adder or Manchester adder.

Proposed BUS gate is used to design the Manchester adder cell. Three signals are produced namely, generate (g=xy), propagate ($p=x\oplus y$) and kill ($k=\overline{xy}$). If both x and y are high, carry bit is generated i.e. output Cout is high. If x and y are low, carry bit is killed i.e. output Cout is low. If either x or y is high, output Cout is equal to carry input Cin. Depending on the inputs x & y, the output carry is either high, low or equal to carry input Cin, thus, reducing the propagation delay.

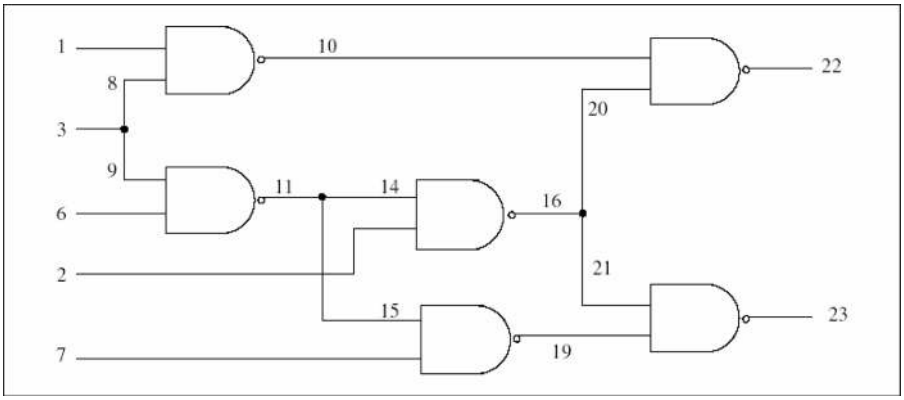

Fig. 11. C17 benchmark circuit-gate level.

Table 5
Performance evaluation of C17 benchmark circuit designed using BUS gate and conventional CMOS circuit.

	180 nm technology		90 nm technology	
Parameters	C17- BUS gate	C17-CMOS	C17- BUS gate	C17-CMOS
Power dissipation (mW)	0.858	2.089	0.056703	0.158
Delay (ns)	0.00790625	0.0114531	0.008609375	0.01215625
PDP (fJ)	6.783563	23.9256	0.488177	1.920688
% power saving w.r.t CMOS logic	58.93		64.11	

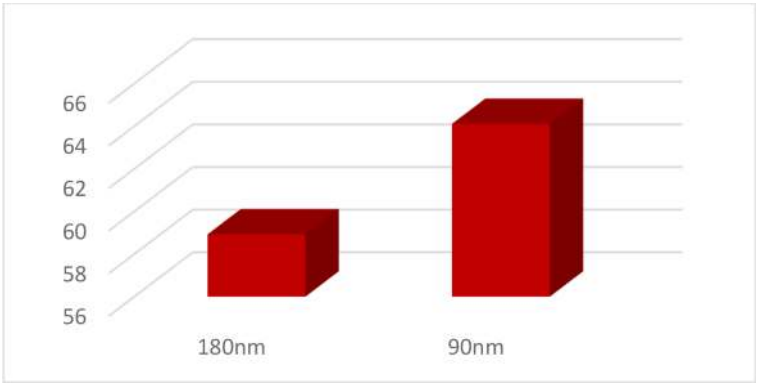

Fig. 12. Percentage power saving in C17 benchmark circuit using reversible BUS gate w.r.t conventional CMOS circuit.

The design of reversible Manchester adder cell using the proposed BUS gate has 4 constant inputs, 3 garbage outputs with a quantum cost of 25. It uses 5 FG gates and one BUS gate. It has a hardware complexity of (11XOR+7AND+ 1NOT).

4-bit Manchester adder is designed by cascading 4 Manchester adder cells. A 4-bit reversible Manchester adder with basic component as reversible Manchester adder cell is designed using the proposed BUS gate. The delay due to propagation of carry is reduced, either by generating or by killing the carry depending on the input bits. If both input bits are high, carry would be generated and if both are low, carry would be low irrespective of the input carry bit. Only if the input bits differ, next stage of the adder has to wait for the carry to be propagated from previous stage.

The Manchester adder cell as well as the 4-bit Manchester adder are simulated using Xilinx, and Model Sim software for evaluating their performance. RTL schematics are shown in Fig. 13 while Fig. 14 display the results obtained during simulation..

Thus, from the simulation results, the functionality of the reversible Manchester adder cell and 4-bit Manchester adder are verified.

4. Conclusion

A new 3 × 3 reversible BUS gate that functions singly as basic, universal and special gate with a quantum cost of 20 is proposed in this paper. The proposed design has fewer number of constant inputs and garbage outputs compared to the other designs available in the literature. An attempt is made to design and implement a reversible Manchester adder cell and 4-bit Manchester adder using the

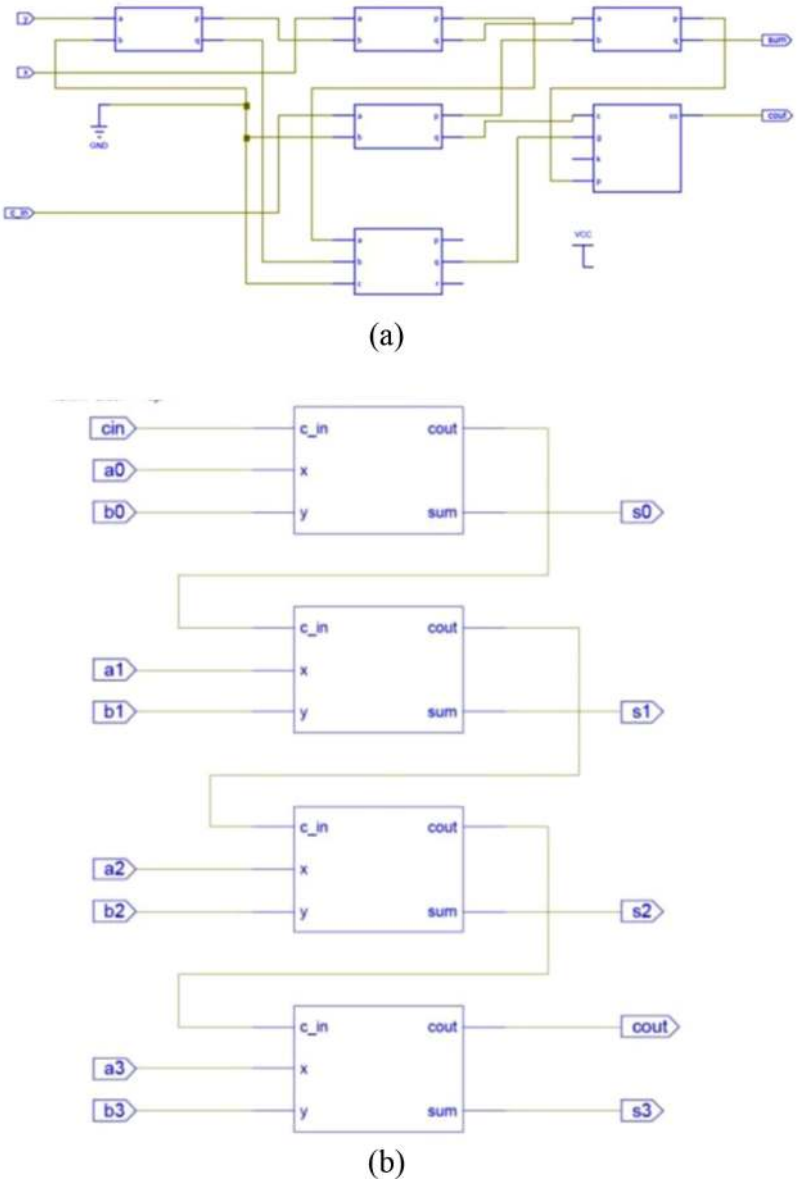

Fig. 13. RTL schematic of (a) Manchester adder cell (b) 4-bit Manchester adder using BUS gate.

proposed BUS gate. The power dissipation and delay in the BUS gate is less compared to the gates implemented using CMOS logic with a power reduction by 64.41% and 14.06% at 180 nm and 90 nm respectively. Comparison of Power dissipation and delay shows that the C17 benchmark circuit of ISCAS' 85 benchmark suite implemented with BUS gates gave better results with optimum PDP than that of the circuit using conventional gates. Power saving in C17 benchmark circuit implemented using BUS gate is 58.93% and 64.11% respectively for the 180 nm & 90 nm CMOS process technology compared its conventional counterpart. The reversible BUS gate can be utilized in building any complex, versatile high speed and low power digital computing systems such as higher order reversible arithmetic network designs, and complex design of quantum computers.

CRediT authorship contribution statement

D. Krishnaveni: Conceptualization, Methodology, Software, Validation, Investigation, Writing - original draft, Writing - review & editing. **M. Geetha Priya:** Data curation, Visualization, Supervision, Software, Project administration.

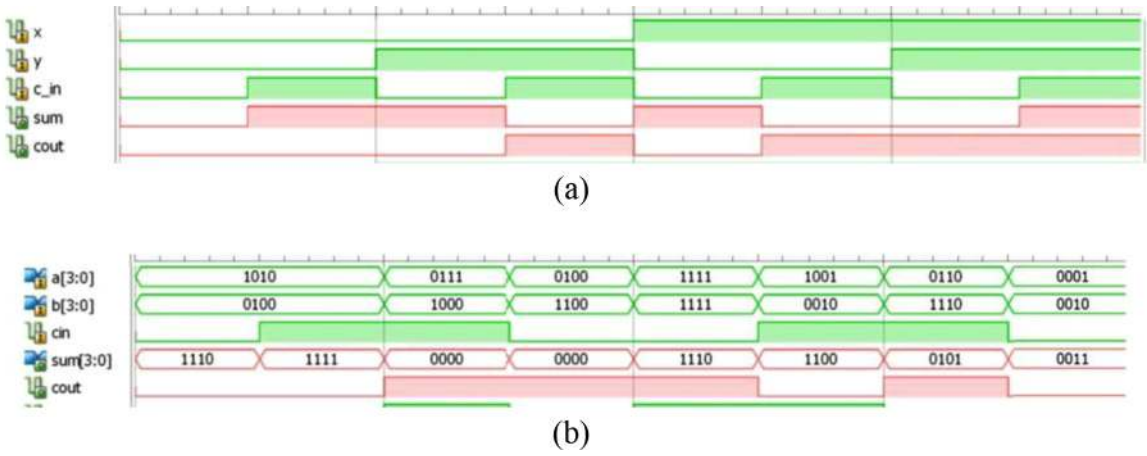

Fig. 14. Simulation results of (a) Manchester adder (b) 4-bit Manchester adder.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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