Design of Arithmetic Logic Unit using Pseudo Dynamic Buffer based Domino Logic

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Abstract. Design of combinational circuits using dynamic logic has the advantage of high speed and less area when compared to conventional CMOS logic. However, it pose problem while cascading dynamic logic architectures and also more prone to leakage current issue. These issues are overcome by using domino logic with static inverter at the output of dynamic node. The increased power dissipation at the output node is reduced by using pseudo dynamic buffer based domino logic by having static like switching at the output node. This paper details the design of arithmetic and logic unit designed using conventional and pseudo dynamic buffer based domino logic. The arithmetic unit comprise adder, subtractor, multiplier and logical unit comprise AND, NAND, OR, NOR and XOR logic blocks based on pseudo dynamic buffer based domino logic and it is compared with the Arithmetic logic unit designed using conventional domino logic. The design and simulations are performed using UMC90nm technology node library using Cadence® Virtuoso® tool. The simulation result of ALU unit demonstrates that arithmetic logic unit designed using PDB logic has reduction in power consumption by 89.14% and delay by 1.995% while compared to conventional domino logic.

1. Introduction

The design of fast and complex processor is underlies on the design of more efficient arithmetic and logic unit (ALU). The design of ALU using various dynamic logic styles enables in achieving high speed with complex operations. The total power consumption consists of two components such as dynamic power and static power. Dynamic power is the power consumed when device is active. Static power is the power consumed when device is powered up but no signals are changing the output value [1]. There are two main source of dynamic power consumption. Primary source of power consumption is switching power, which is the power required to charge and discharge the output capacitance. It depends on the frequency of operation of the device and the activity factor. Hence we can write the equation for dynamic power consumption as,

$$P_{dyn} = \alpha C_L {V_{dd}}^2 f_{clk} \text{----------(1)}$$

Where, α is the activity factor of the circuit, C_L is the output load capacitance, $V_{dd}$is the supply voltage and $f_{clk}$is the frequency of operation of the circuit. Second source of power consumption which contributes to the dynamic power is due to internal power. Internal power is due to the short circuit current which occurs when both PMOS and NMO are on and also on the current required to charge and discharge the internal capacitance of the cell. We need to add this component of power consumption to the dynamic power equation,

$$P_{dyn} = \left(\alpha C_L {V_{dd}}^2 f_{clk}\right) + \left(t_{sc} V_{dd} I_{peak} f_{clk}\right) \text{----------(2)}$$

Where, t_{sc} is the time duration of the short circuit current, I_{peak} is the sum of short circuit current and the current required to charge the internal capacitance. If the ramp time of the input signal is kept short, then the short circuit current occurs only for short duration of time in each transition. Hence the overall dynamic power is dominated by the switching power. In dynamic logic, the switching activity happens in both pre-charge phase and also during the evaluation phase if the logic is true. This contributes to increase in the dynamic power consumption of the circuit. This paper is arranged as follows. Section 2 explains about conventional domino logic and pseudo dynamic buffer based domino logic architecture. Section 3 explains about the integration and implementation of arithmetic and logical blocks. Section 4 presents the simulation and comparison of individual modules using domino logic and PDB based domino logic. Section 5 gives the conclusion of our work.

2. Methodologies

2.1. Conventional Domino Logic

The basic structure of the conventional Domino logic circuit is shown in figure 1. The operation of the domino logic circuit comprises of two phases namely pre-charge phase and evaluation phase [2].

2.1.1. Pre-charge phase

During the pre-charge phase CLK input is logic 0 this will turn ON the PMOS transistor M_p. Hence dynamic node X will be pre-charged to V_{DD} and output will be logic 0. During this time the evaluation transistor M_e is OFF, so the pull-down path is disabled.

2.1.2. Evaluation phase

During the evaluation phase CLK input is logic 1 this will turn OFF the pre-charge transistor Mp and turn ON the evaluation transistor M_e. The dynamic node X will be conditionally discharged based on the input values and pull down circuitry. If the inputs are LOW then PDN is OFF this makes the dynamic node X to remain at V_{DD} and output node discharges to LOW via static inverter. If the inputs are HIGH then PDN is ON this makes the dynamic node X to be pulled down to LOW and this makes the output node to be HIGH state.

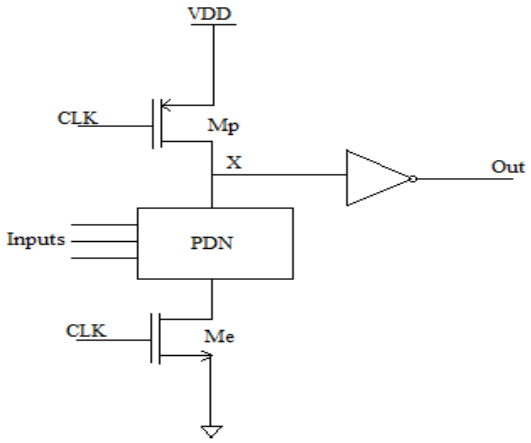

Figure 1. Conventional Domino logic circuit

Let us assume that the input value remains at HIGH state this makes dynamic node X to be pulled down to LOW and makes the output node at HIGH state. During the pre-charge phase the dynamic node X will be pre-charged V_{DD} and output node discharges to LOW. In the next evaluation phase since input remains at HIGH state dynamic node discharges to LOW and output node will be at HIGH state. Thus unnecessary switching occurs at the output even when there is no change in the input logical levels during the consecutive evaluation phases. Unnecessary transition at the output will causes the increase in dynamic power or switching power. By avoiding this unnecessary transition at the output we can reduce the dynamic power dissipation of the circuit. One logic style which reduces this unnecessary transition at output is Pseudo Dynamic Buffer (PDB) based Domino logic.

2.2. Pseudo Dynamic Buffer based Domino logic

In domino logic circuit switching power is very high. To reduce the switching power we can use pseudo dynamic buffer (PDB) based domino logic circuit [3]. Here, source terminal of transistor M2 of the static inverter is not connected to ground, instead it is connected to node A (which is drain terminal of the footer transistor M_e). This prevents the propagation of the pre-charge pulse to output node.

2.2.1. Case1: All the inputs are LOW

During the pre-charge phase dynamic node X will be charged to HIGH this will turn on NMOS transistor M2 of the inverter [4]. Since source terminal of M2 is connected to drain of footer transistor at node A, there is no path for output to discharge because evaluation transistor M_e is OFF since CLK is LOW. Hence output node will hold the previous value this will avoid the pre-charge to propagate to output. In evaluation phase, since all inputs are LOW dynamic node X will not discharge to GND this will turn ON transistor M2 and footer transistor is also ON. Hence, output node will discharge to LOW.

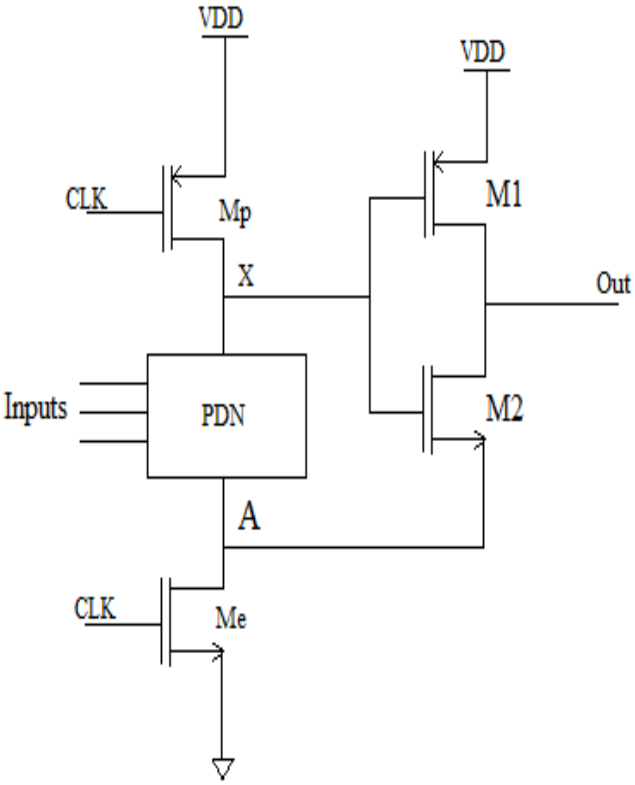

Figure 2. PDB based domino logic circuit

2.2.2. Case 2: All the inputs are HIGH

During the pre-charge phase dynamic node X will be charged to HIGH but output node will not discharge to LOW because footer transistor M2 is OFF and no path for output to discharge. Output node will hold the previous value this will avoid the pre-charge to propagate to output. In evaluation phase, since all inputs are HIGH dynamic node X will discharge to GND this will turn ON transistor M1 and output node will charged to V_{DD}. Hence we can avoid the unnecessary transition at the output due pre-charge when input is stable and we can reduce the switching power [5].

3. Arithmetic and Logical Unit (ALU)

The ALU is the prime component of any processor. The power consumption of the ALU majorly contributes for the total power consumption of the processor. Hence, the appropriate logical style of

the design of the combinational circuits used in the ALU can significantly lead to the overall power reduction of the processor. In this direction, the individual modules of the ALU are designed using the pseudo dynamic buffer based domino logic techniques.

3.1. Functional blocks of ALU

This section elaborates the design of the ALU using conventional domino logic and PDB based domino logic. The arithmetic unit comprises of adder, subtractor, multiplier and logical unit comprise AND, NAND, OR, NOR and XOR logic blocks. The primary modules of ALU are as following,

3.1.1. Adder – Subtractor Unit

The adder – subtractor unit shown in Figure 3. is capable of performing addition and subtraction operations based on the mode signal M [6]. This avoids the use of two individual units for adder and subtractor. When the mode control signal M = 0 it will perform the addition operation A + B. When the mode control signal M = 1 it will perform the subtraction operation {A + (-B)}.

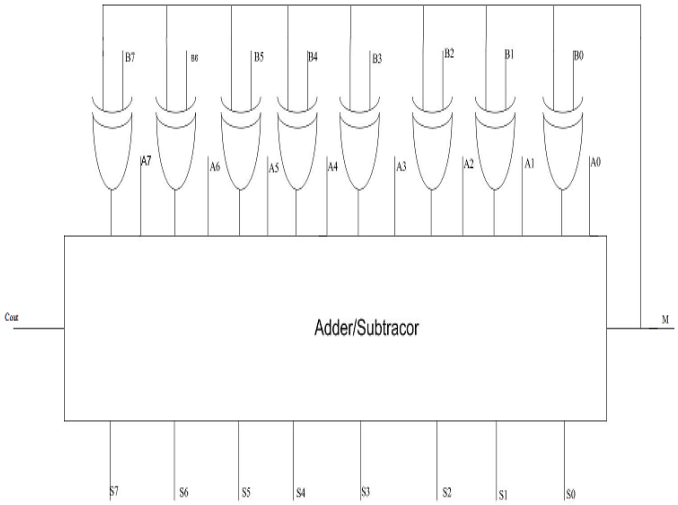

Figure 3. Adder – Subtractor unit

When M = 1 then B bits are complemented by the use of XOR gate and addition from M makes it a two's complement addition of B with A.

In other word,

S = A + (-B)

On the other hand, when control signal M = 0, the addition operation will be carried out.

S = A +B

Block of adder – subtractor is implemented by using the 8 bit carry look ahead adder architecture in domino logic and pseudo dynamic buffer based domino logic [7]. The advantage of the carry look ahead adder is the propagation delay is reduced. The carry output at any stage is dependent only on the initial carry bit of the beginning stage. Using this adder structure it is possible to calculate the intermediate results. This adder is the fastest adder used for computation.

3.1.2. Multiplier Unit

The 8X8 bit vedic multiplier can be implemented by using four 4X4 vedic multiplier and three 8 bit carry look ahead adder [8]. 4X4 vedic multiplier is implemented by using four 2X2 vedic multiplier and three 4 bit carry look ahead adder. Core architecture of 2X2 vedic multiplier consist of four AND gate circuit and two half adder circuit. The advantage of this multiplier is that as the bit increases, the area and the delay increases very slowly, hence it is faster when compared with the other multiplier architecture [9]. Hence total delay of 2X2 vedic multiplier is the sum of delay of two half adders after

partial product generation. Half adder circuit is constructed by using 2 input XOR gate and 2 input AND gate. All these individual components are implemented by using the conventional domino logic and PDB based domino logic architecture style [10].

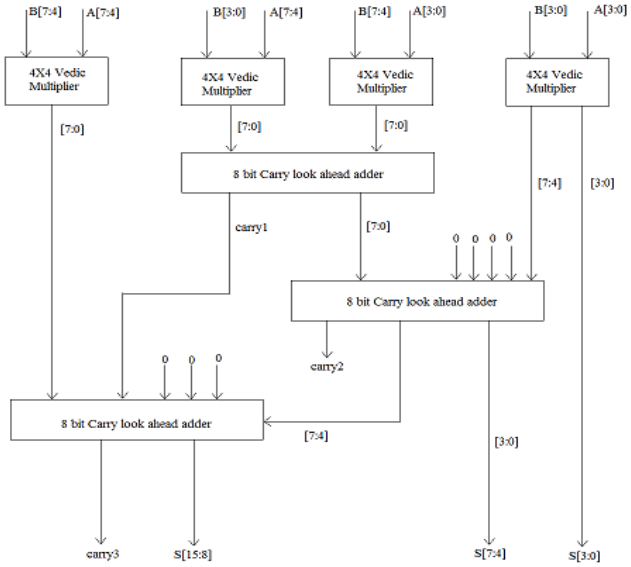

Figure 4. 8X8 Vedic Multiplier unit

3.1.3. Logical Unit

The ALU supports the logical operations such as AND, NAND, OR, NOR and XOR operations [11]. All logical blocks perform its operation on the 8bit input data and results the 8 bit data as output. Decoder circuit is used to send the enable signal to individual components by using the opcode which is used as the input of the 3:8 decoder. Based on the opcode value anyone output of 3:8 decoder will go high and this signal can be used as the enable(En) signal for the arithmetic and logical units.

3.1.4. Integration of ALU

ALU is integrated using the decoder circuit. Decoder circuit is used to send the enable signal to individual components by using the opcode which is used as the input of the 3:8 decoder. Based on the opcode value anyone output of 3:8 decoder will go high and this signal can be used as the enable(En) signal for the arithmetic and logical units. All the components are integrated together to form the ALU architecture as shown in Figure 5 [12]. First and second output of the decoder will act as the enable signal to adder/subtractor block. For adder/subtractor block to perform addition then mode(Cin) should be M = 0. If adder/subtractor block to perform subtraction the mode (Cin) should be M = 1. We can achieve this by inverting the first output and use as first input of AND gate and second output of decoder is used as the second input of AND gate. The output of this AND gate is the Cin or mode(M) signal for adder/subtractor block. Both first and second output of decoder is given as input of OR gate and output of OR gate is used as En signal for adder/subtractor block. For remaining logical blocks output of decoder is used as the En signal to perform the required operation [13].

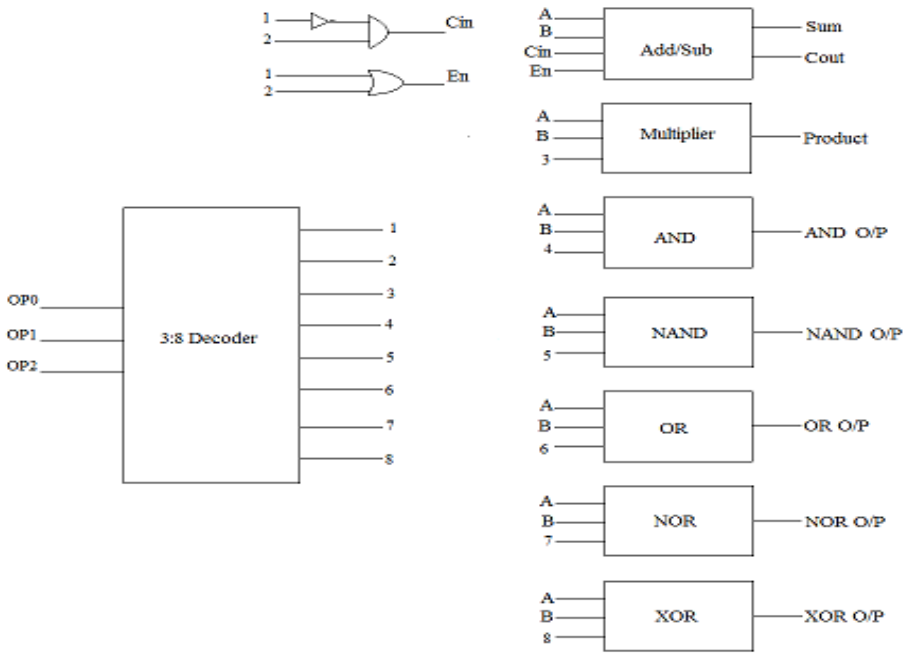

Figure 5. ALU Module

4. Simulation and Analysis

The various sub blocks of the ALU design are simulated using conventional domino logic and pseudo dynamic buffer based domino logic style [9] using UMC90nm technology node library using Cadence® Virtuoso® tool. Table I shows the power dissipation comparison of three individual arithmetic blocks such as adder unit, subtractor unit and vedic multiplier unit. It shows that for adder unit in ALU it has the power dissipation of 12.45mW and 1.426mW for conventional domino logic and PDB based domino logic respectively. For subtractor unit power dissipation is 12.54mW in conventional domino logic structure and 1.384mW in PDB based domino logic structure. For vedic multiplier unit it is 15.74mW and 4.221mW respectively. From the graph it shows that the reduction in power dissipation in PDB based domino logic style by 79.45% for adder unit, 80.07% for subtractor unit and 57.71% for vedic multiplier unit over conventional domino logic style.

4.1. Table I. Power comparison of 8bit arithmetic unit of ALU

Power dissipation(mW)		
Module	**Conventional Domino Logic**	**Pseudo Dynamic Buffer based Domino Logic**
Adder unit	12.45	1.426
Subtractor unit	12.54	1.384
Vedic Multiplier unit	15.74	4.221

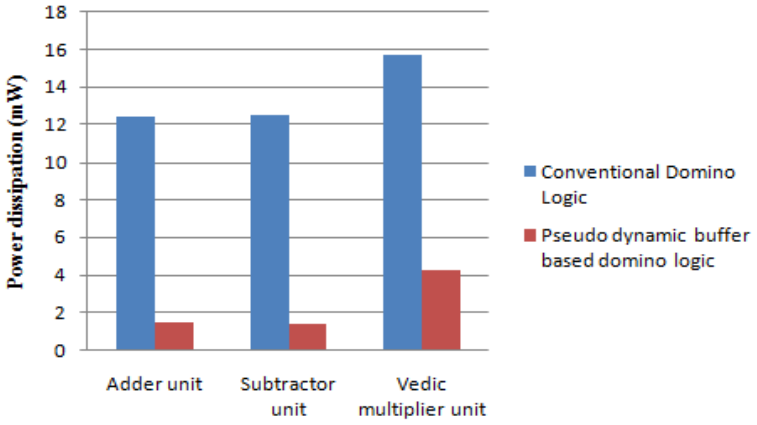

Figure 6. Power comparison of 8bit arithmetic unit of ALU

Table II shows the power dissipation comparison of individual logical blocks of ALU such as AND, NAND, OR, NOR units. All logical blocks perform its operation on the 8bit input data and results the 8 bit data as output. For AND gate power dissipation is 10.86mW for domino logic and 0.714mW for PDB based domino logic architecture. For NAND gate it is 23.38mW and 0.781mW respectively for domino logic and PDB based domino logic structure. For OR gate power dissipation is 13.3mW for domino circuit and 0.6804mW for PDB based domino logic circuit. For NOR gate power dissipation is 18.34mW and 0.473mW respectively for conventional domino logic architecture and pseudo dynamic buffer based domino logic architecture. We can able to achieve the reduction in power dissipation in PDB based domino logic style architecture by 87.65% for AND gate, 93.53% for NAND gate, 90.27% for OR gate and 94.97% for NOR gate logical blocks of ALU over the logical blocks implemented using conventional domino logic style architecture.

4.2. Table II. Power comparison of 8bit logical unit of ALU

Power dissipation(mW)		
Module	**Conventional Domino Logic**	**Pseudo Dynamic Buffer based Domino Logic**
AND gate	10.86	0.714
NAND gate	23.38	0.781
OR gate	13.3	0.6804
NOR gate	18.34	0.473

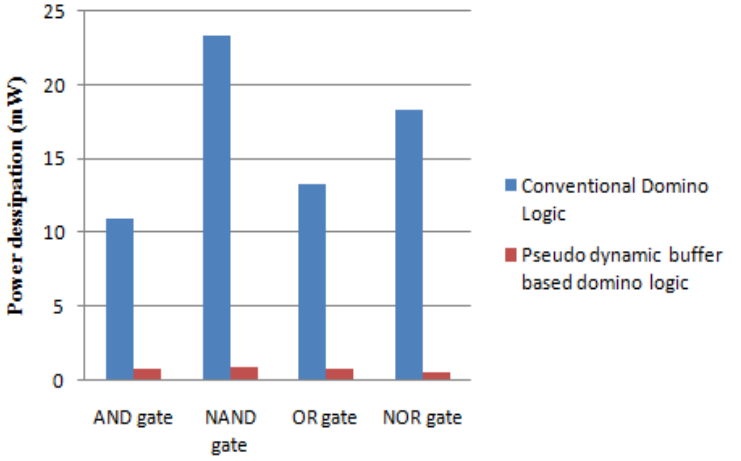

Figure 7. Power comparison of 8 bit logical unit of ALU

5. Conclusion

Arithmetic and logic units are designed and implemented for two types of dynamic logic styles such as conventional domino logic style and pseudo dynamic buffer based domino logic style using UMC90nm technology node library using Cadence® Virtuoso® tool. The switching power overhead which is incurred in conventional domino logic style during pre-charge and evaluation phases is reduced in pseudo dynamic buffer based domino logic style by having static like switching at the output node. The pseudo dynamic buffer based domino logic realizes a power reduction of 83.29% as compared to conventional domino logic ALU. ALU consumes maximum power of 4.221mW for the multiplication operation. Similarly, ALU consumes minimum power of 0.4733mW for the NOR logical operation.

6. References

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