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Error Compensation Techniques for Fixed-Width Array Multiplier Design — A Technical Survey*

S. Balamurugan† and P. S. Mallick‡

School of Electrical Engineering,
VIT University, Vellore 632014, India
†*sbalamurugan@vit.ac.in*
‡*psmallick@vit.ac.in*

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This paper provides a comprehensive review of various error compensation techniques for fixed-width multiplier design along with its applications. In this paper, we have studied different error compensation circuits and their complexities in the fixed-width multipliers. Further, we present the experimental results of error metrics, including normalized maximum absolute error ($\varepsilon_{\max}$), normalized mean error ($\varepsilon_{\text{mean}}$) and normalized mean-square error (ε_{mse}) to evaluate the accuracy of fixed-width multipliers. This survey is intended to serve as a suitable guideline and reference for future work in fixed-width multiplier design and its related research.

Keywords: Mean error; maximum absolute error; mean-square error; fixed-width multiplier; DSP; multimedia computing; Booth multiplier.

1. Introduction

Multimedia applications are widely used in many embedded and portable devices such as latest smart phones, tablets, MP3 players, digital camera and personal digital assistant (PDA), which require low power consumption within high performance constraints. It is expected that in the coming decade, the amount of information to be processed through multimedia and communication systems will grow enormously which demands power efficient VLSI architectures. The practical implementation of algorithms used in many of the communication and digital signal processing (DSP) systems, such as filtering,[1] convolution, fast Fourier transform (FFT), discrete cosine transform (DCT),[2] and hardware implementation of mathematical functions[3–6] maintain fixed-width operations to avoid the excessive growth in the word length.

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Parallel multipliers[7–9] are fundamental building blocks in most of the multimedia and DSP applications and are repetitive, but they require large computational capability to calculate. Many of the multimedia applications maintain the fixed-width operations and in most of the cases these results can be interpreted by human assumptions even if they not perfect. This helps to eliminate the need of true product in the multiplier output. The promising solution for this kind of application is fixed-width multipliers, which receives an n-bit multiplier operand as well as an n-bit multiplicand operand and computes n-bits output as a product.

The most obvious choice to design a fixed-width multiplier is by using full-width multiplier ($n \times n$ multiplier with $2n$ bits output), whose output is rounded to n bits. This method is also known as post-truncation (PT) method. This method gives best results in terms of errors and it is a baseline for evaluation of fixed-width multipliers. On the other hand, fixed-width multiplier can be achieved by directly eliminating the partial products of the n least significant column but huge truncation error is introduced. This method is also known as direct-truncation (DT) method. Fixed-width multipliers rely on the optimal trade-off of computational accuracy for power and/or circuit complexity/chip-area.

In this survey, we have followed a practical approach to study various error compensation circuits for fixed-width multipliers with low hardware cost. The major two techniques used to reduce the error in the fixed-width multipliers are constant correction techniques (CCM) and variable correction techniques (VCM). These techniques introduce suitable compensation circuits, and estimated carries are added to the carry inputs of the retained adder cells that partly compensates the dropped terms, which significantly reduce the truncation error. In this review, an attempt has also been made to compare array based fixed-width multipliers experimentally on the basis of error metrics, including normalized maximum absolute error ($\varepsilon_{\max}$), normalized mean error ($\varepsilon_{\text{mean}}$) and normalized mean-square error (ε_{mse}) to evaluate the accuracy of fixed-width multipliers. This review shows distinct advantages, complexities and hardware implementation of various fixed-width multipliers available in the literature.

2. Full-Width Multiplier

A full-width parallel multiplier receives two n-bit binary numbers and computes the $2n$ bits output as a weighted sum of partial products. Two different parallel multiplier architectures have been proposed in the Literature, namely tree based multipliers,[10,11] and array based multipliers.[12,13] These exploit a structure composed of full adder and half adder which reduces the entire matrix of the partial products to two rows, which will be input to the final adder or vector merging adder (VMA). Array based multiplier is a very common type of parallel multiplier due to its regular structure[14] and it is being a subject of investigation in this paper.

An $n \times n$ unsigned Braun array multiplier which computes a $2n$-bit product P as follows:

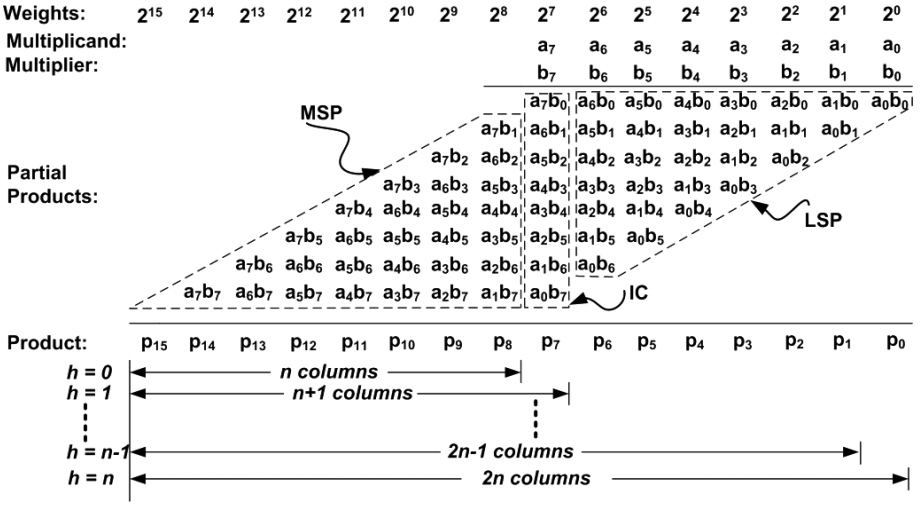

Fig. 1. Subdivision of the matrix of partial products, for unsigned multiplier, $n = 8$ with $h = 0$.

The partial product matrix is subdivided into several regions as shown in Fig. 1. The most significant part (MSP) includes the leftmost n columns of the partial product matrix. The input correction (IC) vector is the $(n + h + 1)$th column, where h is the trade-off parameter between accuracy and area complexity, that varies from 0 to n. When h increases, the error introduced by the multiplier decreases while the power consumption, delay, and area occupation increase. The remaining columns constitute the least significant part (LSP). This can be expressed as

$$\mathrm{P_{full\_width}} = (\mathrm{S_{MSP}} + \mathrm{S_{IC}} + \mathrm{S_{LSP}})\,, \tag{1}$$

where

$$\begin{aligned}\mathrm{S_{MSP}} = {} & ((\mathrm{a_{n-1}\,b_{n-1}}) \times 2^{2n-2}) + ((\mathrm{a_{n-1}\,b_{n-2}} + \mathrm{a_{n-2}\,b_{n-1}}) \times 2^{2n-3}) \\ & + \cdots + ((\mathrm{a_{n-1}\,b_{1-h}} + \mathrm{a_{n-2}\,b_{2-h}} + \cdots + \mathrm{a_{1-h}\,b_{n-1}}) \times 2^{2n-n-h})\,, \end{aligned} \tag{2}$$

$$\mathrm{S_{IC}} = \sum_{i=h}^{n-1} (\mathrm{a_{n-1-i}\,b_{i-h}}) \times 2^{n-h-1}\,, \tag{3}$$

$$\begin{aligned}\mathrm{S_{LSP}} = {} & ((\mathrm{a_{n-2-h}\,b_0} + \mathrm{a_{n-3-h}\,b_1} + \cdots + \mathrm{a_0\,b_{n-2-h}}) \times 2^{n-2-h}) \\ & + ((\mathrm{a_{n-3-h}\,b_0} + \mathrm{a_{n-4-h}\,b_1} + \cdots + \mathrm{a_0\,b_{n-3-h}}) \times 2^{n-3-h}) \\ & + \cdots + ((\mathrm{a_1\,b_0} + \mathrm{a_0\,b_1}) \times 2^1) + ((\mathrm{a_0\,b_0}) \times 2^0)\,. \end{aligned} \tag{4}$$

An $n \times n$ unsigned Braun array multiplier can be easily extended to the Baugh–Wooley array multiplier. Considering two n-bit signed numbers that perform two's complement multiplication,[11] the subdivision of partial products matrix are shown in Fig. 2.

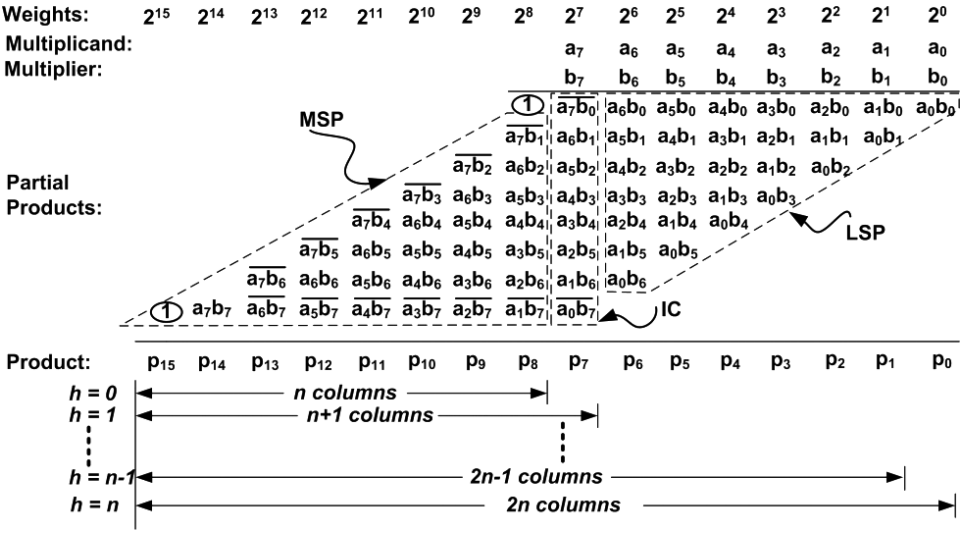

Fig. 2. Subdivision of the matrix of partial products, for Baugh–Wooley array multiplier, $n = 8$ with $h = 0$.

Recently, Booth multiplier[13] design is popular due to the high speed computation. The Booth multiplier is widely used in ASIC applications, where area and time is most important. In Booth multiplier, the numbers of partial products are halved by using modified Booth encoder (MBE). Consider the multiplication of two 2's complement n-bit number, the subdivision of partial product matrix is shown in Fig. 3, where $S_{i,j}$represents the jth bit product of the ith row.

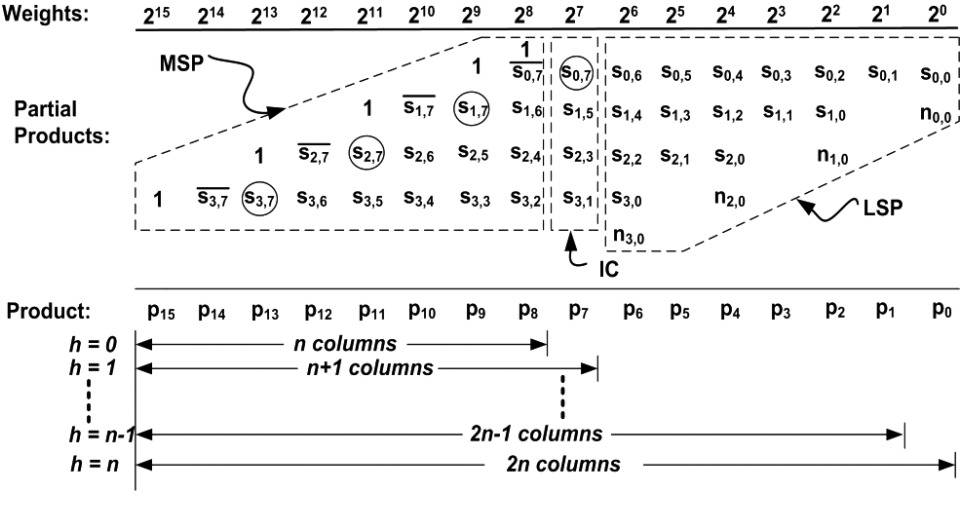

Fig. 3. Subdivision of the matrix of partial products, for modified Booth multiplier, $n = 8$ with $h = 0$.

2.1. *Full-rounded (or) post-truncated multiplier*

Conceptually, the full-rounded or post-truncated multiplier can be obtained by forming all the partial products as in full-width multiplier, then a rounding constant "1" added in the column immediately to the right of the final-product LSB. The LSB is the least significant bit of the truncated multiplier output P. This ensures accurate result of the n bit output, but requires almost the same area as a full-width multiplier. This can be expressed as

$$\mathrm{P_{Post\_Trunc}} = \mathrm{trunc_n}\left(\mathrm{S_{MSP}} + \mathrm{S_{IC}} + \mathrm{S_{LSP}} + \frac{\mathrm{LSB}}{2}\right). \tag{5}$$

2.2. *Direct truncated multiplier*

The simplest method of obtaining a fixed-width multiplier is by removing (or not forming) the partial product matrix of IC and LSP directly and only that the most significant half needs to be calculated. This reduces area and power at the expense of a large truncation error. This can be expressed as

$$\mathrm{P_{Direct\_Trunc}} = \mathrm{S_{MSP}}\,. \tag{6}$$

3. Fixed-Width Multiplier Design

The basic idea of a fixed-width multiplier is to calculate the result by only using the $n + h$ most significant column (MSP) and approximating the contribution of the less significant part with a function of the input correction vector. The general scheme of a fixed-width multiplier is shown in Fig. 4. In order to reduce truncation error introduced by the direct truncation method, many approaches have been proposed in the literature[15–50,53,54] to design error compensation circuits with less truncation error and less area overhead. The compensation methods can be classified into two categories: compensation with constant correction value[15–17] and compensation with variable correction value.[18–57]

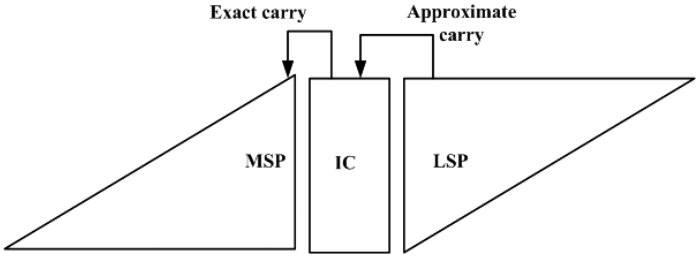

Fig. 4. General scheme of a fixed-width multiplier.

3.1. *Constant correction methods*

In constant correction methods (CCM), the authors[15–17] estimate pre-determined constant (K) of omitted partial products then added to the final product. The circuit can be simpler than that of variable correction methods. In CCM, since the actual data present in the input is not taken into account, large error is introduced into the output. This can be expressed as

$$\mathrm{P_{CCM}} = \mathrm{trunc_n}(\mathrm{S_{MSP}} + \mathrm{K})\,. \tag{7}$$

In Ref. 17, Kidambi *et al.* simplified the multiplier by removing both input correction vector and LSP part of the partial products and estimated constant value for a given bit precision which is added to the final product. This technique reduces the area and power consumption to halves for $h = 0$ with respect to the post truncated method, but a high error in the output limits the uses in practical applications. This technique is extended to $h \geq 0$ by Shuttle and Swartzlander,[16] where rounding error is also taken into account to estimate the total error.

3.2. *Variable correction methods*

In variable correction methods (VCM), the partial products in LSP are dropped, and this is compensated with the introduction of a suitable function of IC partial products ($(n + h + 1)^{\mathrm{th}}$ column). The accuracy of fixed-width multiplier is significantly improved in the variable correction fixed-width multiplier.[18–50,53,54] The main challenge for fixed-width multiplier design is to find efficient compensation function to improve the accuracy with less hardware cost. We consider the number of output bit $w(= n)$, while h is a design parameter which can be used to increase the accuracy without changing the weight of the output LSB. For experimental error analysis, we have considered the architectures with $h = 0$ only. However, this paper considers both signed and unsigned topologies for $h > 0$ also. The variable correction function can be expressed as

$$\mathrm{P_{VCM}} = \mathrm{trunc_n}(\mathrm{S_{MSP}} + \mathrm{f(IC)})\,. \tag{8}$$

Variable correction method was introduced by King and Swartzlander for an unsigned fixed-width multiplier, where partial product bits in the 2^{n-1}(IC) column was used as correction carries into the full adder cell of 2^n column.[18] This method reduces the error metrics effectively at the same time with less hardware cost.

Jou *et al.*[21] reported two different designs with variable correction method for unsigned and two's complement fixed-width multipliers, where they analyze the source of errors generated by LSP part, and then designing carry-generating circuit C_g. Carry generation circuit manipulates the partial products in 2^{n-1} column with circuit composed of AND-OR (AO) gates. For unsigned multiplier, the compensation circuit has n input and $n - 1$ outputs which consists of $(n - 2)$ AO cells and one 2-input AND gate as shown in Fig. 5. Similarly, the compensation circuit for two's

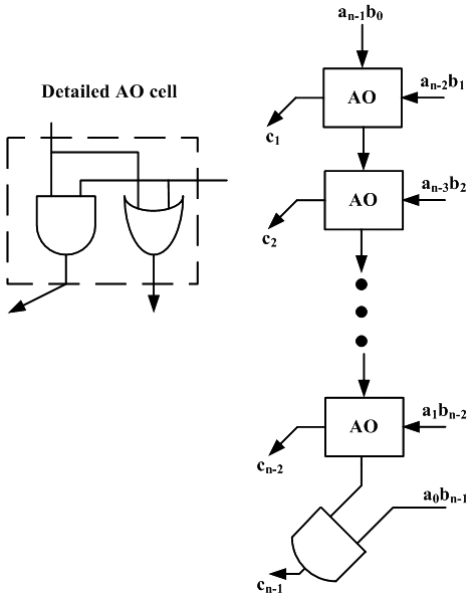

Fig. 5. Jou 99 correction logic for unsigned multiplier, $w = n$ and $h = 0$.

complement multiplier is shown in Fig. 6, which consists of $(n-2)$ OR cells and one 2-input NOR gates. This gives significant improvement in accuracy than that of direct truncated (DT) signed multiplier. However, its ripple based error compensation circuit not only requires considerable amount of logic gates when n increases, but also reduces the speed of the multiplier.

Van *et al.*[22] proposed a new error compensation circuit by choosing proper generalized index to improve the error performance of signed fixed-width multipliers. The error compensation circuit has n inputs and $(n-1)$ outputs which consist of $(n-2)$ AND cells and one NAND gate as shown in Fig. 7. The more generalized method for family of low-error area-efficient signed fixed-width multiplier with $h \geq 0$ has been explained in Ref. 25. This extended work improves the error performances with same area as compared to two's complement $(h = 0)$ fixed-width multiplier in Ref. 21, but for $h > 0$, it improves both error performance and area as compared to signed fixed-width multiplier.[18] This error compensation circuit has n inputs and n outputs, consists of $(n-1)$ OR cells and one NOR gate as shown in Fig. 8. Unfortunately, the work proposed in Refs. 22 and 26 still suffers by ripple error compensation circuits, which is not desirable for high speed applications.

Based on Ref. 21, Jou and Wang[23] analyzed error correction circuits and found that several assumptions considered for deriving C_g is not true in real case. They showed the best correction to add to the 2^n column is partial product bits of 2^{n-1} column and it is most suitable for DSP applications due to fast circuitry. It can be noted that this error correction method is same as King and Swartzlander.[18]

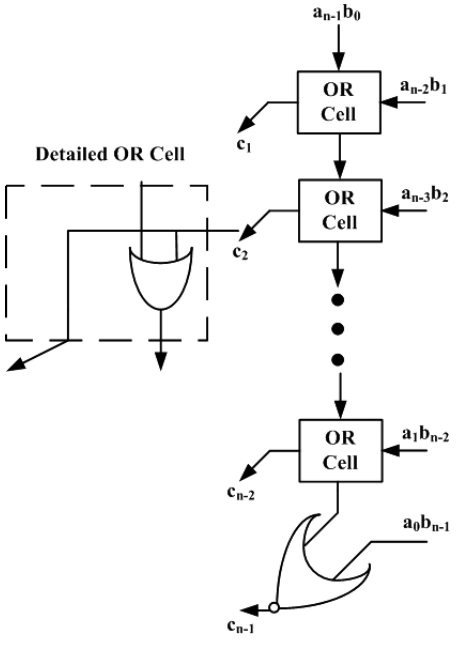

Fig. 6. Jou 99 correction logic for signed multiplier, $w = n$ and $h = 0$.

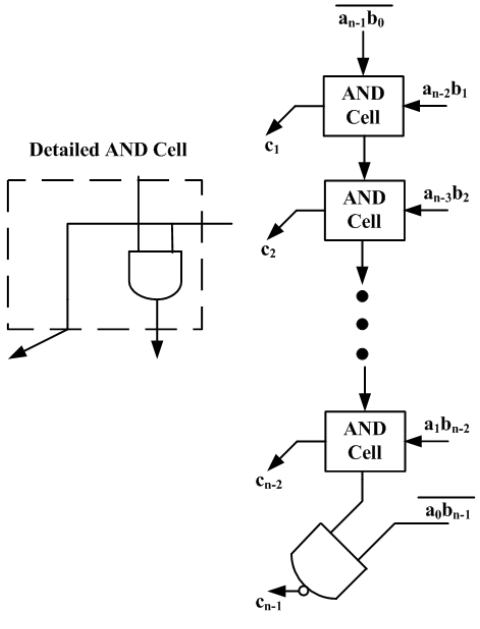

Fig. 7. Van 2000 correction logic for signed multiplier, $w = n$ and $h = 0$.

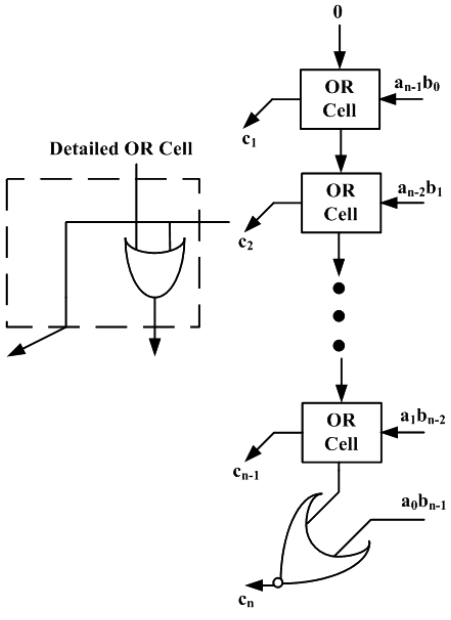

Fig. 8. Van 2005 correction logic for signed multiplier, $w = n$ and $h = 0$.

Curticapean and Niittylahti[24] presented a modified version of the correction circuit of Jou *et al.*[21] for a direct digital frequency synthesizer (DDFM) that uses unsigned fixed-width multiplier. This technique provides good error performances, but computation function is still based on slow ripple architecture. However, the authors[24] have not given any explanation to justify the improved error performances. This error compensation circuit has n inputs and $n-1$ outputs which consist of $(n-2)$ AO cells and one OR gate as shown in Fig. 9.

Stine and Duverne's introduced the hybrid correction method (HCM) for fixed-width multiplier,[25] which takes the advantages of both constant correction[16] and variable correction.[19] This HCM technique provides lower average error and maximum absolute error than both CCM and VCM for fixed-width multiplier.

New error correction circuits for unsigned fixed-width multipliers has been described in Ref. 27 by Strollo *et al.*, either to optimize the maximum absolute error or the mean square error. Unlike the methods[21,22,24] used ripple structure to generate the correction bias value, Strollo *et al.*[27] used tree based compensation structure to compensate the error. Strollo Type I error compensation circuit was used to optimize the maximum absolute error and has n inputs and n outputs which consists of one half-adder (HA), one $n-2$ input NOR gate, and one AND gate as shown in Fig. 10. Strollo Type II error compensation circuit was used to optimize the mean error which has n inputs, $n-1$ outputs and it consists of one full-adder (FA) and one HA as shown in Fig. 11.

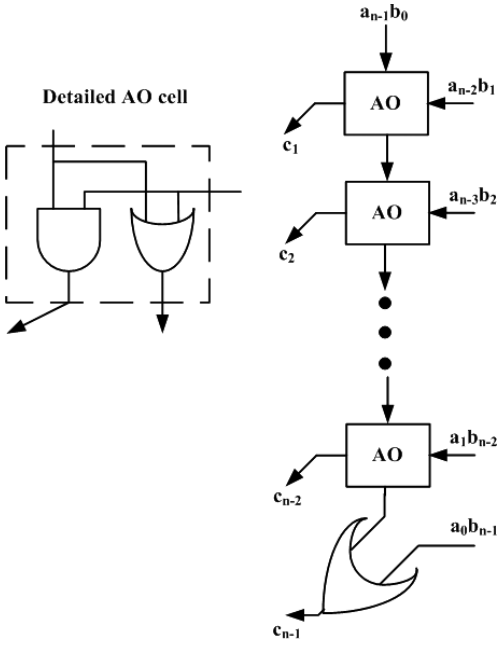

Fig. 9. Curticapean 2001 correction logic for unsigned multiplier, $w = n$ and $h = 0$.

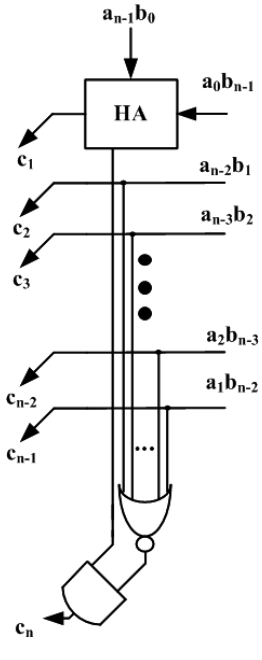

Fig. 10. Strollo Type I correction logic for unsigned multiplier, $w = n$ and $h = 0$.

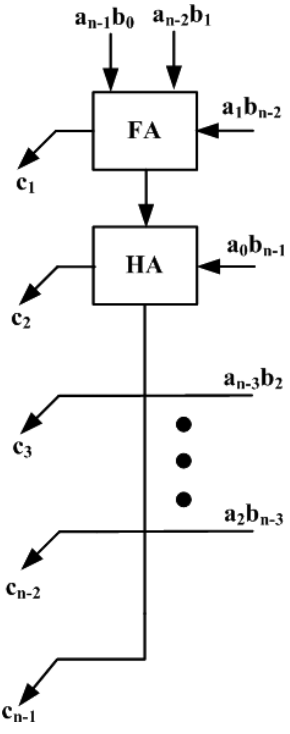

Fig. 11. Strollo Type II correction logic for unsigned multiplier, $w = n$ and $h = 0$.

Liao *et al.*[28] attempted to explain the results obtained in Ref. 22 by analytical method which proposed three carry estimation schemes based on the dependency among the partial products and the inputs. However, proposed circuits are too complex to implement in a practical multiplier and do not improve the performances as compared to Van *et al.* in Ref. 22.

Kuang and Wang[29] proposed two different configurable error compensation circuits for unsigned fixed-width multiplier with minimal modification of the technique presented by Strollo *et al.* in Ref. 27. This correction reduces hardware complexity with respect to Ref. 27. Kuang and Wang Type I error compensation circuit reduces mean square error while increasing the mean error with respect to Type I error compensation circuit in Ref. 27 and has n inputs and $n - 2$ outputs as shown in Fig. 12. On the other hand, Kuang and Wang Type II error compensation circuit obtains lower mean error, but a higher mean square error with respect to Type II error compensation circuit in Ref. 27 and has n inputs and $n - 3$ outputs as shown in Fig. 13. It can be noted that the error compensation circuits,[29] generate less carry signals to the retained adder cells as compared to the other compensation circuits, which can help us to simplify the retained adder cell.

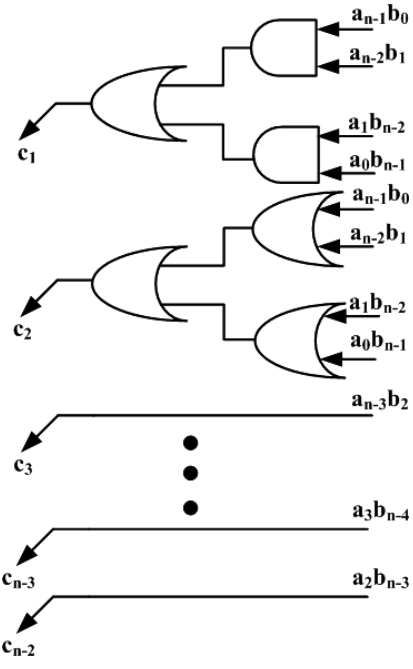

Fig. 12. Kuang and Wang Type I correction logic for unsigned multiplier, $w = n$ and $h = 0$.

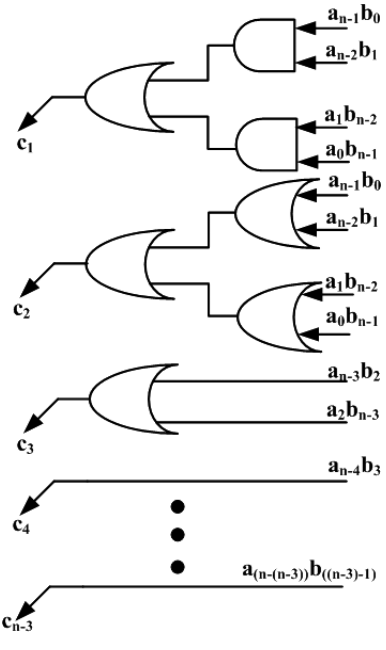

Fig. 13. Kuang and Wang Type II correction logic for unsigned multiplier, $w = n$ and $h = 0$.

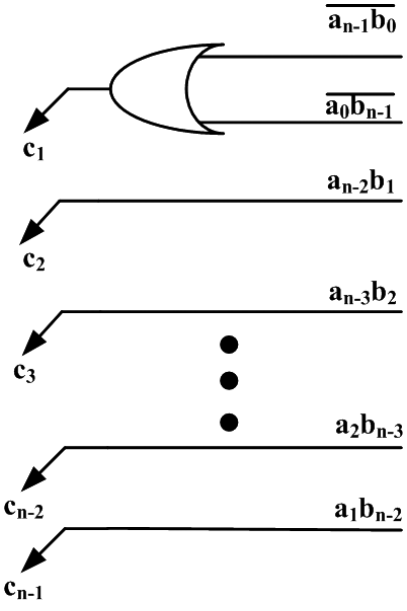

Fig. 14. Wang and Kuang correction logic for signed multiplier, $w = n$ and $h = 0$.

Wang and Kuang[30] proposed a new error compensation circuit for signed fixed-width multiplier to reduce maximum error, mean error, and mean-square error with simple tree based compensation circuit as compared to ripple based error compensation circuits in Refs. 21, 22 and 26. It has n inputs and $n-1$ outputs that consist of only one OR gate as shown in Fig. 14.

Petra *et al.*[31] proposed the optimal compensation function that is analytically derived to minimize the mean square error of the signed and unsigned fixed-width multiplier. Since this optimal compensation function cannot be implemented efficiently in hardware, they introduced a sub-optimal linear compensation function[32] to implement in hardware by performing a drastic quantization of its coefficients, which are approximated by using only single bit.

Garofalo *et al.*[33] demonstrated closed form analytical calculation of the maximum absolute error for the family of fixed-width multiplier proposed in Refs. 27, 31 and 32. This calculation is valid for both signed and unsigned fixed-width multipliers and is valid for every bit width of the multiplier.

The fixed-width multipliers studied in Refs. 27, 29 and 31 are the most precise fixed-width multipliers among the previous fixed-width multipliers. Recently, Wey and Wang[34] proposed a new error compensation circuit by using dual group minor input correction vector (MIC) for unsigned fixed-width multiplier by considering the impact of the most significant column of the LSP part to further enhance the error compensation precision. However, the hardware complexity and delay of the error compensation circuit is increasing as the multiplier input bits increase because the

proposed error compensation circuit mainly constructed by the "outer" partial products.

De Caro *et al.*[35] proposed fixed-width multipliers and multipliers-accumulators with min-max approximation error for applications like function evaluation. In these applications, reducing maximum absolute error is an important parameter than the average error metrics (like mean-square error). Van and Tu[38] introduced reconfigurable and programmable structures in fixed-width multiplier, which allow hardware multiplier architecture to operate in different modes.

Balamurugan *et al.*[55–57] proposed fixed-width multipliers with bypassing technique to further reduce the power consumption. In Ref. 55, dynamic power reduction is achieved by reducing the switching activity of the adder cells at the cost of delay and area. Extended work was presented to reduce the power and delay by using decomposition logic.[56,57]

The fixed-width techniques can also be applied to multiplexer based array multipliers,[39] CSD algorithm,[40] and Booth array multiplier.[41–54] Bough–Wooley array based fixed-width multipliers have been widely studied since long time. Recently, researchers are paying more attention to fixed-width modified Booth multipliers due to its high speed computation and area saving as compared to the fixed-width Bough–Wooley array multipliers. However, most of the variable correction methods developed for fixed-width Bough–Wooley array multiplier cannot be applied for fixed-width modified Booth array multipliers directly to reduce the truncation error.

To overcome this problem, fixed-width Booth multipliers[41–54] with variable error correction method have been proposed to effectively reduce the truncation errors. The fixed-width Booth multipliers[49] having less truncation error as compared to fixed-width Baugh–Wooley array multipliers since a few partial products are truncated after Booth encoding.

Jou *et al.*[42] proposed a low cost compensation bias using linear regression analysis to approximate truncation error part as a first order polynomial. This approach significantly reduce the mean error, however maximum absolute error and mean square error are still large. Cho *et al.*[43] proposed a simple error compensation circuit, which utilizes more information from Booth encoded output to generate the error compensation value. This circuit gives a better error performance with a huge area penalty.

Juang and Hsiao[44] proposed a condition probability based error compensation function rather than time-consuming simulation method as presented in Refs. 42 and 43. However, Juang and Hsiao[44] compensation circuit cannot improve the performance in accuracy as compared with Refs. 42 and 43. Huang *et al.*[45] proposed a self-compensation approach using conditional mean method derived from an exhaustive simulation method, this approach reduces the hardware complexity as compared to Ref. 42 with a slightly increased mean error and almost same hardware complexity as in Ref. 43 with smaller mean error.

Song *et al.*[46] introduced the column information h to provide more choices between accuracy and area cost in fixed-width modified Booth multiplier. Nowadays, it is obvious that trade-off occurs between area-cost and accuracy in low-error multiplier designs. Song *et al.* presented two types (Type-1 and Type-2) of binary threshold derived from the simulation results and a little improvement in accuracy and speed are observed in Type-1 with $h = 0$ as compared with Ref. 42.

Wang *et al.*[47] proposed a high accuracy fixed-width modified Booth multiplier by using an effective error compensation circuit, which is derived from the simulation results. However, the area cost was increased. Li *et al.*[48] proposed a probability estimation bias (PEB) method to replace the time-consuming exhaustive simulation methods. In this way, an area-efficient and low-error PEB circuit was derived based on a simple and systematic procedure.

Chen *et al.*[49] further improved the work of Li *et al.*[48] by using a generalized probabilistic estimation method (GPEB) known as expected probabilistic method. Besides higher accuracy and lower area, the proposed GPEB circuit has more power-efficient as compared with other methods. Chen *et al.*[50] proposed an adaptive conditional-probability estimator in fixed-width Booth multiplier to further improve the accuracy by varying column information h. However, this was achieved at the cost of increased area overhead.

Chen *et al.*[53] proposed a more complex multi-level conditional probability (MLCP) model that achieves higher accuracy with huge area penalty. Unlike other studies, He *et al.*[54] proposed a dynamic error-compensation circuit for a fixed-width Booth multiplier based on probability as well as computer simulation (PACS). Combining the advantages of the two methods the overall error performances can be improved. The PACS method utilizes both expected as well as conditional probability to obtain the highest accuracy. However, there is again a trade-off between the accuracy and area overhead.

This review presents the investigation based on Bough–Wooley array multipliers as well as Booth array multipliers and intended to serve as a suitable reference paper for future work in array based fixed-width multipliers and its related research.

All literature does not cover all the error metrics ($\varepsilon_{m,}\varepsilon_{\max}$ and ε_{mse}) of fixed-width multiplier for signed and unsigned topologies. In this paper, we have presented all the state-of-the art architectures that have been proposed by various researchers in recent years and compared based on novelty, correction method and applications in the Tables 1 and 2. Table 1 describes history of various fixed-width Bough–Wooley array multipliers. From the discussion, it is identified that the correction functions[27,29,31] for fixed-width Bough–Wooley array based multipliers provides better performance for DSP and multimedia applications, on the other hand correction function[35] provides better performance for function evaluation than the other listed methods.

Table 1. History of fixed-width Bough–Wooley array multiplier architectures.

Authors	Novelty	Year	Reduction method	Synthesis/Simulation	Correction method	System	Applications
Lim[15]	New	1992	Truncated	Theoretical	Various	Multiplier	—
Schulte and Swartzlander[16]	New	1993	Truncated	Theoretical	Constant	Multiplier	—
Kidambi *et al.*[17]	New	1996	Truncated	Theoretical	Constant	Multiplier	Filter
King and Swartzlander[18]	New	1997	Truncated	Theoretical	Variable	Multiplier	
Swartzlander Jr, E. E.[19]	Review	1999	Truncated	Theoretical	Various	Multiplier	
Schulte *et al.*[20]	Review	1999	Truncated	Synthesis and Simulation	Various	Multiplier	—
Jou *et al.*[21]	New	1999	Truncated	Theoretical	Variable	Multiplier	
Van *et al.*[22]	New	2000	Truncated	Theoretical	Variable	Multiplier	FIR Filter
Jou, S. J. and Wang, H. H[23]	New	2000	Truncated	Theoretical	Variable	Multiplier	—
Curticăpean, and J. Niittylahti[24]	New	2001	Truncated	Synthesis and Simulation	Variable	DDFS	DDFS
Stine and Duverne[25]	New	2003	Truncated	Xilinx Virtex2	Hybrid	Multiplier	—
Van and Yang[26]	New	2005	Truncated	Chip	Variable	Multiplier	FIR Filter
Strollo *et al.*[27]	New	2005	Truncated	Synthesis and Simulation	Variable	Multiplier	—
Liao *et al.*[28]	New	2006	Truncated	Theoretical	Variable	Multiplier	—
Kuang and Wang[29]	New	2006	Truncated	Synthesis and Simulation	Variable	Multiplier	DWT
Wang, J. P. and S. R. Kuang[30]	New	2007	Truncated	Synthesis and Simulation	Variable	Multiplier	IDCT
Garofalo[1]	Review	2008	Truncated	Synthesis and Simulation	Variable	FIR Filter	FIR Filter
Van and Tu[38]	New	2009	Trun./Recon.	Chip	Variable	Mulitplier	—
Petra *et al.*[31]	New	2010	Truncated	Chip	Variable	MAC	FIR Filter
Chang and Satzoda[39]	New	2010	Truncated	Synthesis and Simulation	Variable	Multiplier	DCT, JPEG
Petra *et al.*[32]	New	2011	Truncated	Chip	Variable	MAC	FIR Filter
Garofalo *et al.*[33]	New	2011	Truncated	Numerical Simulation	Variable	Multiplier	—
Wey and Wang[34]	New	2012	Truncated	Chip	Variable	Multiplier	—
De la Guia Solaz *et al.*[37]	New	2012	Truncated	Chip	Software	System	Biomedical
De Caro *et al.*[35]	New	2013	Truncated	Synthesis and Simulation	Variable	Multiplier MAC	Elementary Function
Wey *et al.*[36]	New	2015	Truncated	Chip	Variable	Multiplier	—

Table 2. History of fixed-width modified Booth array multiplier architectures.

Authors	Novelty	Year	Reduction method	Synthesis/Simulation	Correction method	System	Applications
Jou *et al.*[42]	New	2003	Truncated	Synthesis and Simulation	Variable	Multiplier	Filter
Cho *et al.*[43]	New	2004	Truncated	Synthesis and Simulation	Variable	Multiplier	FIR Filter
Juang and Hsiao[44]	New	2005	Truncated	Conditional probability	Variable	Multiplier	DCT/IDCT, JPEG
Huang *et al.*[45]	New	2006	Truncated	Chip/Simulation	Variable	Multiplier	FFT
Song *et al.*[46]	New	2007	Truncated	Simulation	Variable	Multiplier	FIR Filter
Wang *et al.*[47]	New	2011	Truncated	Synthesis and Simulation	Variable	Multiplier	DWT/IDWT
Li *et al.*[48]	New	2011	Truncated	Chip	Variable	Multiplier	DCT
Chen *et al.*[49]	New	2011	Truncated	Chip	Variable	Multiplier	2-D DCT
Chen and Chang[50]	New	2012	Truncated	Chip	Variable	Multiplier	2-D DCT
Chen[53]	New	2015	Truncated	Chip	Variable	Multiplier	—
He *et al.*[54]	New	2015	Truncated	Chip	Variable	Multiplier	2-D DCT

Table 3. Comparison of established compensation circuits for Bough–Wooley array multiplier.

Authors	UnSigned $h = 0$	Signed $h = 0$	Signed/Unsigned $h > 0$	Observation
Lim[15]	Proposed in the original paper	—	Can be extended to this case	Estimated carry bits from truncation part are generated that will ripple into the most significant part of the product.
Schulte and Swartzlander Jr.[16]	Proposed in the original paper	Can be extended to this case	Can be extended to this case	Expected correction error is computed by combining the expected reduction error and the expected rounding error, which is then used to compute the correction constant.
Kidambi *et al.*[17]	Proposed in the original paper	Can be extended to this case	—	Unlike the other constant correction method, this method compute the expected value by using probabilistic biases and are then fed to the inputs of the retained adder cells.
King and Swartzlander Jr.[18]	Proposed in the original paper	—	Proposed in the original paper	The Variable Correction truncated multiplier is introduced. The error is reduced by using unformed partial product bits in the 2^{n-1} column are added to the 2^n.
Swartzlander Jr.[19]	Review	—	—	Constant correction and variable correction substantially reduce the complexity of rounded multipliers without introducing large amounts of error is reported.
Schulte *et al.*[20]	Review			Reduction in power dissipation and area is achieved by truncated multiplier is explored.
Jou *et al.*[21]	Proposed in the original paper	Proposed in the original paper	Proposed in the original paper	In this work reduced-width multiplier is explored, which has lower product error than that of a fixed-width multiplier and still maintains a low area complexity.
Van *et al.*[22]	Can be extended to this case	Proposed in the original paper	Proposed in the original paper	The general methodology for designing a lower error two's-complement fixed-width multiplier was proposed and applied to speech processing applications.

Table 3. (*Continued*)

Authors	UnSigned $h = 0$	Signed $h = 0$	Signed/Unsigned $h > 0$	Observation
Jou and Wang[23]	Proposed in the original paper	Can be extended to this case	Can be extended to this case	In this work, the authors claimed that new architecture for unsigned multiplier have low error, low area overhead and with a faster operation speed.
Curticăpean and Niittylahti[24]	Proposed in the original paper	—	Can be extended to this case	In this paper, for better error statistics, modified version of the correction circuit presented in Jou *et al.* is used.
Stine and Duverne[25]	—	—	Proposed in the original paper	Hybrid Correction Truncated (HCT) multiplier was reported. It uses both constant and variable correction techniques to reduce the overall error.
Van and Yang[26]	Can be extended to this case	Proposed in the original paper	Proposed in the original paper	In this paper more generalized methodology is available for designing a family of low-error area-efficient fixed-width multipliers for different values of w.
Strollo *et al.*[27]	Proposed in the original paper	Can be extended to this case	Can be extended to this case	A new dual-tree error-compensation network is proposed, which are optimally chosen in order to minimize either the mean-square error or the maximum absolute error.
Liao *et al.*[28]	—	Proposed in the original paper	—	In this paper, three different carry estimation schemes are proposed using an analytical approach to reduce the mean and mean square error.

Table 4. Comparison of established compensation circuits for Bough–Wooley array multiplier continued.

Authors	UnSigned $h = 0$	Signed $h = 0$	Signed/Unsigned $h > 0$	Observation
Kuang and Wang[29]	Proposed in the original paper	—	Can be extended to this case	In this Letter, a simple configurable error-compensation circuit with very low hardware complexity is proposed to minimize either the mean error or the mean-square error.
Wang and Kuang[30]	—	Proposed in the original paper	Can be extended to this case	A very simple error compensation circuit with lower maximum absolute error, mean error and mean-square error for signed fixed-width multipliers were presented.
Garofalo[1]	Review	—		The performances provided by different architectures of fixed-width multipliers when used to implement FIR filters using a single Multiply and Accumulate unit, was reported.
Van and Tu[38]	Can be extended to this case	Proposed in the original paper	—	Pipelined reconfigurable fixed-width multiplication with four useful multipliers under the limited hardware resource is proposed.
Petra *et al.*[31]	Proposed in the original paper	Proposed in the original paper	Proposed in the original paper	The optimal compensation function is analytically calculated, that minimizes the mean square error of the truncated multiplier.
Chang and Satzoda[39]	Proposed in the original paper	Can be extended to this case	—	This paper proposed a new multiplexer based truncation scheme with lower average and mean square errors
Petra *et al.*[32]	Proposed in the original paper	Proposed in the original paper	Proposed in the original paper	The effect of the coefficients quantization in truncated multipliers with linear compensation function is reported.
Garofalo *et al.*[33]	Proposed in the original paper	Proposed in the original paper	—	The analytical formula of the maximum error for the state-of-the-art family of truncated multipliers (LMS) available in literature is presented.

Table 4. (*Continued*)

Authors	UnSigned $h = 0$	Signed $h = 0$	Signed/Unsigned $h > 0$	Observation
Wey and Wang[34]	Proposed in the original paper	—	—	A new error compensation circuit by using the dual group minor input correction vector is proposed to lower input correction vector compensation error.
De la Guia Solaz[37]	Proposed in the original paper	Proposed in the original paper	Proposed in the original paper	A programmable truncated multiplier (PTM), describes a full-precision multiplier, where the elements of the partial product matrix can be disabled through an external control word in a column-wise mode is presented.
De Caro *et al.*[35]	Proposed in the original paper	Proposed in the original paper	Proposed in the original paper	An efficient numerical method to compute the MAE in fixed-width multipliers and MAC is described.
Wey *et al.*[36]	Proposed in the original paper	—	—	A low-error and area-efficient fixed-width RPR-based ANT multiplier design is presented.

Table 5. Comparison of established compensation circuits for modified Booth array multiplier.

Authors	UnSigned $h = 0$	Signed $h = 0$	Signed/Unsigned $h > 0$	Observation
Jou *et al.*[42]	—	Proposed in the original paper	—	The compensation bias is approximated from a linear regression analysis. This approach significantly reduces the mean error, but maximum absolute error and mean-square error is still large.
Cho *et al.*[43]	—	Proposed in the original paper	Can be extended to this case	By using information from the Booth encoder, the truncation error is reduced with the area as a penalty.
Juang and Hsiao[44]	—	Proposed in the original paper	—	Conditional probability based compensation method is introduced. Thus the compensation method does not improve the accuracy than the existing multiplier, because the conditional bits are not chosen well.
Huang *et al.*[45]	—	Proposed in the original paper	—	Self-compensation approach for fixed-width Booth multiplier is proposed by using the conditional mean method to reduce the hardware complexity.
Song *et al.*[46]	—	Proposed in the original paper	Proposed in the original paper	Truncation error is reduced by using two different types of binary threshold and more information from partial products. There is a trade-off between accuracy and area cost.
Wang *et al.*[47]	—	Proposed in the original paper	Can be extended to this case	In this work, simulation based error compensation formula is derived to improve the accuracy of the fixed-width booth multiplier with high speed computation.
Li *et al.*[48]	—	Proposed in the original paper	—	In this work, The probabilistic estimation bias is proposed to replace the time-consuming exhaustive simulation methods with good accuracy performance.

Table 5. (*Continued*)

Authors	UnSigned $h = 0$	Signed $h = 0$	Signed/Unsigned $h > 0$	Observation
Chen *et al.*[49]	—	Proposed in the original paper	Proposed in the original paper	A generalized probabilistic estimation bias (GPEB) is proposed, that minimizes the truncation error, achieves higher accuracy under the same or lower area, compared with the existing works.
Chen and Chang[50]	—	—	Proposed in the original paper	The proposed ACPE provides a high accuracy, mathematical, and flexible compensation function for fixed-width Booth multiplier design and it can be easily applied to the large length multiplier.
Chen[53]	—	—	Proposed in the original paper	A more complex multi-level conditional probability model is proposed to achieve high accuracy at the cost of area overhead.
He *et al.*[54]	—	—	Proposed in the original paper	Overall performance is improved by using a dynamic error-compensation circuit for a fixed-width Booth multiplier based on probability as well as computer simulation.

Fixed-width Booth array multipliers are ideal for high speed applications. Table 2 describes the history of various fixed-width modified Booth multipliers. From the discussion, it is identified that the fixed-width modified Booth multipliers in Refs. 43 and 46 achieve better error performance in terms of the maximum absolute error and the mean-square error when compared with the previous published multiplier in Ref. 42. However, their mean errors are much larger than that of Jou *et al.*[42] The methods in Refs. 42, 46 and 47 improve accuracy; however, the establishment of the compensation value requires excessive simulation time than the designs in Refs. 44, 48, 49 and 53. The highest accuracy is obtained either by using Wang's multiplier[47] or He *et al.*[54] In general, it is obvious that a trade-off occurs between the area-cost and the accuracy in low-error multiplier designs.

It can be noted that every literature does not cover both signed and unsigned topologies and can be applied to the general case $h \geq 0$, while h is a design parameter that can be used to increase the accuracy without changing the weight of the output LSB. In Tables 3–5, the comparisons of established compensation circuits are listed by considering both signed and unsigned topologies with $h \geq 0$.

4. Error Performance of Different Fixed-Width Multipliers

In this paper, we have coded the state of the art fixed-width multipliers available in the Literature by using Verilog HDL code and carried out exhaustive simulations to evaluate the accuracy of the fixed-width multipliers. The accuracy of the fixed-width multipliers are evaluated using error metrics including normalized maximum absolute error ($\varepsilon_{\max}$), normalized mean error (ε_m), and normalized mean-square error (ε_{mse}). Let P be the output of the full-width multiplier and P_t is the output of the FWM, and then error terms are defined as

$$\varepsilon_{\max} = \frac{\text{Max}\{|\text{P} - \text{P}_\text{t}|\}}{2^\text{n}}, \tag{9}$$

$$\varepsilon_m = \frac{\text{Ave}\{(\text{P} - \text{P}_\text{t})\}}{2^\text{n}}, \tag{10}$$

$$\varepsilon_{\text{mse}} = \frac{\text{Ave}\{(\text{P} - \text{P}_t)^2\}}{2^{2\text{n}}}, \tag{11}$$

where "Max" represents maximal operator and "Ave" represents average operator. Note that the higher accuracy in multipliers, the smaller error values ε_m, $\varepsilon_{\max}$ and ε_{mse} are obtained. The error performances of different fixed-width multipliers with $h = 0$ are listed in Tables 6–9. As expected, the PT method is the most accurate fixed-width multiplier and gives best error performance and DT multiplier gives worst error performance in this comparison tables. All the error compensation circuits proposed in the literature for fixed-width multiplier have a goal of achieving PT multiplier accuracy with less area and high speed.

Table 6. Mean errors of fixed-width Bough–Wooley array multipliers (^{*S} = Data apply to signed multiplier only; ^{*U} = Data apply to unsigned multiplier only; Remaining data are valid for both signed and unsigned multipliers).

		$\varepsilon_{\text{mean}}$				
	Architecture	$n = 8$	$n = 10$	$n = 12$	$n = 14$	$n = 16$
$h = 0$	PT	0.0078	0.0024	0.0007	0.0002	0.0001
	DT (Braun)	−1.7510	−2.2502	−2.7501	−3.2500	−3.7500
	DT (BW)	−2.2510	−2.7502	−3.2501	−3.7500	−4.2500
	^{*U}King[18]	0.2490	0.2498	0.2499	0.2500	0.2500
	Jou[21]	−0.6509	−0.6939	−0.7184	−0.7322	−0.7400
	^{*S}Van[22,26]	0.2489	0.2497	0.2499	0.2500	0.2500
	^{*U}Curticapean[24]	0.0324	0.0185	0.0105	0.0059	0.0033
	^{*U}Strollo[27]					
	Type I	−0.1217	−0.1502	−0.1664	−0.1756	−0.1808
	Type II	−0.0166	−0.0159	−0.0157	−0.0156	−0.0156
	^{*U}Kuang_wang[29]					
	Type I	0.0537	0.0544	0.0546	0.0547	0.0547
	Type II	**−0.0088**	**−0.0081**	**−0.0079**	**−0.0078**	**−0.0078**
	^{*S}Wang_Kuang[30]	0.1865	0.1873	0.1874	0.1875	0.1875
	Petra[31]	−0.0166	−0.0159	−0.0157	−0.0156	−0.0156
	^{*U}Wey_Wang[34]	0.0532	0.0885	0.1171	0.1388	0.1549
	De Caro[35] (B = 0)	−0.1217	−0.1502	−0.1664	−0.1756	−0.1808

Table 7. Maximum errors of fixed-width Bough–Wooley array multipliers (^{*S} = Data apply to signed multiplier only; ^{*U} = Data apply to unsigned multiplier only; Remaining data are valid for both signed and unsigned multipliers).

		ε_{max}				
	Architecture	$n = 8$	$n = 10$	$n = 12$	$n = 14$	$n = 16$
$h = 0$	PT	0.5000	0.5000	0.5000	0.5000	0.5000
	DT (Braun)	7.0039	9.0010	11.0002	13.0001	15.000
	DT (BW)	7.0039	9.0010	11.0002	13.0001	15.000
	^{*U}King[18]	1.7227	2.0557	2.3889	2.7222	3.0556
	Jou[21]	2.0117	2.3467	2.6804	3.0139	3.3472
	^{*S}Van[22,26]	1.7227	2.0557	2.3889	2.7222	3.0556
	^{*U}Curticapean[24]	1.5547	1.8887	2.2222	2.5555	2.8889
	^{*U}Strollo[27]					
	Type I	**1.5117**	**1.8467**	**2.1804**	**2.5139**	**2.8472**
	Type II	1.7227	2.0557	2.3889	2.7222	3.0556
	^{*U}Kuang_wang[29]					
	Type I	1.7227	2.0557	2.3889	2.7222	3.0556
	Type II	2.3164	2.6416	2.9729	3.3057	3.6389
	^{*S}Wang_Kuang[30]	1.5547	1.8887	2.2222	2.5555	2.8889
	Petra[31]	1.7227	2.0557	2.3889	2.7222	3.0556
	^{*U}Wey_Wang[34]	1.5078	1.9600	2.2849	2.6098	2.9413
	De Caro[35] (B = 0)	1.5117	1.8467	2.1804	2.5139	2.8472

Table 8. Mean square errors of fixed-width Bough–Wooley array multipliers (*S = Data apply to signed multiplier only; *U = Data apply to unsigned multiplier only; Remaining data are valid for both signed and unsigned multipliers).

		ε_{mse}				
	Architecture	$n = 8$	$n = 10$	$n = 12$	$n = 14$	$n = 16$
$h = 0$	PT	0.0833	0.0833	0.0833	0.0833	0.0833
	DT (Braun)	4.0183	6.3069	9.0976	12.3890	16.1806
	DT (BW)	5.8952	8.6824	11.9727	15.7640	20.0556
	*U King[18]	0.2634	0.3054	0.3472	0.3889	0.4306
	Jou[21]	0.5984	0.6995	0.7804	0.8473	0.9049
	*S Van[22,26]	0.2634	0.3054	0.3472	0.3889	0.4306
	*U Curticapean[24]	0.2338	0.2846	0.3331	0.3796	0.4246
	*U Strollo[27]					
	Type I	0.2354	0.2950	0.3503	0.4017	0.4499
	Type II	0.2160	0.2584	0.3003	0.3420	0.3837
	*U Kuang_wang[29]					
	Type I	0.2127	0.2547	0.2964	0.3381	0.3798
	Type II	0.2304	0.2715	0.3131	0.3547	0.3964
	*S Wang_Kuang[30]	0.2322	0.2742	0.3159	0.3576	0.3993
	Petra[31]	0.2160	0.2584	0.3003	0.3420	0.3837
	*U Wey_Wang[34]	**0.1792**	**0.2275**	**0.2764**	**0.3250**	**0.3727**
	De Caro[35] (B = 0)	0.2322	0.2742	0.3159	0.3576	0.3993

From these circuits, Kuang and Wang[29] unsigned type II architectures have less ε_m than other circuits. However, Petra *et al.*[31] architecture has less ε_m for signed and unsigned fixed-width multiplier than other circuits and it is shown in Table 6. The maximum absolute error ε_{max} is the main parameter to be considered in several practical applications such as function evaluation.[3–6] From the survey it has been identified that Strollo *et al.*[27] Type I architecture and De Caro *et al.*[35] provide better results than the other listed methods and it is shown in Table 7. In most of the DSP and multimedia applications the mean-square error and mean error represents the error metrics, which better describe the multiplier performances. As it can be seen form Table 8, Wey and Wang[34] unsigned fixed-width multipliers have less ε_{mse} than other unsigned multipliers listed in the table. However, for signed fixed-width multiplier it has been identified that Stollo *et al.*[27] Type II, Petra *et al.*,[31] and De Caro *et al.*,[35] provide better results than other listed methods.

Table 9 shows a comparison of error performance of various fixed-width modified Booth multipliers. All the works in Table 9 use exhaustive simulations to produce the compensation fit function except Juang[44] and Li *et al.*,[48] where the compensation functions generated mathematically. The compensation fit functions established from exhaustive simulations that consume long time, especially for larger n, because the simulation time increases exponentially. He *et al.*[54] developed the compensation function based on probability as well as computer simulation. Many multimedia and DSP applications we have to maintain the error distribution not only be symmetric

Table 9. Error performance of different fixed-width modified Booth array multipliers.

		$h = 0$				
	Multiplier	$n = 8$	$n = 10$	$n = 12$	$n = 14$	$n = 16$
$\varepsilon_{\text{mean}}$	PTM[Booth]	0.0078	0.0024	0.0007	0.0002	0.0001
	DTM[Booth]	1.5010	1.8752	2.2500	2.6250	3.0000
	Jou[42]	0.0010	0.0002	0.0001	0.0000	0.0000
	Cho[43]	0.1328	0.1211	0.1270	0.1240	0.1254
	Juang[44]	−0.0825	−0.0799	−0.0767	−0.0753	−0.0739
	Song[46]	0.0207	0.0077	0.0029	0.0011	0.0003
	Wang[47]	0.0078	−0.0039	0.0019	−0.0009	0.0006
	Li[48]	0.0000	0.1875	−0.1248	0.0625	−0.2499
	He[54]	0.0078	−0.0039	0.0019	−0.0009	0.0006
ε_{max}	PTM[Booth]	0.5000	0.5000	0.5000	0.5000	0.5000
	DTM[Booth]	4.0000	5.0000	6.0000	7.0000	8.0000
	Jou[42]	1.7305	2.1299	2.5300	2.9300	3.3300
	Cho[43]	1.5000	1.5000	2.0000	2.0000	2.5000
	Juang[44]	1.9180	2.2607	3.0867	3.4201	3.9175
	Song[46]	1.7320	2.1027	2.4711	2.9300	3.3280
	Wang[47]	1.1680	1.5000	1.6667	2.0000	2.1667
	Li[48]	1.5000	2.0000	2.0000	2.0000	2.5040
	He[54]	1.5000	2.0000	2.0000	2.0000	2.1667
ε_{mse}	PTM[Booth]	0.0833	0.0833	0.0833	0.0833	0.0833
	DTM[Booth]	2.6880	4.0563	5.7068	7.6390	9.8525
	Jou[42]	0.2715	0.3368	0.4019	0.4670	0.5321
	Cho[43]	0.1664	0.1713	0.1950	0.2088	0.2235
	Juang[44]	0.2767	0.3148	0.3589	0.4017	0.4477
	Song[46]	0.2502	0.3285	0.3971	0.4642	0.5271
	Wang[47]	0.1367	0.1542	0.1671	0.1821	0.1961
	Li[48]	0.1831	0.2460	0.2500	0.2599	0.3462
	He[54]	0.1367	0.1542	0.1671	0.1821	0.1961

but also centralize in zero error as much as possible in order to achieve high accuracy. As it can be seen from Table 9, both Wang *et al.*[47] and He *et al.*[54] have smaller mean error as well as mean-square error, which is most desirable for any DSP applications. However, Wang *et al.*[47] method is limited to 32-bits.

5. Conclusion

Fixed-width multipliers can be utilized for DSP and multimedia applications to minimize the power consumption by disabling or eliminating parts of the multiplier which results in low switching activity, but introduces certain error in the multiplier output.

Post-truncated multiplier is the most accurate approach but require large circuit area. Direct-truncated multiplier is proposed to reduce area overhead, but causes more error in the output. All these studies are done to find the reasonable balance

between area overhead and accuracy. Two different correction techniques, namely constant correction technique and variable correction technique are proposed to compensate the error introduced in the fixed-width multipliers with minimal correction logic circuits. Unfortunately, constant correction techniques were inefficient in terms of approximation error. On the other hand, the variable correction techniques proposed to date, significantly improving accuracy.

As there are different variable correction methods are available for fixed-width multipliers to optimize error performance, it is quite difficult to conclude that a particular method is suitable for all the applications. In the fixed-width multipliers, researchers introduces a design parameter h, which is varying from $h = 0$ to $h = n$, to help the designer to trade-off between the accuracy and area. The main trade-off effort for fixed-width multiplier design is finding a compensation function that is efficiently implemented in hardware, and provides a correction value more close to the PT method. The selection can be made based on circuit complexity, speed, error performance and its applications as described in the Tables 1–9. In this paper, error performances of all the analyzed fixed-width multipliers are experimentally computed through exhaustive simulations for $n \leq 16$ and $h = 0$, since the simulation time increases as $O(2^{2n})$, requiring an unreasonable amount of CPU time when n increases. The observations listed in the table will serve as a guide for researchers to select appropriate correction techniques for their applications.

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