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Geometry-Based Crosstalk Reduction in CNT Interconnects*

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This paper proposes novel triangular cross-sectioned geometry of carbon nanotube (CNT) bundles for crosstalk and delay reduction in CNT bundle interconnects for VLSI circuits. First, we formulate the equivalent single conductor (ESC) transmission line models of the interconnects. Through SPICE analysis of the ESC circuits, we find the propagation delays of the proposed CNT bundles. Next, we model the capacitively coupled interconnects for crosstalk analysis. It is found that the coupling capacitance of triangular CNT bundle is 29% lesser than the traditionally used square CNT bundles. Further, the crosstalk-induced delay of triangular interconnects is found to be 30% lesser when compared to square bundle interconnects. The reduction in delay is found to increase as the number of CNTs in the bundle increases. So, we suggest that triangular CNT bundles are the most suitable candidates as global interconnects.

Keywords: Carbon nanotubes; interconnects; geometry; crosstalk; delay.

1. Introduction

Performance and reliability of future VLSI circuits is a major issue in electronics industry.[1] Ever since carbon nanotubes (CNTs) were discovered in 1991, they have gained a prominent place in nanoelectronics research especially as channel material in FETs as well as metallic interconnections in integrated circuits (ICs).[2–4] Metallic single-walled CNTs (SWCNTs), multi-walled CNTs (MWCNTs) and mixed CNT bundles were modeled as interconnects in ICs.[5,6] Further, it was experimentally shown that individual MWCNTs can indeed act as interconnects up to 1.02 GHz.[7] The researchers had done experiments using MWCNTs as interconnects in 256 ring

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oscillators that were fabricated at 0.25 μm CMOS technology. Recent work in modeling of CNT bundles as VLSI interconnects reveals that adjacent interconnects suffer from crosstalk especially during out of phase transitions of the input signals.[6,8] This crosstalk induces a capacitive delay characterized by a coupling capacitance. In long global interconnects whose lengths range from 500 μm to tens of millimeters, this capacitive coupling will be very high and is a major factor that contributes to the propagation delay in wires.[8] For copper interconnects, this capacitive coupling was reduced by using multiple dielectric materials as the cladding and etch stop layers, as well as by separating adjacent wires by a safer distance. However, as the technology progresses to nanometer scale, using large separations by multiple dielectrics is becoming a less feasible option.[1] In the case of CNTs, bundles of CNTs are used instead of single CNTs as interconnects since the intrinsic quantum resistance associated with a single CNT is very high. It is equal to $R_Q = h/4e^2 = 6.45\,\text{k}\Omega$ for two conducting channels; h being the Planks constant and e being the electron charge. However, it is seen that the bundle geometry plays an important role in determining the performance of CNT bundle interconnects. For global interconnects, the bundle width and height are scaled up to meet the requirements of high bandwidth and frequencies.[9] However, this is done at the expense of increased wire resistance at long lengths as well as high quantum and coupling capacitances at large wire cross-sectional area. Recent work on temperature-dependent crosstalk analysis of bundled SWCNT interconnects shows that the performance of SWCNT bundles approaches to that of copper interconnects at global interconnect lengths.[10] Another work shows that multilayer Graphene nano ribbons (MLGNR) and MWCNT interconnects have propagation delays of the order of hundreds of nano seconds for global interconnect lengths.[11] Even though buffering of signals at global level is a good option,[12,13] it is more attractive if we can improve the performance at the interconnect level itself so that, the number of buffers can be reduced further and chip area can be saved.

In this paper, we address the reliability issues of global interconnects by proposing geometry-induced crosstalk and delay reduction methods in bundled CNT interconnects, for the first time. For that, we propose a novel triangular-shaped bundle geometry of CNT bundle interconnects such that the crosstalk-induced delay of coupled interconnects is minimum. We analyze the dynamic crosstalk behavior of the interconnects at in-phase and out-of-phase scenarios by considering them as capacitively coupled interconnects placed on a grounded substrate and by modeling them using a driver-interconnect-load (DIL) setup. We perform transient analysis using SmartSPICE to study the crosstalk-induced delay at various lengths of 500, 1000, 1500 and 2000 μm. We show that the coupling capacitance between triangularly arranged bundles is minimal and hence the crosstalk-induced delay is also minimal compared to traditionally used square CNT bundle interconnects.

2. CNT Bundle Geometries

Bundled CNT interconnects are proposed as ideal candidates for future ultra deep submicron (UDSM) technologies.[5] Traditionally, copper interconnects were treated as rectangular or square cross sectioned interconnects which is essentially true for dual damascene CMOS process technologies.[5] On the other hand, CNTs are grown first on a substrate and then densified into vertical or horizontal pillars.[14] It is shown that the metal contact, on which CNTs are grown, can be patterned according to the bundle width.[15]

Till date, no work has reported alternate geometries for CNT bundle interconnects. All the existing works on CNT bundle interconnect modeling use square or rectangular form as shown in Fig. 1(a) of bundles as they are easy to fabricate and meet the W/L aspect ratio requirements stated by the ITRS. However, modification of wire geometry of copper interconnects was done by Ciofi *et al.*[16] They have proposed an interconnect geometry where the line width is decreased by a certain extent to reduce the crosstalk. Wang and co-workers[17] have formed 'V'-shaped trenches by dry etching on silicon substrates for device applications. Another work by Smith and his team[18] showed fabrication of V-shaped grooves coated with gold on SiO_2 substrate for optical plasmon waveguides in SoCs. These developments motivated us to consider the possibility of using CNTs in triangular bundle form as shown in Fig. 1(b) to reduce crosstalk in VLSI circuits. We came up with this type of geometry of CNT bundles keeping in mind that coupling capacitance between adjacent bundle interconnects must be minimal. This is essential to attain least possible crosstalk.

Fabrication of the proposed triangular CNT bundles can be achieved by forming V-shaped groves on a SiO_2 substrate by lithography process. Metal electrodes which can be made of gold/tungsten must be formed on either sides of the groves to guide the dielectrophoretic assembly of CNTs between them.[19] Then, the substrate must

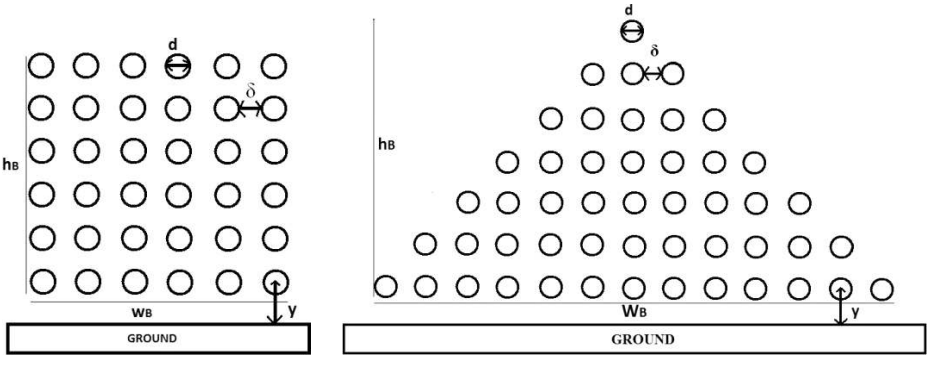


Fig. 1. CNT bundle geometries considered in this paper (a) square CNT bundle and (b) triangular CNT bundle.

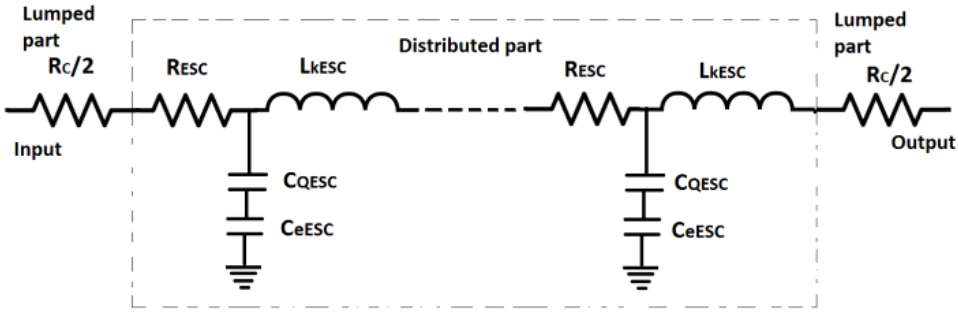


Fig. 2. ESC model of CNT bundle interconnects.

be placed in a solution like dichlorobenzene where CNTs can be dispersed in it. An alternating voltage of 20 V peak-to-peak must be applied at 500 kHz between the electrodes. CNTs align themselves neatly between the electrodes. Finally, the top metal contact can be deposited at either ends of the CNT bundles and the remaining contact metal, if any, can be etched away. As the trenches are in V-shape, the CNT bundle geometry will be V-shaped or inverted triangular in geometry. The International Technology Roadmap of Semiconductors (ITRS) specifications for interconnects is discussed in the ITRS 2013 Edition of Interconnect Summary Chapter.[1] In coupled triangular CNT bundle interconnects, the inter-CNT distance varies optimally while maintaining the overall bundle distance within the ITRS requirements as shown in Fig. 2. The ITRS-predicted dimensional parameters for the year 2013 are listed in Table 1.

For square CNT bundles as shown in Fig. 1(a), the number of CNTs along the width is nW and number of CNTs along the height is nH. The total number of CNTs, n_{SB} is given by

$$n_{SB} = n_W \times n_H \,. \tag{1}$$

Hence, the width w_B and height h_B of the bundle are given as

$$w_B = n_W \times D + (n_W - 1) \times \delta \,, \tag{2}$$

$$w_H = n_H \times D + (n_H - 1) \times \delta \,, \tag{3}$$

Table 1. International Technology Roadmap of Semiconductors (ITRS) 2015 data for 20 nm Technology node interconnects.[1]

Parameter	Intermediate wires	Global wires
Min. Wire pitch (nm)	34	51
Min. half pitch (nm)	16	26
Thickness, H (nm)	100	125
Aspect ratio (W/L)	2	2.34
V_{DD} (volts)	0.7	0.8

where δ is the van der Vaals gap equal to 0.34 nm. We consider the arrangement of CNTs in columns rather than the one described previously in the literature[6] such that the total number of CNTs in both square as well as triangular bundles is same, thereby making the analysis easy and comparable. Moreover, our CNT bundle model can be practically realized by a bottom-up approach, where CNTs can be deposited on a substrate by dielectrophoresis method and metal contacts can be fabricated on either sides. For the triangular bundle as shown in Fig. 1(b), considering the fact that the number of CNTs along each row is odd, the total number of CNTs in the bundle n_{TB} is given as

$$n_{TB} = (n_S \times n_B) - [n_S \times (n_S - 1)]\,, \tag{4}$$

where n_S is the number of CNTs along the side and n_B is the number of CNTs along the base of the triangular bundle. So, for the sake of simplified analysis, we consider $n_{SB} = n_{TB}$. The values of n_S and n_B are considered based on the CNT diameter and the technology node that is used as per ITRS recommendations. In the following sections, we consider different values of these two parameters and explain them too.

3. Equivalent Single Conductor (ESC) Model

Equivalent single conductor (ESC) models are derived for resistance, capacitance and inductance of the CNT bundles considered in this paper. These parameters are dependent on the number of conducting channels in a CNT as well as the number of metallic CNTs in a bundle. Recent advancements in the fabrication process show that metallic (or semiconducting) CNTs can be segregated into a bundle form using dielectrophoresis.[19] So, we consider in this paper that all the CNTs in the bundle are metallic, instead of considering only one-third as metallic which is being done traditionally. This makes our analysis unique with respect to previous analyses reported in the literature.[6,8,10] The ESC parameters of CNT bundles that was modeled by us earlier is considered here.[20] The transmission line equations of the voltage and current through an SWCNT bundle interconnect are given as

$$\frac{\partial V(z,t)}{\partial z} + L\frac{\partial I(z,t)}{\partial t} + RI(z,t) = 0\,, \tag{5}$$

$$\frac{\partial I(z,t)}{\partial z} + C\frac{\partial V(z,t)}{\partial t} = 0\,. \tag{6}$$

Considering an individual CNT in a SWCNT bundle, the number of conducting channels that contribute to its electrical conduction is given as

$$N_i = \begin{cases} aDT_i + b, & \text{if } D_i > d_T/T\,, \\ 2, & \text{if } D_i < d_T/T\,, \end{cases} \tag{7}$$

where T is temperature in kelvin, D_i is the diameter of the ith shell, $a = 3.87 \times 10^{-4}$ $\text{nm}^{-1}\text{K}^{-1}$, $b = 0.2$ and $d_T = 1300$ nmK. The interconnect resistance is dependent on

its effective mean free path λ_{eff} (MFP) as discussed in Ref. 23. The factors that affect λ_{eff} are the optical phonon and acoustic phonon scattering mechanisms which have different scattering MFPs at different ambient temperatures. The MFP due to acoustic phonons can be given as

$$\lambda_{\text{AC}} = \lambda_{\text{AC.300}}\left(\frac{300}{T}\right), \tag{8}$$

where $\lambda_{\text{AC.300}}$ is the acoustic phonon MFP at 300 K which is roughly 1.6 m. The second contribution to λ_{eff} is the optical phonon scattering. So, both optical absorption ($\lambda_{\text{OP.abs}}$) and optical emission ($\lambda_{\text{OP.ems}}$) need to be considered which can be given as

$$\lambda_{\text{OP.abs}} = \lambda_{\text{OP.300}}\left(\frac{N_{\text{OP}}(300)+1}{N_{\text{OP}}(T)}\right), \tag{9}$$

$$\lambda_{\text{OP.ems}} = \frac{1}{\lambda^{\text{fld}}_{\text{OP.ems}}} + \frac{1}{\lambda^{\text{abs}}_{\text{OP.ems}}}, \tag{10}$$

$$\lambda^{\text{fld}}_{\text{OP.ems}}(T) = \frac{\hbar\omega_{\text{OP}}}{eV_{\text{dd}}}l + \left(\frac{N_{\text{OP}}(300)+1}{N_{\text{OP}}(T)+1}\right)\lambda_{\text{OP.300}}, \tag{11}$$

$$\lambda^{\text{abs}}_{\text{OP.ems}}(T) = \lambda_{\text{OP.abs}}(T) + \left(\frac{N_{\text{OP}}(300)+1}{N_{\text{OP}}(T)+1}\right)\lambda_{\text{OP.300}}, \tag{12}$$

where $\lambda^{\text{abs}}_{\text{OP.ems}}$ is the optical emission MFP after absorption, $N_{\text{OP}}(T) = \frac{1}{[\exp(\hbar\omega_{\text{OP}}/K_BT)-1]}$, $\lambda^{\text{fld}}_{\text{OP.ems}}(T)$ is the former optical emission MFP event, $\hbar_{\text{OP}}$ is the optical energy (0.18 eV) and $\lambda_{\text{OP.300}}$ is the spontaneous optical emission at 300 K which is roughly 15 nm. So, the effective MFP λ_{eff} can be given as

$$\frac{1}{\lambda_{\text{eff}}(T)} = \frac{1}{\lambda_{\text{AC}}} + \frac{1}{\lambda_{\text{OP.abs}}} + \frac{1}{\lambda_{\text{OP.ems}}}. \tag{13}$$

Considering these facts, the MFP and temperature-dependent resistance of a CNT bundle can be given as

$$R_b(T) = \frac{R_{\text{SWCNT}}}{n_B} = \begin{cases} \dfrac{R_C + R_Q}{n_B} & \text{for } l < \lambda_{\text{eff}} \\ \dfrac{R_C + R_S}{n_B} & \text{for } l > \lambda_{\text{eff}} \end{cases}, \tag{14}$$

where n_B is the total number of CNTs in a bundle. The temperature-dependent expressions of the ESC inductance of a CNT bundle can be given as

$$L^b_{\text{ESC}}(T) = \frac{L_m + (L_k/N)}{n_B}, \tag{15}$$

where L_m and L_k are the magnetic and kinetic inductances CNT. Similarly, the effective capacitance of a CNT bundle placed on a ground plane is the series

combination of the electrostatic and quantum capacitances of the CNT bundle and can be expressed as

$$C^b_{\mathrm{ESC}}(T) = \frac{C^b_E \dot{C}^b_Q}{C^b_E + C^b_Q}\,. \tag{16}$$

The electrostatic capacitance of the bundle is calculated by considering only the outer CNTs in the bundle as the inner CNTs are not capacitively coupled to the substrate due to the shielding effect of the outer CNTs. It must be noted that the ESC parameters for both square and triangular CNT bundles are same as the number of CNTs in the bundles. However, the electrostatic capacitance between the ground and the interconnect will change as the number of CNTs facing the ground varies for both types of bundle interconnects. Further, the coupling capacitance between adjacent coupled interconnects will change as the distance between the corresponding CNTs will differ as depicted in Fig. 2.

4. Transient Analysis

We use a DIL setup as shown in Fig. 3 to perform transient analysis.

We consider the ASU Predictive Technology Model (PTM) library[21] based inverter as driver at 20 nm technology node. After considering the appropriate ESC parameters for the interconnects, we perform transient analysis by applying a pulsed signal to the DIL setup. Table 2 shows the number of CNTs per bundle and the number of CNTs facing the ground for both square and triangular CNT bundle interconnects. From the results of the transient analysis of Fig. 4, it is seen that the electrostatic coupling capacitance, even though an order of magnitude lesser than the quantum capacitance, impacts the propagation delay of the interconnects. We carried out the simulation considering 36 CNTs, each CNT of 2 nm diameter.

As evident from Fig. 4(a), the propagation delay is slightly higher for triangular interconnects compared to square interconnects. The difference in delay between square and triangular bundles is 0.4 ns at 500 μm, 1.0 ns at 1000 μm, 1.3 ns at 1500 μm and 1.5 ns at 2000 μm. The main reason behind the higher delay for triangular bundle particularly at 2000 μm is the contribution of length-dependent

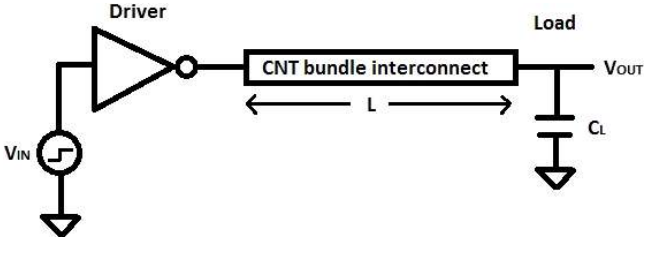


Fig. 3. DIL setup.

Table 2. Number of CNTs in square and triangular bundles.

No. of CNTs in the bundle ($n_{SB} = n_{TB}$)	No. of CNTs facing ground in	
	Square bundle	Triangular bundle
36	6	11
49	7	13
64	8	15
81	9	17
100	10	19

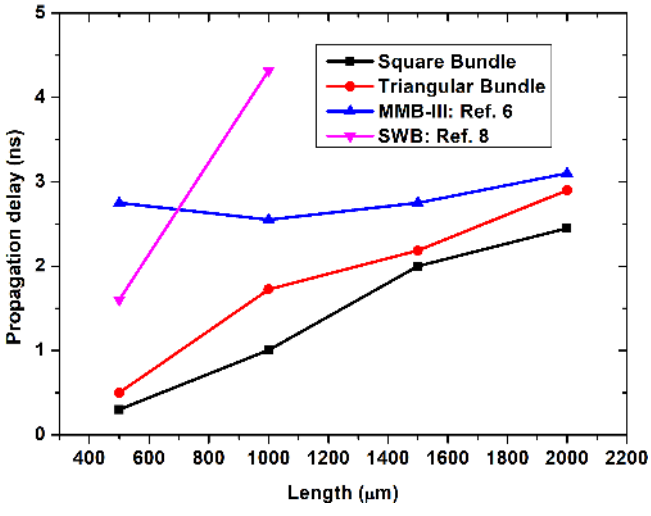


Fig. 4. Propagation delay of square and triangular bundled CNT interconnects compared with other models from the literature.

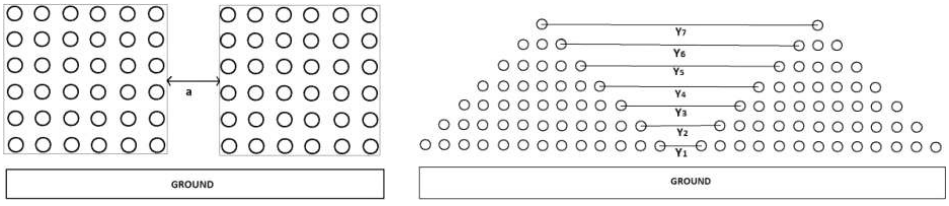
quantum capacitance of 28.8 pF and the electrostatic capacitance of 660 fF, which is highest among other lengths.

5. Crosstalk in Coupled Interconnects

We design the global interconnects for various number of CNTs in the bundle as listed in Table 2. Figure 5 shows coupled CNT bundle interconnects of square and triangular cross section. The two coupled lines are characterized as aggressor and victim lines. The coupling capacitance, C_C, is given as

$$C_C = \frac{2\pi\epsilon}{\cosh^{-1}\frac{y}{d}}, \tag{17}$$

where d is the diameter of the CNT, y is the center to center distance between corresponding CNTs in aggressor and victim lines. The distance between



(a) (b)

Fig. 5. Coupled CNT bundle interconnects of (a) square geometry and (b) triangular geometry.

corresponding CNTs in coupled triangular bundles is given as

$$Y_n = 2(d + \delta) + Y_{n-1}\,, \tag{18}$$

where $n = 1, 2, 3$, d is the diameter of the CNT and δ is the van der Vaals gap of 0.34 nm. So, for triangular CNT bundles, y can be replaced by Y_n in Eq. (17) to get

Table 3. Equivalent single conductor parameters.

				C_{eESC} (fF)	
Length (μm)	R_{ESC} (kΩ)	L_{ESC} (μH)	C_{QESC} (pF)	Square bundle	Triangualr bundle
500	89.580	0.111	7.2	90	165
1000	179.16	0.222	14.4	180	330
1500	268.74	0.333	21.6	270	495
2000	358.32	0.444	28.8	360	660

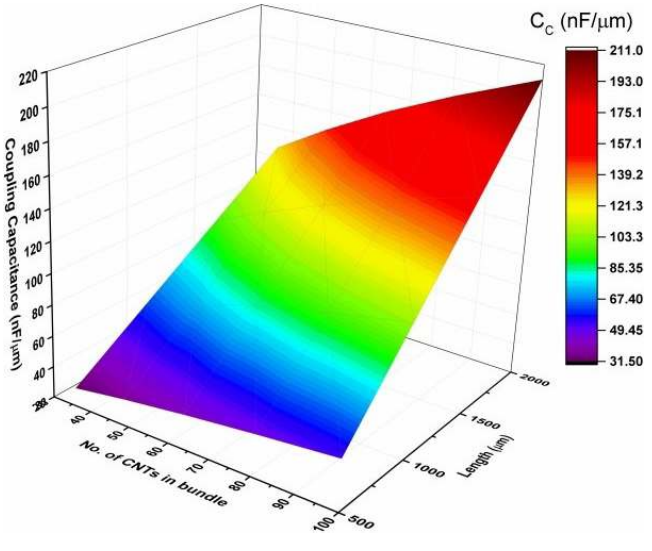


Fig. 6. Coupling capacitance of square bundle at various lengths and number of CNTs in bundle.

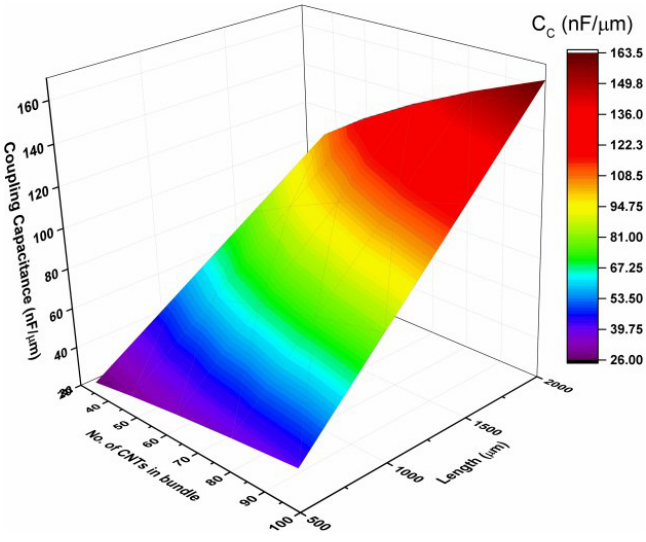


Fig. 7. Coupling capacitance of triangular bundle at various lengths and number of CNTs in bundle.

the capacitance values. Table 3 outlines the ESC parameter values that are calculated for 36 CNTs in a bundle. Similarly, we extend the calculations for 49, 64, 81 and 100 CNTs in a bundle, respectively. The coupling capacitance calculated for both types of bundles at various bundle lengths and number of CNTs in the bundles is shown in Figs. 6 and 7.

We found that the coupling capacitance from Eq. (8) for triangular bundle coupled interconnects is 29.4% lesser than the square bundle coupled interconnects.

6. Performance Analysis

SmartSPICE simulations are done to analyze the impact of crosstalk-induced delay for both the types of coupled interconnects. The simulation setup that we have made for SmartSPICE involves creation of the net-list of the proposed DIL model. The DIL model contains an inverter as the driver and the lumped as well as distributed RLC parameters of the interconnect. The FinFET-based inverter is made of an nFET and a pFET. We use 20 nm FinFET library cards provided by PTM.[21] For 20 nm technology node, we take the V_{dd} values from Table 1, i.e., 0.7 V for intermediate and 0.8 V for global interconnects. Simulations are carried out at room temperature.

Figure 8 shows capacitively coupled interconnects that are modeled as per DIL setup. We energize the wires using a 1 V pulsed signal for analysis. Various switching scenarios viz. in-phase and out-of-phase are considered. We consider the load capacitance $C_L = 10$ aF as we consider minimum-sized driver and load in our simulations.[5] This is because the interconnect RLC will be dominating over the RC values

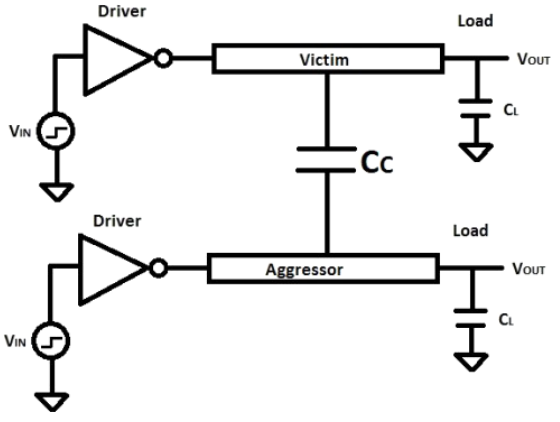


Fig. 8. Schematic of capacitively coupled interconnects.

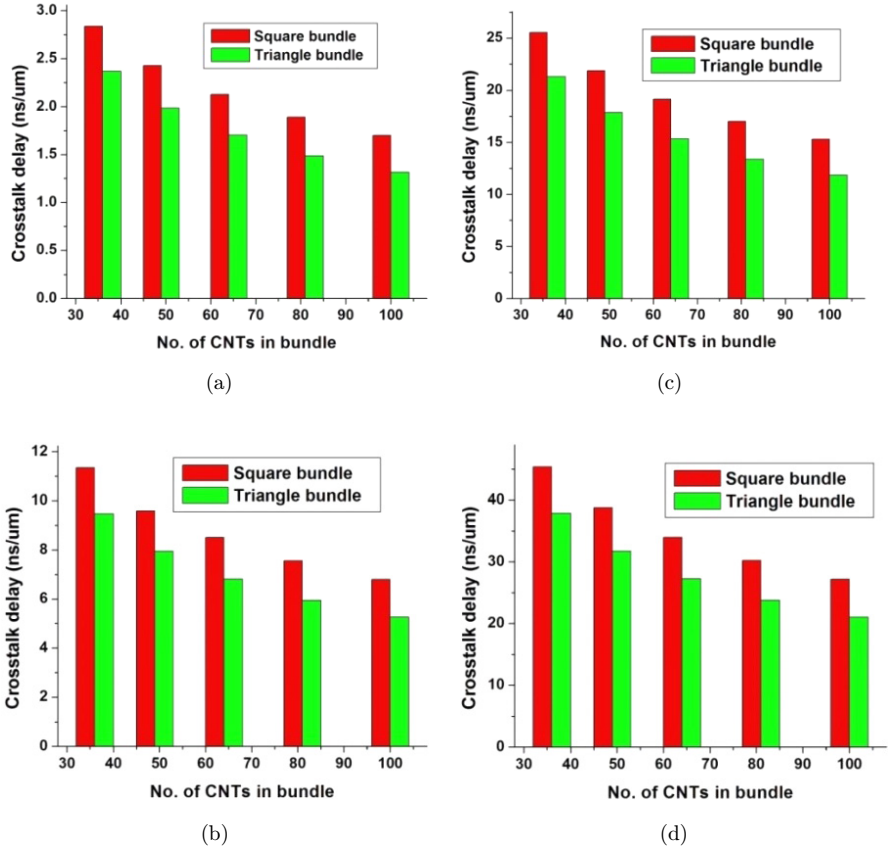


Fig. 9. Crosstalk-induced delay for square and triangular CNT bundle interconnects for lengths of (a) 500 μm, (b) 1000 μm, (c) 1500 μm and (d) 2000 μm.

of the driver/load so that the delay is more dependent on the interconnect parasitics. We carried out the analysis at global interconnect lengths of 500, 1000, 1500 and 2000 μm. We consider Miller capacitance effects as it is demonstrated that in simultaneously switching lines, the line-to-ground capacitance is affected by the type of switching transition.[22] When one line is switching and the other line is idle, the Miller capacitance is equal to coupling capacitance, C_C. During in-phase transitions, considering that switching events track each other perfectly, the Miller capacitance is zero. During out-of-phase switching, maximum coupling occurs between the lines. So, the Miller capacitance is $2*C_C$. Considering these effects, we perform the analysis of crosstalk-induced delay. Figure 9 shows the crosstalk-induced delay of both square and triangular CNT bundle interconnects at lengths of 500, 1000, 1500 and 2000 μm. It was found that the crosstalk-induced delay is less for triangular bundle interconnects at all lengths. The least possible delay improvement of triangular bundles over square bundles is 19.6% for 36 CNTs in a bundle and the maximum improvement was 29.5% for 100 CNTs in a bundle as shown in Fig. 10. The main reason for this improvement can be attributed to the reduction in the coupling capacitance between the adjacent triangular CNT bundle interconnects. Also, the increase in delay improvement for larger bundles is due to the fact that more numbers of CNTs are farther and less coupled than for the smaller bundles. This again is more advantageous when compared to larger square CNT bundles. Very recent developments like high speed subthreshold interconnects[23] can be used to extend this work in the future.

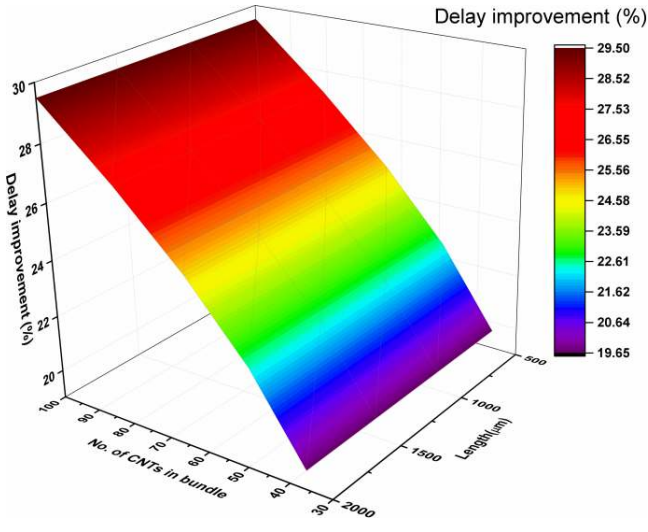


Fig. 10. Delay improvement of triangular interconnects over square interconnects for various no. of CNTs in a bundle and at various lengths.

7. Conclusions

We had studied the influence of geometry on the crosstalk-induced delay in coupled CNT bundle interconnects. We found that for triangular CNT bundle interconnects, the coupling capacitance is 29% lesser than square CNT bundle interconnects. Further, we had carried out simulations of ESC models of interconnects using a DIL setup. We found that the crosstalk-induced delay is 30% less for a triangular bundle compared to square bundles at lengths of 500, 1000, 1500 and 2000 μm. These observations suggest that triangular CNT bundle interconnects can replace traditionally proposed square/rectangular CNT bundle interconnects for better performance in futuristic ICs.

References

1. International Technology Roadmap for Semiconductors, http://www.itrs2.net/itrs-reports.html (2015).
2. P. Uma Sathyakam and P. S. Mallick, Carbon nanotube interconnects with air-gaps: Effect on thermal stability, delay and area, *J. Nano Res.* **48** (2017) 29–37.
3. P. U. Sathyakam and P. S. Mallick, Towards realisation of mixed carbon nanotube bundles as VLSI interconnects: A review, *Nano Commun. Netw.* **3** (2012) 175–182.
4. A. D. Franklin and Z. Chen, Length scaling of carbon nanotube transistors, *Nat. Nanotechnol.* **5** (2010) 858–862.
5. A. A. Vyas, C. Zhou and C. Y. Yang, On-chip interconnect conductor materials for end-of-roadmap technology nodes, *IEEE Trans. Nanotechnol.* **17** (2018) 4–10.
6. M. K. Majumder, P. K. Das and B. K. Kaushik, Delay and crosstalk reliability issues in mixed MWCNT bundle interconnects, *Microelectron. Reliabil.* **54** (2014) 2570–2577.
7. G. F. Close, S. Yasuda, B. Paul, S. Fujita and H.-S. P. Wong, A 1 GHz integrated circuit with carbon nanotube interconnects and silicon transistors, *Nano Lett.* **8** (2008) 706.
8. M. K. Majumder, P. K. Das, V. R. Kumar and B. K. Kaushik, Crosstalk induced delay analysis of randomly distributed mixed CNT bundle interconnect, *J. Circuits Syst. Comput.* **24** (2015) 1550145.
9. S. Zhao and Z. Pan, Bandwidth expanding technology for dynamic crosstalk aware single-walled and multi-walled carbon nanotube bundle interconnects, *Microelectron. J.* **78** (2018) 101–113.
10. A. Alizadeh and R. Sarvari, Temperature-dependent comparison between delay of CNT and copper interconnects, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **24** (2016) 803.
11. V. R. Kumar, M. K. Majumder, A. Alam, N. R. Kukkam and B. K. Kaushik, Stability and delay analysis of multi-layered GNR and multi-walled CNT interconnects, *J. Comput. Electron.* **14** (2015) 611.
12. A. Karthikeyan and P. S. Mallick, Optimization techniques for CNT based VLSI interconnects a review, *J. Circuits Syst. Comput.* **26** (2017) 1730002.
13. A. Karthikeyan and P. S. Mallick, Transmission gate as buffer for carbon-nanotube-based VLSI interconnects, *IETE J. Res.* **64** (2018) 296–305.
14. Z. Li, L. Ci, S. Kar, P. M. Ajayan and J. Q. Lu, Fabrication and electrical characterization of densified carbon nanotube micropillars for IC interconnection, *IEEE Trans. Nanotechnol.* **8** (2009) 196.

15. S. Esconjauregui, S. Bhardwaj, J. Yang, C. C. Cudia, R. Xie, L. Darsi, T. Makaryan, H. Sugime, S. Eslava, C. Cepek and J. Robertson, Carbon nanotube growth on conductors: Influence of the support structure and catalyst thickness, *Carbon* **73** (2014) 13.
16. I. Ciofi, A. Contino, P. J. Roussel, R. Baert, V.-H. Vega-Gonzalez, K. Croes, M. Badaroglu, C. J. Wilson, P. Raghavan, A. Mercha, D. Verkest, G. Groeseneken, D. Mocuta and A. Thean, Impact of wire geometry on interconnect RC and circuit delay, *IEEE Trans. Electron Dev.* **63** (2016) 2488.
17. X. Wang, A. Wang and N. K. Ingle, V trench dry etch, US Patent: United States Applied Materials, Inc. (Santa Clara, CA, US), US Grant No. US9355856B2.
18. C. L. C. Smith *et al.*, Efficient excitation of channel plasmons in tailored, UV-lithography-defined V-grooves, *Nano Lett.* **14** (2014) 1659.
19. G. F. Close and H.-S. P. Wong, Fabrication and characterization of carbon nanotube interconnects, *IEEE Trans. Electron Dev.* **63** (2007) 203.
20. P. U. Sathyakam, A. Bisht, Y. Tandon and P. S. Mallick, Triangular CNT bundles as VLSI interconnects, *Proc. 2016 3rd Int. Conf. Emerging Electronics (ICEE, 2016)* (IEEE, 2017), doi: 10.1109/ICEmElec.2016.8074592.
21. ASU Predictive Technology model (PTM) library: www.ptm.asu.edu/.
22. S. Sapatnekar, *Timing* (Kluwer, Boston, 2004), p. 87.
23. P. U. Sathyakam, P. S. Mallick and A. A. Saxena, High speed subthreshold operation of carbon nanotube interconnects, *IET Circuits Dev. Syst.* **13** (2019) 443–455, doi: 10.1049/iet-cds.2018.5118.