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Low-power selective pattern compression for scan-based test applications ☆

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ABSTRACT

The ever-increasing test data volume and test power consumption are the two major issues in testing of digital integrated circuits. This paper presents an efficient technique to reduce test data volume and test power simultaneously. The pre-generated test sets are divided into two groups based on the number of unspecified bits in each test set. Test compression procedure is applied only to the group of test sets which contain more unspecified bits and the power reduction technique is applied to the remaining test sets. In the proposed approach, the unspecified bits in the pre-generated test sets are selectively mapped with 0s or 1s based on their effectiveness in reducing the test data volume and power consumptions. We also present a simple decoder architecture for on-chip decompression. Experimental results on ISCAS'89 benchmark circuits demonstrate the effectiveness of the proposed technique compared with other test-independent compression techniques.

1. Introduction

The high level integration of the circuits in ultra deep sub-micron (UDSM) technology increases the complexity of testing which increases the manufacturing cost of integrated circuits (ICs). The scan-based testing methodology is widely used in industry to test digital ICs with automatic test equipment (ATE). However, the major problem in the scan-based testing is, it requires large memory to store the patterns as well as its response in ATE. The commercial ATE has limited memory, bandwidth and input–output (I/O) channel capacity. It is necessary to develop techniques to test complex system-on-a-chips (SoCs) without exceeding memory, bandwidth and I/O channel limit of ATE. The power dissipation of the digital ICs during test mode is higher as compared to its normal mode of operation [1]. This high power dissipation during test mode affects the circuit reliability due to elevated average power during loading and unloading of the test stimuli and its response. It adds to the thermal load which can cause structural damage to silicon, bonding wires, or package [2]. The peak-power leads to erroneous data transfer in capture phase of test mode, which invalidates the testing process and leads to unnecessary yield loss [3]. So, it is necessary to develop techniques to reduce the test data volume and power consumptions to test complex system-on-a-chip (SoC).

Several techniques are available in the literature for test data compression and test power reduction which can be categorized into test-dependent and test-independent techniques. The test-dependent compression techniques based on the test pattern generation, fault simulation and structure of the circuit under test (CUT). For example, linear feedback shift register (LFSR) is used to generate test patterns in built-in self test (BIST) embedded architectures. The LFSR-reseeding approach with seed compression were used to compress the test data and test sequence length [4–6]. Also, several other

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approaches such as multi-mode Illinois scan architecture [7], clock-gating [8], embedded deterministic test (EDT) [9], adaptive scan network [10,11], and reconfigured scan forest architecture [12] were proposed to reduce the test data volume and test application time. Several linear decompresser-based compression methods were used to reduce the test data volume [13,14]. The Viterbi-based test compression architecture finds a set of compressed test vectors using the Viterbi algorithm [14]. All these methods are not suitable for SoC testing if the structural information of intellectual property (IP) cores are not available to the design-for-testability (DFT) team.

On the other hand, test compression procedure is applied to the pre-generated test sets in test-independent compression techniques. A typical automatic test pattern generation (ATPG) tool is used to generate test sets for the given fault lists. In these approaches, unspecified bits (also called as do not care bits or *X*-bits) in the test sets are filled with logic values and encoded with suitable coding theory. For example, statistical and Huffman codes [15–18], Golomb code [19] and run-length codes [20–25], lossless image coding [26] techniques were used to compress/decompress the test data. In these techniques, the unspecified bits are filled to logic 0 or 1 to achieve high compression. The technique used to combine run-length encoding and Huffman encoding to compress the test data is proposed in [27]. In this scheme, the test data are compressed by encoding the long data sequence based on counting the repeated patterns or characters. In nine-coded compression technique [28], nine codewords were used to encode the data. Lee et al. [29] have described the approach to encode $2^{|n|}$ runs of compatible or inversely compatible patterns, either inside single test data segment or across multiple test data segments.

The unspecified bits in the pre-generated test sets can also be filled to reduce the shift and capture-power in scan test applications. Many *X*-filling techniques were used to reduce either shift or capture-power or both [30–35]. *X*-filling is a process of mapping the unspecified bits in the test sets into logic 0 or 1. Adjacent-fill technique [30] is the most successful approach in reducing average power. In this technique, the unspecified bits are filled based on their adjacent scan cells' value. The low-capture-power *X*-filling (denoted as LCP-filling) reduces the capture transitions by filling the unspecified bits incrementally using forward implications and backward justification method [31]. The major limitation of this technique is, it reduces the capture transitions by filling the unspecified bits one by one without considering its impact on unspecified bits in their response. Ramersaro et al. [32] proposed a probability based *X*-filling technique called as "preferred-fill" where all the unspecified bits in the test set are filled in a single step. The low shift and capture-power *X*-filling technique known as "LSC-filling" was used to reduce both shift-and capture-power during scan test [2]. In this method, the unspecified bits are filled based on its impact on test response. All these techniques consider the entire unspecified bits for the reduction of test power only. These techniques do not provide better compression ratio. Because, the compression schemes that provide high compression ratio do not reduce the test power effectively, or vice versa.

In this paper, we present a low-power selective pattern compression (LP-SPC) technique to reduce the test data volume and test power consumption simultaneously in full-scan sequential circuits. Test compression procedure is applied only to the group of test sets which contain more unspecified bits and the power reduction technique is applied to the remaining test sets. One selective pattern compression scheme [36] is considered as a base scheme for our compression technique. However, the attention is given only to reduce shift-in average power in [36]. Our compression technique focuses on reduction of both average and peak-power and the test data compression. In the proposed approach, we have mapped the unspecified bits to either 0 or 1 to obtain the maximum compression maintaining the peak-power under safe limit.

The rest of our paper is organized as follows: Section 2 describes the test power reduction scheme followed in our approach. Section 3 describes the proposed LP-SPC scheme and its decompression architecture. Experimental results on compression ratio, peak and average power reductions, test application time and area overhead with our LP-SPC approach are presented in Section 4. We also compare our work with other published works and related evaluations are presented in Section 4. Section 5 concludes the paper.

2. Test power reduction

Typical industrial circuits contain 95–98% of *X*-bits in the test sets generated by ATPG [37]. We have flexibility to fill these *X*-bits with logic 0 or 1 to get fully specified test sets without affecting the circuit's fault coverage. In conventional ATPG, these *X*-bits are filled randomly to get fully specified test set. This neither considers the correlation among adjacent test bits during shifting phase nor correlation between the stimuli and response of the same scan cells. So, the average and peak-power of the circuit during test mode will increase. The filling of *X*-bits in the test set with suitable logic value is the key to reduce shift-power, capture-power and test data volume. Unfortunately, it is not possible to use the same *X*-bit for the reduction of capture-power, shift-power and test data volume simultaneously.

One common practice to minimize the power dissipation during scan-based testing is to reduce the number of scan cell's signal transitions. These can be classified into three categories: (1) the scan-in transitions defined as the difference between the adjacent scan cells' values while loading the test stimuli into the scan-chain, (2) the capture transitions defined as the difference between the test stimuli and its response of the same scan cells, and (3) the scan-out transitions defined as the difference between the adjacent scan cells' values while unloading the responses in scan-out mode. The first and third categories are associated with scan-shift-power which should be minimized, so that the higher shift frequency can be used to reduce the testing time and cost. The second category is associated with the capture-power. The capture-power in test mode should be lesser than the peak-power limit of CUT to avoid the damage of ICs due to excess heat.

The total power consumption in scan-based testing is not only based on the number of transitions in test set but also on relative position of where the transition occurs [38]. One common metric used to estimate the test power is the weighted transitions metric (WTM). The WTM is strongly correlated to the switching activity in the internal nodes of CUT during scan-shift operation. Sankaralingam et al. [38] showed experimentally that scan vectors with higher WTM dissipate more power in CUT.

The WTM for the scan-in test stimuli t_j can be determined by

$$WTM_j = \sum_{i=1}^{l-1}(l-i)(t_{j,1} \oplus t_{j,i+1}) \tag{1}$$

where l is the scan-chain length and $t_j = t_{j,1}, t_{j,2}, t_{j,3} \ldots t_{j,l}$, is the scan vector with $t_{j,1}$ scanned in before $t_{j,2}$ and so on.

The average power (P_{avg}) and the peak-power (P_{peak}) in scan-in mode for a test set $T_D = \{t_1, t_2, t_3, \ldots, t_n\}$ can be estimated as

$$P_{avg} = \frac{\sum_{j=1}^{n}\sum_{i=1}^{l-1}(l-i)(t_{j,i} \oplus t_{j,i+1})}{n} \tag{2}$$

$$P_{peak} = \max_{j\epsilon(1,2,\ldots,n)} \sum_{i=1}^{l-1}(l-i)(t_{j,i} \oplus t_{j,i+1}) \tag{3}$$

Eqs. (2) and (3) show that, reducing the test vector's transition and the weight $(l-i)$ are the key factors for reducing the average and peak-power. The same equations can be used to estimate also the average and peak-powers in scan-out mode.

We consider the number of transitions in scan cells for each scan-chain to compute the capture-power. This is because of the linear relationship exists between capture transitions on the scan-chain and peak-power of the circuit. So, it is attempted to minimize the Hamming distance between test stimuli and its response on each scan cell. This will reduce the peak-power of the circuit in test mode. Filling the entire or larger number of unspecified bits in the test set to reduce the peak-power may affect the compression efficiency and may increase the total power, i.e. scan-in and scan-out transitions. It is required to maintain the capture-power within the circuit's peak-power limit for proper operation. Filling one unspecified bit in the test stimuli may affect many unspecified bits in the test response which may cause capture-power violations. So, it is necessary to estimate the impact of filling of each unspecified bit in the test set. The logic values are assigned to the unspecified bit(s) based on its impact on capture-power. The impact of filling of one unspecified bit with the logic value v (i.e. 0 or 1) for the nth scan cell of mth test vector can be computed as

$$C_{impact}(m,n,v) = \sum_{for\ all\ n} R_{m,n} \oplus S_{m,n} - \sum_{for\ all\ n} R_{m,n} \odot S_{m,n} \tag{4}$$

where $S_{m,n}$ and $R_{m,n}$ are logic values of the test stimulus and response of same scan cells respectively. The two terms of the right side of Eq. (4) represent the number of inconsistent and consistent bit-pairs respectively. It can be noted that, both $R_{m,n} \oplus S_{m,n}$ and $R_{m,n} \odot S_{m,n}$ terms will be 0, if either one of its value is unspecified. That is, $X \oplus 1, X \oplus 0, 0 \oplus X, 1 \oplus X, X \oplus X, X \odot 1, X \odot 0, 0 \odot X, 1 \odot X$ and $X \odot X$ are evaluated as 0. Therefore, the unspecified bit with smaller value of $C_{impact}(m,n,v)$ is to be filled first in order to minimize the capture transitions effectively.

In the proposed power reduction technique, first the unspecified bits are filled based on minimum-transition filling (MT-filling) to minimize the shift-power, and the number of capture transitions are computed. If the capture transition of the given test set is within the threshold limit, then corresponding test set need not be considered for capture-power reduction. The threshold limit is decided based on switching activities of the CUT. If the capture transitions exceed the threshold, then one unspecified bit with smallest $C_{impact}(m,n,v)$ (computed using Eq. (4)) is filled into the logic value v and the remaining unspecified bits are filled to minimize the WTM. If capture-power violation still exists, then unspecified bit with next smallest $C_{impact}(m,n,v)$ is to be filled. The process is iterated till the capture-power becomes lesser than the threshold limit.

The process of reducing capture and shift-powers are illustrated as follows. Fig. 1(a) shows the test stimuli and its response as 1XX100X0 and X0X11X10 respectively. The threshold for capture transition is assumed as 3 in this case, i.e, maximum 3 scan cells are allowed to switch in capture mode. If we conduct MT-filling on the test set, then stimuli and its response becomes 11110000 and 10001010 respectively. The capture transition is computed as 5 which violates the threshold limit. So, it is necessary to compute C_{impact} for unspecified bits. For example, filling the S2 bit into 0 results in two inconsistent and three consistent bit-pairs, so the $C_{impact}(m, S2, 0)$ becomes -1 as shown in Fig. 1(b). The C_{impact} for S2 = 1, S3 = 0 are 0 and -2 respectively as shown in Fig. 1(c) and (d). Similarly the C_{impact} for S3 = 1, S7 = 0 and S7 = 1 are computed as 1, 2 and -1 respectively. Since the $C_{impact}(m, S3, 0)$ has the smallest value, the scan cell S3 is filled with logic 0 and other unspecified bits in the test sets are filled to minimize WTM as shown in Fig. 1(e). Now, the capture transition is 3 and WTM for scan-in and scan-out modes are computed as 8 and 13 respectively.

It can also be noted that, our approach in capture-power reduction differs from [2] in following ways: The impact of unspecified bits are computed only for (1) the scan cells with maximum fan-out, and (2) the unspecified bits having different adjacent values. These two approaches lead to the significant reduction of average power in both shift-out and shift-in modes in addition to the reduction of peak-power. Also, only small fractions of unspecified bits are utilized to reduce the capture transitions.

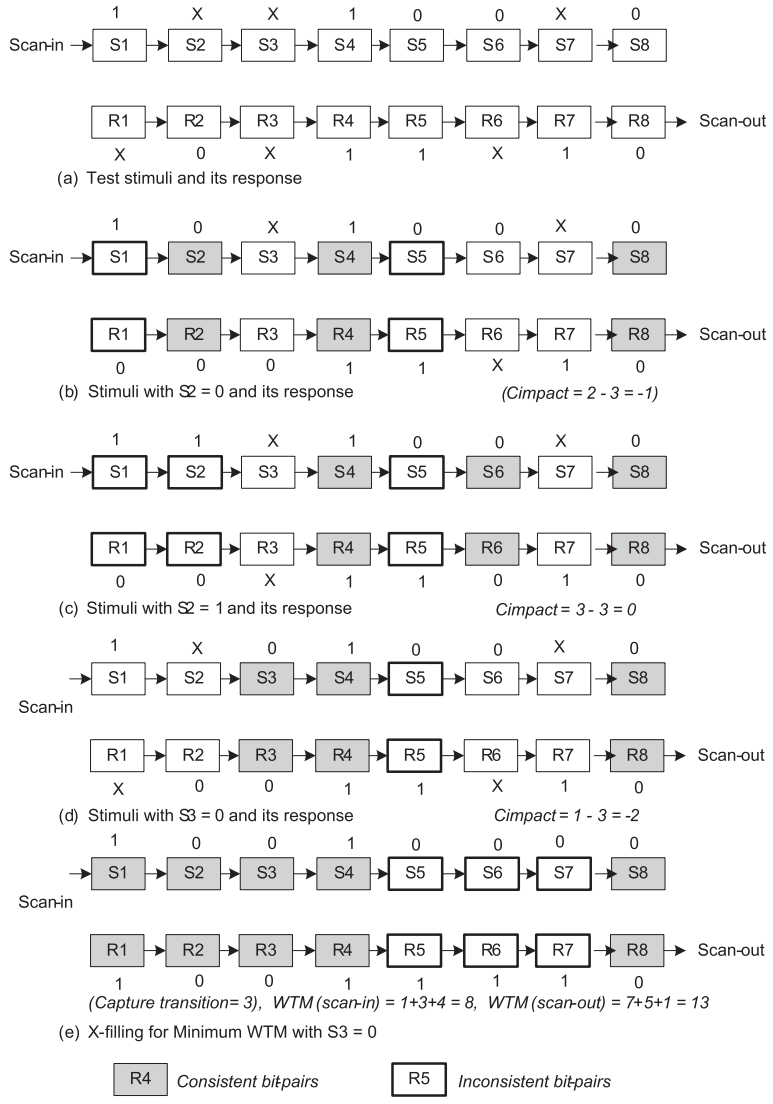

Fig. 1. Example for filling *X*-bits to reduce the test power.

3. Low-power selective pattern compression (LP-SPC) technique

The test set with more unspecified bits can achieve higher compression ratio. So, the proposed LP-SPC technique considers the test sets which contain more unspecified bits for test data compression, and the remaining test sets average power reduction. That is, the entire test sets are divided into two groups based on the number of unspecified bits in each test set. The boundary value to divide the patterns into two groups is user defined. Each boundary value provides different compression ratio and power reduction for different circuits. The test sets which contain lesser unspecified bits than the boundary value are denoted as average power reduction (APR) group. The unspecified bits in the APR group are filled as per the procedure described in the last section to reduce the power. The remaining test sets are denoted as test data compression (TDC) group and unspecified bits in this group are filled to achieve high test data compression. The resultant patterns do not violate the peak-power limit.

The test sets in TDC group are compressed as per the following procedure. In TDC group, each test set is divided into number of segments with equal in size. Then test data in each segment are merged and rearranged in such a way that the resultant patterns shrink into minimum possible patterns. The maximum possible patterns in each segment are limited to 2^m or less, where m is the size of the encoder. This can be achieved by proper filling of unspecified bits in each segment. Then patterns in each segment are mapped with codeword. The size of the codeword is determined based on the number of merged patterns in each segment.

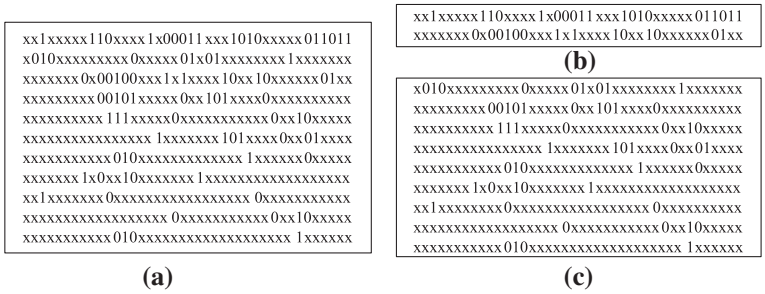

Fig. 2. Procedure for grouping patterns. (a) original test sets (b) APR group (c) TDC group.

Table 1
Pattern encoding procedure with encoder size $m = 3$.

Seg.1		Seg.2		Seg.3		Seg.4		Seg.5	
Pattern	Codeword	Pattern	Codeword	Pattern	Codeword	Pattern	Codeword	Pattern	Codeword
00000000	0	00000000	00	00000000	00	00000000	0	00000000	00
00100001	1	00010100	01	10001101	01	10110000	1	11000000	01
		00111000	10	10001110	10			11010000	10
		00001000	11						

The proposed LP-SPC technique can be illustrated as follows. Fig. 2(a) contains eleven test sets, each with 40-bits wide. These test sets can be divided into two groups based on the number of unspecified bits in each test set. Let us consider the boundary to separate the test set to categorize the group as 30% in this case. That is, the test set which contains 30% or less unspecified bits are considered into APR group and the rest are considered for TDC group. As a result, the APR and TDC groups contain 2 and 9 test sets as shown in Fig. 2(b) and (c) respectively. The unspecified bits in APR group are filled in order to reduce the power as described in Section 2.

The unspecified bits in the TDC group are filled as follows. Let the encoder size is m=3. Each test set can be partitioning into 5 segments with size of 8-bits each. The pattern encoding procedure for TDC group is shown in Table 1. The first segment contains the following nine patterns: x010xxxx, xxxxxxxx, xxxxxxxx, xxxxxxxx, xxxxxxxx, xxxxxxx1, xx1xxxxx, xxxxxxxx and xxxxxxxx. Among these nine patterns, six contain full of unspecified bits. These six patterns can be mapped with any combination of merged patterns. However, to reduce the test power, the unspecified bits are filled with 0s which can be represented as 00000000. Also in segment 1, three patterns (x010xxxx, xxxxxxx1, xx1xxxxx) contain at least one specified bit. These three patterns can be merged in to a single pattern as 00100001. The patterns are encoded with 1-bit codeword since it contains only two patterns, 00000000 and 00100001, which is encoded as 0 and 1 respectively.

Similarly, the test vectors in each segment are merged to shrink the encoding size as small as possible. Table 1 shows the resultant codewords for patterns in each segment. The total number of merged patterns (T_p) in each segment decides the codeword size. For example, in the first segment, $T_p = 2$. So, we can encode patterns in the first segment with 1-bit codewords. If the T_p value is in between 2 and 4, then codeword size will be 2-bits as in segment 2. If $T_p > 8$, then the codeword size needs to be increased to 4 and so on. Finally, the nine test sets in TDC group are encoded with 8-bit codewords as 10001001, 00110000, 01000001, 00001110, 01100100, 11101000, 10000000, 00000001 and 01100001.

The compression ratio can be calculated as

$$\textit{Comp. ratio } (\%) = \frac{T_D - (T_E + T_P)}{T_D} \times 100 \tag{5}$$

where, T_D and T_E are the size of uncompressed test set and encoded test set respectively, and T_P is the size of test sets in the APR group.

In this case, the compression ratio is computed as, $\left\{\frac{440-(72+80)}{440} \times 100\right\} = 65.45\%$. The pattern transformation can be done to get the original test data by using proper remapping hardware logic in decoder.

4. Decompression architecture

Fig. 3(a) shows the decompression architecture used for the on-chip decompression. It consists of a finite-state-machine (FSM), a selector, a log_2k counter, an 2^m-bit shift-register and a combinational logic circuitry for pattern mapping. This decoder feeds the parallel synchronizer logic which generates synchronized data for the CUT's scan-chain. The decoder receives serial data from tester. The first bit of each pattern from tester is considered as *Select* bit which determines whether the

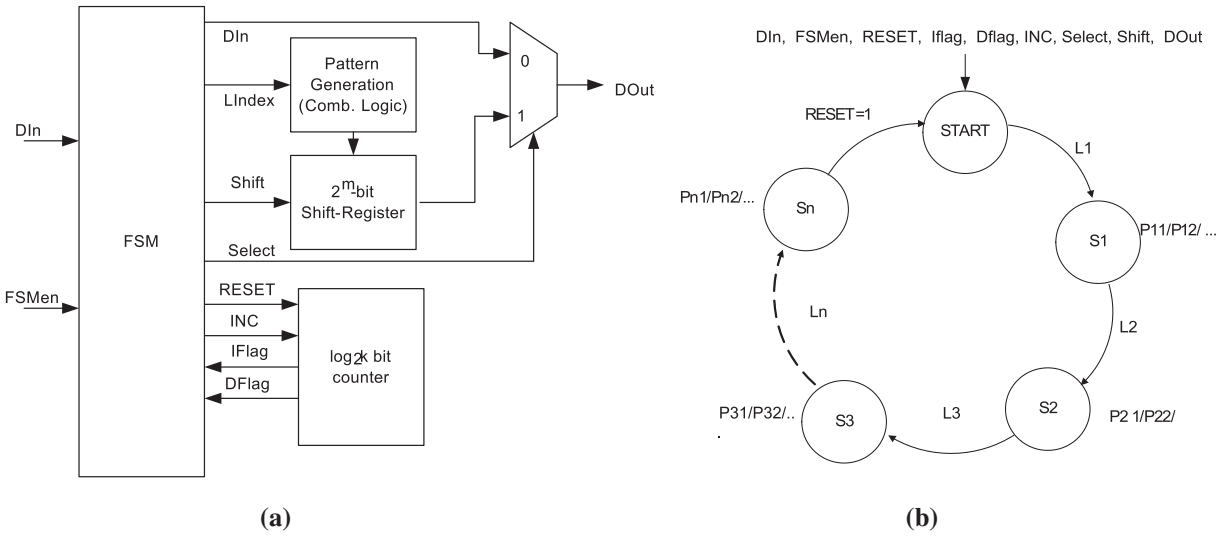

Fig. 3. A decoder used for on-chip decompression (a) block diagram of decompression architecture and (b) state diagram.

pattern is in compressed or in uncompressed form. If *Select = 0*, then the subsequent bits in the test pattern are the actual data and is shifted into the scan-chain as *DOut* in *k* clock cycles, where *k*-is the test data volume in APR group. *Select = 1* indicates that the pattern is in compressed form that needs to be decoded to get the uncompressed data. The *LIndex* specifies the size and position of each segment in the encoded data. With this index bits, the decoded pattern can be constructed using combinational logic. To keep track the number of bits shifted, we use $log_2 k$ – bit counter. The operations of the counter and generation of data-bits based on *LIndex* are controlled by the FSM.

Fig. 3(b) shows the state diagram of FSM which is used for controlling the counter operations and data-bits *DOut* generation. The following signals are used in the FSM: *DIn*, *FSMen*, *Select*, *INC*, *DFlag*, *IFlag*, *RST*, and *DOut*. The FSM receives new bit of data *DIn* when *FSMen* is 1, the counter is set to 0 by assigning *RST = 1*, the decoder receives the first bit *Select* of the pattern from the tester. Now the FSM is in *START* state. In this state, the FSM sends the data to *DOut* or move to *S1* state depending on *Select* bit. If *Select = 0*, the FSM sends *DIn* to the scan cell through the buffer and the counter increments (*INC*) for every *DOut*. The counter value becomes 0 after *k* clock cycles which indicate that pattern is transfered. Once the counter becomes 0, FSM goes back to *START* state to receive the next pattern. If *Select = 1* in *START* state, FSM receives the subsequent bit(s) based on the *LIndex* and set the *LFlag* value to 1 after receiving *LIndex* for the segment 1. The pattern for the codeword is generated using combinational logic. The pattern of *j*th codeword in *i*th segment can be denoted as *Pij*. The decoded bits are shifted through shift register and *DFlag* is set to 1 after *m* clock cycles, where *m*-is the size of decoded bits for the codeword. The FSM starts receiving its next *LIndex* value and moves to *S2* state for decoded logic generation. This procedure is repeated until the FSM reaches its last state *Sn*, where *n* is the number of segments in each pattern.

5. Experimental results

In this section, the effectiveness of low-power selective pattern compression (LP-SPC) method is demonstrated to reduce the test data volume, average and peak-powers in scan-based testing. Experiments were conducted on six larger ISCAS'89 benchmark circuits. We have implemented this work in C and compiled using gcc v3.4.5 compiler. The experiments were carried out with Pentium dual core, 3.2 GHz processor and 2 GB of RAM. To compare our work with others, we have used the test sets generated using Mintest ATPG program [39] which is same as used in [22,20,23,16,15,17,18,29]. The Mintest test profile for ISCAS'89 benchmarks is presented in Table 2.

Table 2
Test set profile for ISCAS'89 benchmark circuits using Mintest ATPG program [39].

Circuit	Scan cells	TV	Size of T_D	% *X*-bits
s5378	214	111	23,754	72.62
s9234	247	159	39,273	73.01
s13207	700	236	165,200	93.15
s15850	611	126	76,986	83.56
s38417	1664	99	164,736	68.08
s38584	1464	136	199,104	82.28

The efficiency of compression and test power reduction depends on the boundary value chosen to separate the TDC and APR group. Each circuit requires different boundary value to obtain maximum compression ratio and lowest test power. Initial boundary value can be set as 5, which can be increased in the order of 5 based on the compression ratio and test power. The compression ratio obtained from our LP-SPC scheme with the encoding size of 4 is compared with other test-independent compression methods as shown in Table 3. The compression ratio for our scheme is computed using Eq. (5). In Table 3, columns 2 through 9 give the compression ratio obtained from other test-independent compression methods such as frequency-directed fun-length (FDR) coding [20], alternating run-length (ARL) coding [22], variable-input Huffman (VIHC) coding [16], extended FDR (EFDR) coding [21], optimal selective Huffman coding [17], equal-run-length coding (ERLC) [23], geometric method [40], and $2^{|n|}$-pattern run-length coding [29] respectively. The last column provides the compression ratio of LP-SPC method and the last row shows the average compression ratio achieved in all the compression methods. On average, the proposed LP-SPC method achieves the percentage of compression ratio improvement of 19.8%, 15.0%, 14.4%, 13.2%, 9.4%, 16.2%, 16.2%, 6.6 v and 5.5% against [20,22,16,21,17,23,40,29] methods respectively. The compression improvement percentage is calculated using $\left[\frac{CR^{others}-CR^{ours}}{CR^{others}} \times 100\right]$, where CR^{others} denotes the average compression ratio of other methods, CR^{ours} denotes the average compression ratio of LP-SPC method.

Next, we present the experimental results for test power reduction. The peak-power threshold is set as 20% of scan cells in the CUT, i.e., only 20% or lesser scan cells are allowed to switch during capture cycle. The actual peak-power constraints depend on the switching activities of the nodes in CUTs and normally provided by design team. In our experiment, the threshold limit is decided based on the switching profile of ISCAS'89 circuits. The shift-in peak-power and average power consumptions of our scheme are compared with FDR [20] , EFDR [21], ARL [22] and ERLC [23] compression methods in Table 4 and 5 respectively. We use WTM metric to compute the average and peak-power (see Eqs. (2) and (3)) which is same as used in [19,22,20,23,29,17,18,25]. The reduction in peak-power and the average power consumption is computed using Eqs. (6) and (7) respectively.

$$peak\ power\ reduction\ (\%) = \frac{P^{C}_{peak} - P^{X}_{peak}}{P^{C}_{peak}} \times 100 \tag{6}$$

$$average\ power\ reduction\ (\%) = \frac{P^{C}_{avg} - P^{X}_{avg}}{P^{C}_{avg}} \times 100 \tag{7}$$

where P^{C}_{peak} and P^{C}_{avg} represent the peak and average power consumptions of the test vector obtained from Mintest program, the term "X"in P^{X}_{peak} and P^{X}_{avg} represents peak and average power of respective methods. It is evident from the Table 4 and 5 that, on average our method achieves 29.9% reduction in peak-power and 83.41% reduction in average power in scan-in mode compared to Mintest test sets. This reduction in both peak and average power has been achieved with higher compression ratio as compared to other compression methods.

We also present the peak and average power consumption in scan-out mode in Table 6. On average, our scheme provides 24.5% and 34.5% reductions in peak and average power respectively in shift-out phase as compared to mintest test set [39]. However, the amount of shift-out average power reduction is less compared to the shift-in average power since we have focused mainly on the reduction of shift-in power while maintaining the peak-power within the limit.

We present the hardware overhead of the decoder which is modeled using Verilog HDL and synthesized using Encounter RTL compiler from Cadence with 1.8 V, TSMC 180 nm CMOS standard cell library. The patterns for different codewords in the segments are considered as parameters and these are synthesized into combinational circuits. The full-scan ISCAS'89 benchmark circuits are synthesized with single scan-chain. The number of cells and cells area for the circuits without and with including the decoder architecture are shown in Table 7. The last column presents the area overhead (%) of the decompression architecture for various circuits. It can be noted from the Table 7 that the cells area increases linearly with the test data volume. We can also use look-up-table approach for pattern mapping, however it requires more hardware overhead.

Next, we analyze the total test application time (TAT) reduction that can be achieved with our LP-SPC technique. The TAT for compressed test depends on the compression ratio, system clock frequency and decompression architecture. In general, the amount of TAT reduction depends on the compression ratio and decompression method. The decoder decompresses the data with f_{SoC} and it is usually larger than f_{ATE}, where f_{ATE} and f_{SoC}, are the ATE and system clock frequencies respectively. The

Table 3
Compression ratio: Comparison with other test–independent compression methods.

Circuit	FDR [21]	ARL [22]	VIHC [16]	EFDR [20]	Opt.Huff. [17]	ERLC [23]	Geometric [40]	2^n-PRL [29]	LP-SPC (Ours)
s5378	47.9	50.8	51.8	51.9	54.9	47.8	57.9	54.2	68.9
s9234	43.6	45.0	47.3	45.6	55.3	43.5	57.2	57.7	55.3
s13207	81.3	80.2	83.5	81.9	83.4	80.6	86.6	87.6	89.7
s15850	66.2	65.8	67.9	68.0	67.9	66.4	70.2	74.3	70.5
s38417	43.4	60.6	53.4	60.6	60.9	58.7	62.2	58.3	68.6
s38584	60.9	61.1	62.3	62.9	65.4	61.6	65.6	72.4	74.5
Average	57.2	60.6	61.0	61.8	64.6	59.8	66.6	67.4	71.3

Table 4
Scan-in peak-power transitions: Comparison with other compression methods.

Circuit	Mintest [39]	FDR [20]	EFDR [21]	ARL [22]	ERLC [23]	LP-SPC (Ours)
s9234	17,494	12,994	12,062	12,060	12,069	12,102
s13207	135,607	101,127	97,613	97,606	97,614	97,685
s15850	100,228	81,832	63,494	63,478	63,511	63,586
s38417	683,765	505,321	404,654	404,617	404,693	404,676
s38584	572,618	234,233	479,547	479,530	479,573	479,748
Average	301,942	187,101	211,474	211,457	211,462	211,559

Table 5
Scan-in average power transitions: Comparison with other compression methods.

Circuit	Mintest [39]	FDR [20]	EFDR [21]	ARL [22]	ERLC [23]	LP-SPC (Ours)
s9234	14,630	5692	3469	3466	3500	3512
s13207	122,031	12,416	8016	7703	8115	7849
s15850	90,899	20,742	13,394	13,381	13,450	13,498
s38417	601,840	172,665	117,834	112,198	120,775	112,235
s38584	535,875	136,634	89,138	88,298	89,356	89,428
Average	273,055	69,630	46,370	45,009	47,039	45,304

Table 6
Scan-out peak and average power transitions: Comparison with [39].

Circuit	peak-power			average power		
	[39]	LP-SPC	Red. (%)	[39]	LP-SPC	% Red.
s9234	16,777	13,248	21.0	14,555	9831	35.5
s13207	132,129	98,341	25.6	116,695	86,878	25.6
s15850	99,647	74,871	24.9	88,385	59,743	32.4
s38417	619,929	430,492	30.6	553,491	322,621	41.7
s38584	577,365	475,324	17.7	521,882	369,383	29.2
Average	259,002	218,455	24.5	261,126	169,601	34.5

Table 7
Area overhead of the decoder.

Circuit	Without decoder		With decoder		Cell area
	# Cells	Cells area (nm^2)	# Cells	Cells area (nm^2)	Overhead (%)
s5328	1647	30,217	2076	33,087	8.67
s9234	1192	25,144	1657	27,256	774
s23207	3182	84,683	3850	88,324	4.12
s15850	4032	88,093	4487	90,647	2.82
s38417	11,791	247,866	13,600	251,831	1.57
s38584	14,059	274,561	16,028	278,401	1.38

system clock frequency is assumed as ϕ-times that of the ATE's clock frequency f_{ATE}, where $\phi > 1$ and it is chosen in multiples of f_{ATE} for synchronization.

Our decompression architecture uses a parallel decoding approach in which the FSM and the system work at two clock domains independently. The FSM receives and identifies the codewords at an ATE clock frequency f_{ATE} and generates the pattern at a system operating frequency f_{SoC}. The test time is the same as the transfer time when there is no compression. If the total bits in uncompressed test is $|T_D|$ and ATE transfers data to SoC at the rate of f_{ATE}, then the TAT of uncompressed test set ($TAT_{no-comp}$) is

$$TAT_{no-comp} = \frac{|T_D|}{f_{ATE}} \tag{8}$$

The LP-SPC technique contains uncompressed data from APR group and compressed data from TDC group. The uncompressed data can be directly fed to the scan-chain through buffer and the compressed data in the form of codewords are decompressed on-chip before sending to the scan-chain. The single channel ATE is used to send data to CUT which takes one ATE clock cycle to send 1-bit to the CUT.

Table 8
Comparison of test application time of LP-SPC method with others (in ATE clock cycles).

Circuit	LP-SPC	Mintest	2n-PRL	FDR	VIHC	TAT red. (%) over			
		[39]	[29]	[20]	[16]	[39]	[29]	[20]	[16]
s5378	9852	23,754	17,346	24,933	17,668	58.5	43.2	60.5	44.2
s9234	23,254	39,273	27,354	42,066	27,235	40.8	15.0	44.7	14.6
s13207	24,120	165,200	94,924	116,101	90,920	85.4	74.6	79.2	73.5
s15850	30,025	76,986	48,274	65,020	48,169	61.0	37.8	53.8	37.7
s38417	62,270	164,736	115,031	186,261	118,989	62.2	45.9	66.6	47.7
s38584	71,678	199,104	128,566	179,530	127,849	64.0	44.2	60.1	43.9
Average	–	–	–	–	–	62.0	43.5	60.8	43.6

The TAT for APR group with T_P-bits can be computed as

$$TAT_{APR} = \frac{|T_P|}{f_{ATE}} \tag{9}$$

The TAT for encoded test set T_E is based on the number of codewords and their size. Here, size of codewords within the same segment is same. Suppose the number of codewords and its size in ith-segment are N_j and W_j respectively, where $j = 1, 2, 3 \ldots, n$ then total ATE clock cycles required for sending the codewords to system are

$$T_E = \sum_{j=1}^{n} (N_j).(W_j) \tag{10}$$

Once ATE sends a codeword C_x to the system, the FSM identifing the current codeword C_x and the decoder generates a pattern for the previous codeword C_{x-1} simultaneously, since we use the parallel decoding approach. The time required for generating a test pattern includes the time for shifting the test pattern from the buffer into the scan-chain. Both FSM and scan clock operate at a frequency of f_{SoC}. The majority of the time used for shifting the pattern into scan-chain while generating the test pattern from codeword. However, smallest frequency ratio f_{SoC}/f_{ATE} is sufficient for the decoder to generate a test pattern for each codeword without halting the ATE. In other words, we can use the 2^m times faster system clock (f_{SoC}) as compared to the ATE clock frequency (f_{ATE}), where m is the size of the encoder. The pattern generation starts once the FSM receives the codeword. During pattern generation process the FSM will not receive any bit from ATE, so it enters to halt state. That is, the ATE enters into the idle state between any two codewords. Therefore, the total ATE clock cycles required to transfer the compressed test set with C_{total} codewords are

$$TAT_E = (C_{total} - 1) + \sum_{j=1}^{n} (N_j).(W_j) \tag{11}$$

Table 8 shows the test application time of LP-SPC method. Column 2 describes the TAT of the proposed LP-SPC and columns 3–6 describe total ATE clock cycles required in the case of applying uncompressed test set [39], and other compression methods presented in [29,20,16] respectively. OurLP-SPC technique reduces the total application time of 62.0%, 43.5%, 60.8% and 43.6% in comparison to [39,29,20,16] respectively.

6. Conclusion

The proposed low-power selective pattern compression (LP-SPC) technique is based on the fact that the test set with more unspecified bits can achieve higher compression ratio. Experimental results shows that the LP-SPC technique can be used to reduce test data volume, test power consumption and test application time simultaneously. The proposed power reduction technique is based on careful mapping of the unspecified bits in pre-computed test sets to 0 and 1. It leads to significant savings in peak and average power without requiring a slower scan-clock. We have also presented decompression architecture with simple pattern transformation logic for on-chip decompression, where test pattern decouples the internal scan-chain from the ATE. We have shown through analysis and experiments that the LP-SPC technique can reduce the test application time. Reduction of overall test application time is an added advantage of the proposed method which is mainly due to parallel decoding approach followed in the decompression architecture. The decoder size and testing time can be reduced further with multiple scan-chains since patterns transformation logic are shared across the scan-chains. Furthermore, the LP-SPC technique can be applied for IP core based SoCs since the compression is performed on pre-generated test sets.

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