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**Abstract**. In this paper the design of low power SRAM has been presented. SRAM memory cell has been realized using adiabatic logic to achieve low power operation. Adiabatic SRAM has been realized using two methods such as i) gradual charging and discharging of bit-line during writing mode and ii) utilizing control transistor based adiabatic circuit i.e., Two Phase Adiabatic Dynamic Logic (2PADL) circuit for the design of memory cell. Furthermore, energy recovery of word line and bit line charge stored in the interconnect capacitances has been realized for the benefit of energy savings. Charge recovery circuits based on 2PADL has been employed in the proposed SRAM memory core to achieve energy recovery. SRAM memory array of (4×4) has been designed as a test circuit. All the circuits are implemented using 180nm CMOS technology and simulations are carried out using Cadence® Virtuoso tool. Simulation results prove that the proposed memory cell has significant amount of energy savings when compared to the conventional static CMOS SRAM cell.

## 1. Introduction

In any electronic system static memory is found either as an on-chip memory in high- end processors or as a memory core due to its higher storage capacity. SRAM contributes significant amount of power consumption in these circuits as it drives large bit line and word line capacitance. Hence, low power memory design is a very highly sought-after research in recent years. Charge recovery or adiabatic logic is one of the most promising non-conventional approaches for the low power design [1].

Several static memory designs using energy recovery circuits have been proposed in the literature. The energy recovery circuit namely, Efficient Charge Recovery Logic (ECRL) has been employed for the implementation of auxiliary circuits such as row and column decoder, row and column drivers and latches [2]. Thus, the SRAM achieves low power by recovering word line as well as bit line charge. There are several energy recovery drivers have been proposed for the design of SRAM memory core [3]. Write scheme using low voltage swing as well as charge recycling on bit line has been proposed [4]. All these circuits use conventional 6T circuit for SRAM memory cell realization. In contrast, SRAM memory cell using adiabatic logic has been proposed [5] [6].

During writing mode, gradual change in supply voltage from Vdd to ground and vice versa, and during reading, word line voltage is decreased to Vth has been developed for SRAM memory cell [5]. Adiabatic SRAM with shared reading and writing port has been developed. Adiabatic SRAM with trapezoidal pulses for word line and bit line voltages have been proposed [7].

In this paper adiabatic SRAM memory cell has been designed using i) gradual change in supply voltage during writing mode and ii) control transistor-based SRAM memory cell for charge recovery. An attempt has been made to design SRAM memory array using 2PADL based charge recovery

circuits [8] for auxiliary circuits and memory cell using 8T adiabatic SRAM. The remaining paper is organized as follows. The design and working of adiabatic SRAM memory cell is discussed in section 2. Simulation results of adiabatic memory cell is presented in Section 3. The SRAM memory array design is explained in Section 4. Section 5 concludes.

## 2. Adiabatic SRAM Cell

### *2.1. Conventional 6T SRAM Cell*

The traditional 6T SRAM cell has two cross coupled inverters with two pass transistors M5 and M6 that is used for the enabling write operation into the circuit by WL. During the write mode the BL line is charged to write a logic 1 into the Q, then the BL is made active thereby the NMOS M1 is ON and PMOS M2 is OFF on the left side and the naturally BL bar is in logic 0, hence the PMOS M4 is ON and NMOS is M3 is OFF on the right side inverter. Thereby the charge logic high is stored in Q. And similarly, the discharging of the Qbar node can be seen.

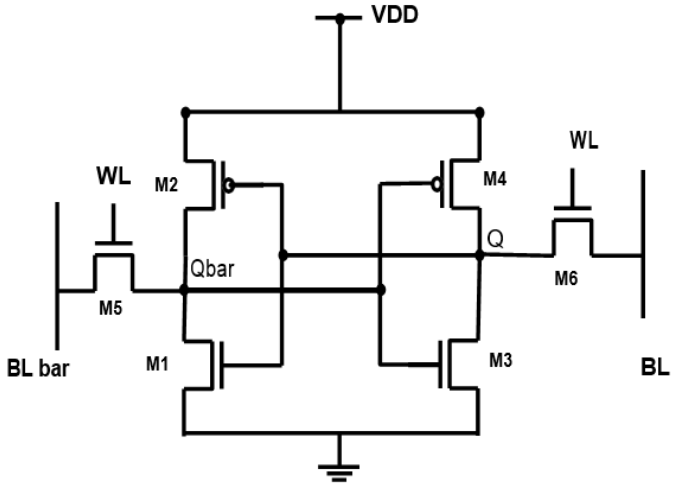



**Figure 1.** SRAM Cell

### *2.2. Adiabatic SRAM.*

The 8T SRAM cell [5] used here has an adiabatically charging bit line in write mode. The SRAM cell consists of traditional 6T-SRAM along with two switching transistors MN1 and MP1 (NMOS & PMOS) as shown in Figure 2. The switching transistors can be shared by many transistors along the rows through MCPL (Memory cell power line) node. Through this sharing the number of transistors can be kept as original i.e. 6T but still achieve adiabatic charging on bit line in writing mode and this means there is negligible area penalty [2]. The PMOS is connected between the power line VDD and MCPL while the NMOS is connected between the ground and MCPL.

To understand the working of adiabatic SRAM, let us consider Figure 2. Based on the control signals S1 and S2 the MCPL node has been connected to either VDD or ground or a floating node. When the S1 and S2 are off, the PMOS is ON and the MCPL follows the VDD. When the S1 and S2 are on then the MCPL follows the GND as NMOS is ON. When S1 is ON and S2 is OFF then, both the NMOS and PMOS are off hence the MCPL node is floating. Thus, the data coming from the bit lines through the cross coupled inverters charge the node adiabatically.

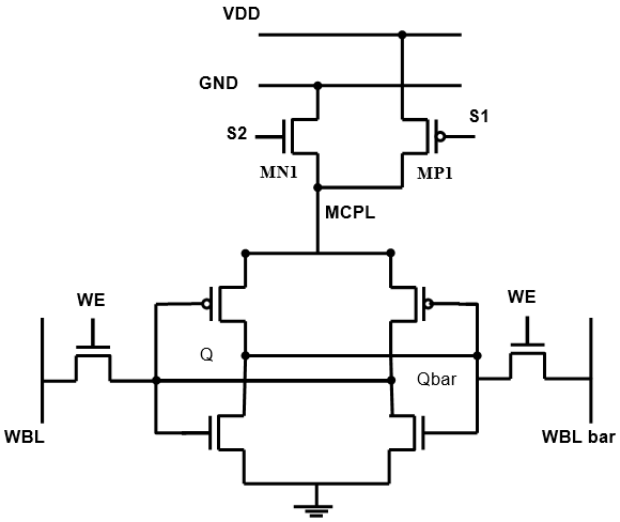



**Figure 2.** SRAM Cell with MCPL

During write mode of operation, the output of memory cell Q (Bit Line) is gradually charged after the control signals S1 is ON and S2 is OF i.e., Q follows the WBL with the delay. The MCPL is already in floating mode. When Q is charged to HIGH the MP1 is OFF and MN1 is ON. Similarly, the Qbar becomes LOW adiabatically. The same operation can be assumed when WBL is discharged and BL bar is charged. During the read mode of operation, the control signals are provided in such a way that S1 and S2 are OFF. Hence, SRAM memory cell works as tradition 6T SRAM with MCPL as the power rail VDD.

*2.3. 2PADL Adiabatic SRAM Cell*

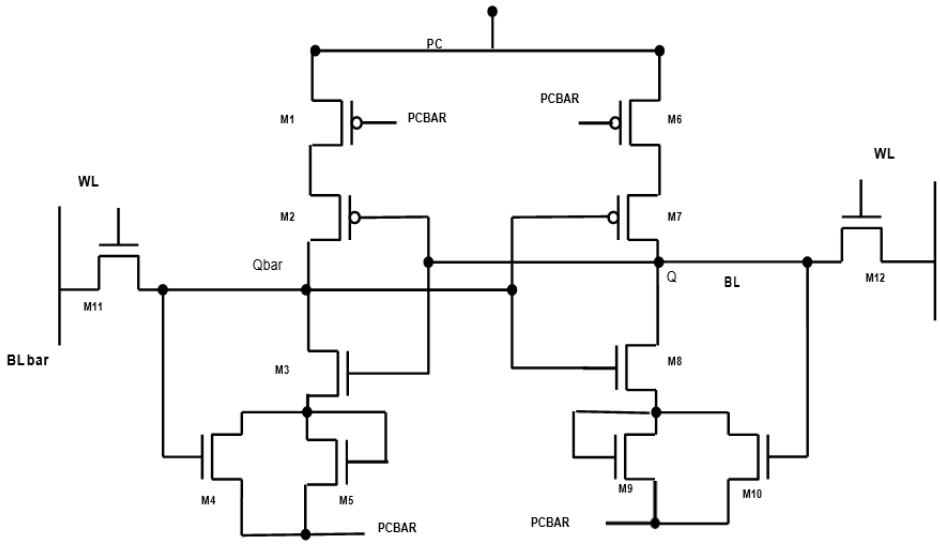



**Figure 3**. 2PADL SRAM Cell

Figure 3 shows the schematic of SRAM cell implemented using 2PADL logic. 2PADL is a two-phase adiabatic logic operated by complementary sinusoidal signals PC and PCBAR [8]. 2PADL SRAM cell employs two additional control transistors along with the 6T-SRAM cell. Complementary

sinusoidal signal PC and PCBAR are used as power supply lines to charge and discharge the output lines Q and Qbar adiabatically.

## 3. Simulation Results

A 1-bit SRAM memory cell is implemented using 2PADL as well as 8T adiabatic logic. For comparison purposes, it is also implemented using 6T static CMOS logic. All the circuits are simulated with the same 180nm process technology. The simulation results of SRAM memory cell are presented and discussed in this section. Average power dissipation is measured directly by integrating the power over the period of simulation cycles. All the simulations are carried out using Cadence® Virtuoso tool.

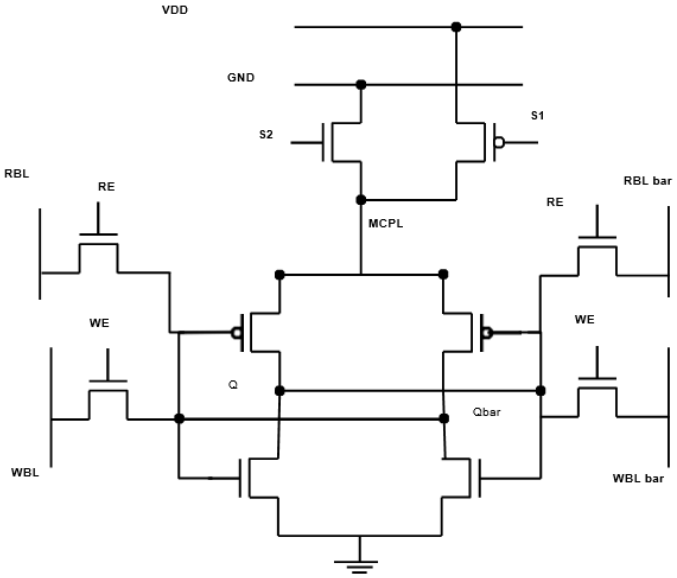



**Figure 4** (a). MCPL based SRAM Cell with Read and Write access transistors

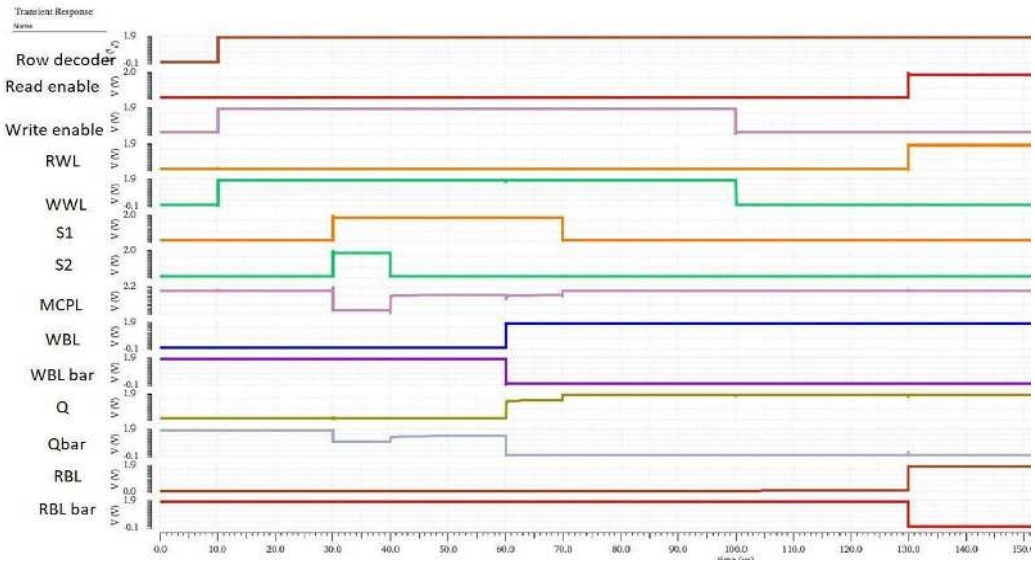



**Figure 4.** (b) MCPL based SRAM Cell with Read and Write Operation

SRAM memory cell has been validated using the memory cell with two separate access transistors for read and write operation as shown in Figure 4 (a). All the circuits are simulated with the power

supply voltage of 1.8V and aspect ratio of 10:1 for both NMOS and PMOS transistors. Figure 4 (b) shows the simulation results of SRAM memory cell implemented using 8T SRAM adiabatic cell. At t=30ns write is enabled and MCPL, Q and Qbar is charged/discharged gradually as shown in Figure 4(b). Read operation is enabled at 130ns and BL and BLbar follows Q and Qbar of the memory cell. Table 1 shows the power consumption comparison of SRAM memory cell implemented using CMOS, 8T-Adiabatic SRAM and 2PADL SRAM. The result proves low power operation of adiabatic SRAM.

**Table 1**. Power Consumption of comparison of 6T SRAM, 8T Adiabatic SRAM and 2PADL SRAM
Cell.

| MODE OF OPERATION | CMOS 6T SRAM CELL | ADIABAT IC MCPL SRAM CELL | 2PADL SRAM CELL |
|---|---|---|---|
| **Writing Power Consumption** | $97.33\times10^{-9}$ W | $38.5\times10^{-12}$ W | $19.27\times10^{-9}$ W |
| **Reading Power Consumption** | $6.740\times10^{-12}$ W | $19.01\times10^{-12}$ W | $1.56\times10^{-12}$ W |

## 4. Design of SRAM Array

An attempt has been made to design SRAM memory array using 2PADL based charge recovery circuits for auxiliary circuits and memory cell using 8T adiabatic SRAM. Figure. 5 shows the architecture of SRAM array. The SRAM array consists of a storage cell, address decoders, sense amplifiers with read and write circuitry [2]. All the circuits except the storage-cell array are realized by using two adiabatic circuit called 2PADL. The address decoder is used for selecting an SRAM cell by adiabatically charging the word line. The required word line is activated by passing address values to the decoders through the two input NOR gate acts as decoder and the type of operation that is the Read or Write is selected by read or write enable circuit.

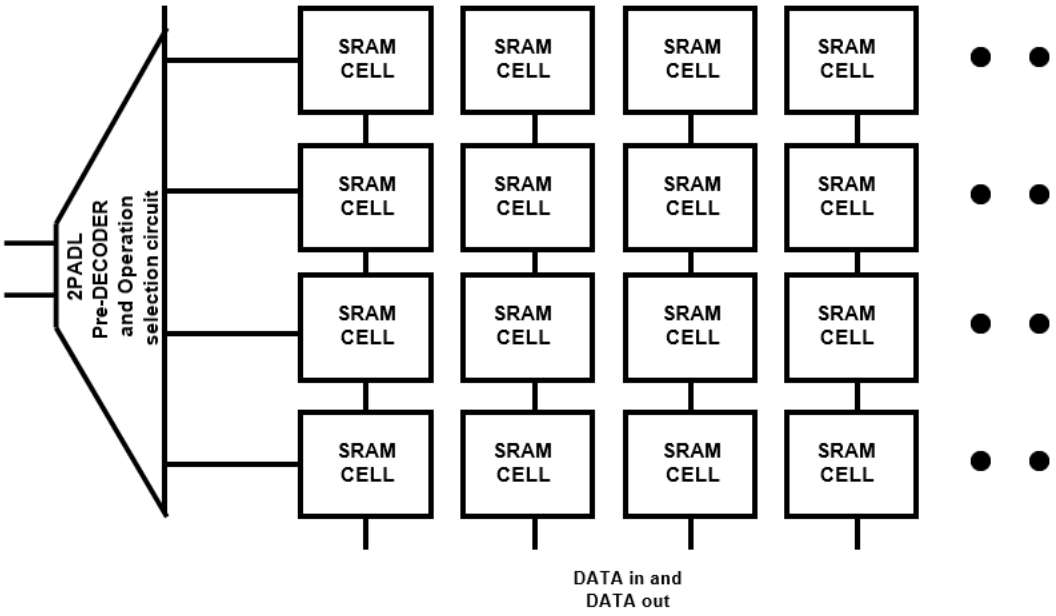
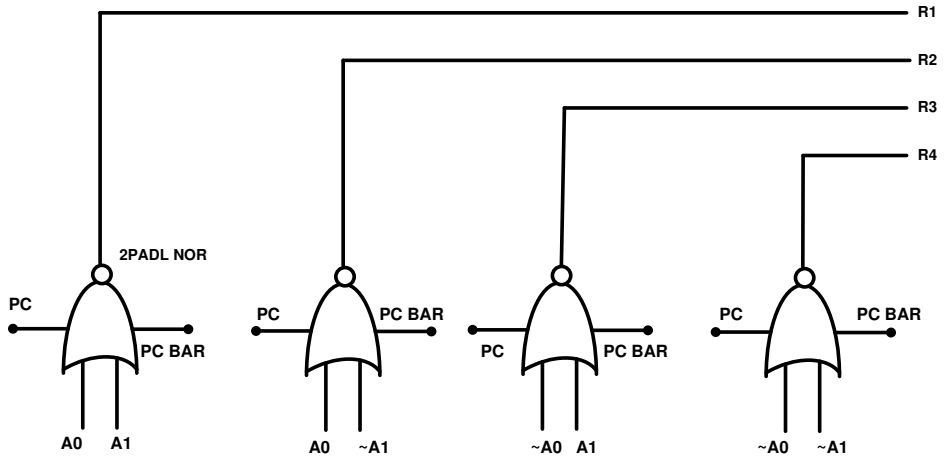


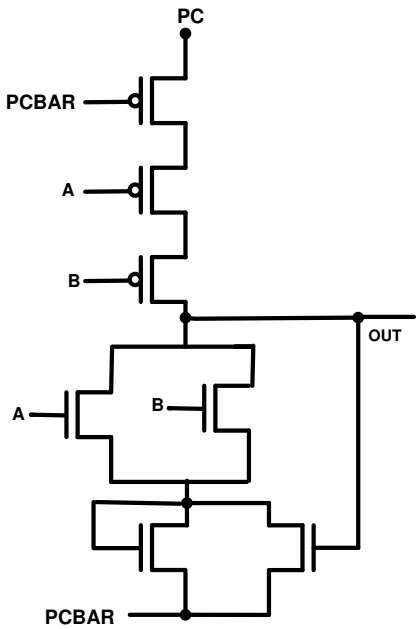

**Figure 5.** Architecture of SRAM Array

Figure 6 shows the schematic of decoders and the transistor schematic of NOR gate implemented using 2PADL. The respective row is selected by giving the signals of A0 and A1 select lines. Then any one row of R1, R2, R3 or R4 is enabled based on the input of the A0 and A1.This row selection

signal from the row decoder is sent to the 2PADL AND gate for selecting the read or write operation on the SRAM. Now based on the Read enable or Write enable signal, the signals RE and WE are generated. Firstly, during write operation Write enable is activated and thereby WE becomes HIGH. Hence, the two access transistors are ON and the data will be written to SRAM cell as explained in the section 4.1.




(a)




(b)

**Figure 6. (a)** 2PADL Pre-Decoder **(b)** Transistor Schematic of 2PADL NOR

A 4x4 array of SRAM memory as a test circuits has been designed. Figure 7(a) shows the single sectional view of SRAM cell used in the implementation of SRAM array. The 8T adiabatic SRAM cell is used in implementation of SRAM array and its functionality is verified. The charge storing in the nodes Q and Qbar has a one-unit clock latency because of the 2PADL adiabatic auxiliary circuit, whereas the read operation occurs in the same clock as intended without delay. Here the speed of the circuit is a necessary trade-off for low power consumption.

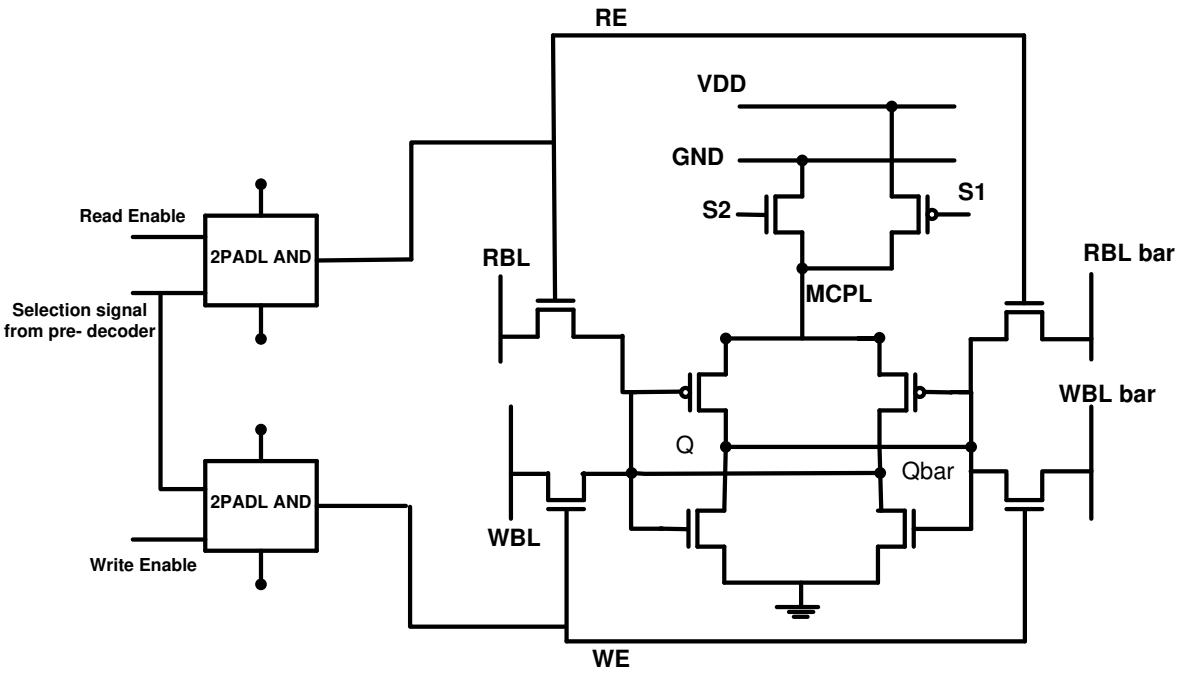



**Figure 7 (a)** MCPL Based SRAM Cell with 2PADL auxiliary circuits.

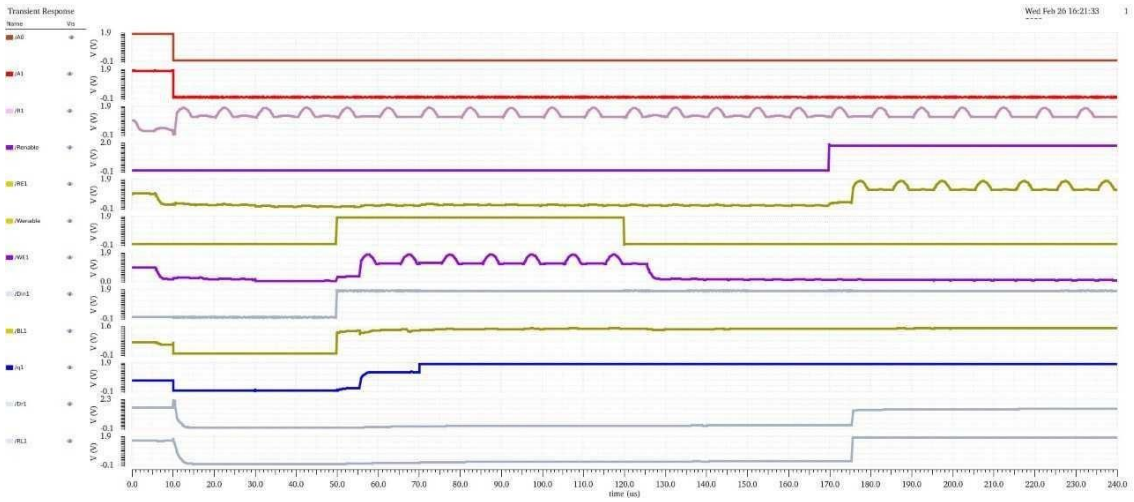


**Figure 7 (b)** MCPL Based SRAM Cell with Read and Write Operation using 2PADL auxiliary circuits.

Figure 7(b) shows the simulation results of 4x4 array for read and write operation. At t=10ns the 2PADL decoder inputs are given as A0=0 & A1=0. Hence the row R1 is selected. Therefore, all the 8 SRAM transistors are activated for the operation of either read or write. Here initially write operation is performed at t=50ns and at the same time the data to be stored WBL=1 and WB bar=0 is also given but not shown and abstracted. Then, there is a latency of one clock cycle for this write operation to be reflected on the WE, so the pass transistors are activated after a clock latency of one clock cycle because of the 2PADL implementation of auxiliary circuit.

The charge in the WBL and WBLbar is stored in the nodes of Q and Qbar respectively by the operation of MN1 and MP1 transistors as discussed in the previous sections of paper. After the write operation is finished i.e., the charge is stored at Q and Qbar, the read operation is done. The read

enable signal is activated at t=120us and RE becomes HIGH after a 1 clock cycle latency. And the charge at Q and Qbar is seen at RBL and RBLbar. The dynamically changing signals at the row selection signal, read enable and write enable using 2PADL logic realize that the power is conserved.

## 5. Conclusion

SRAM memory cell has been designed using 8T adiabatic SRAM and 2PADL SRAM in this paper. Energy dissipation measurement of the SRAM cell is carried out and the result proves that proposed 8T SRAM cell reduced the power dissipation approximately by 25% and 2PADL SRAM cell reduced the power consumption by 70%. In the proposed 8T SRAM write power is comparable to the read cycle power consumption is observed. 2PADL SRAM cell has reduced energy comparison during both read and write operation. The SRAM core designed using the above-mentioned cell along with the adiabatically operated 2PADL auxiliary circuits for decoders help in further reduction of the power consumption. The realization of SRAM memory array using adiabatic circuits in both the SRAM cell design and for the application of auxiliary circuits confirmed the low power operation in this approach.

## References

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