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Optimization Techniques for CNT Based VLSI Interconnects — A Review*

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Interconnects plays an important role in integrated circuits. Copper is used as an interconnect material, but beyond 22 nm technology node it faces many problems due to grain boundary scattering, and therefore carbon nanotubes are the most promising future interconnect materials. Various techniques and approaches such as driver sizing, repeater sizing, repeater insertion, wire sizing, wire spacing, shielding, boos table repeater were used by various researchers. Many of these techniques can be utilized for future CNT based VLSI interconnects as well. This paper presents a detailed discussion on the techniques and approaches of past, present and future relevant for interconnects of VLSI circuits.

Keywords: Interconnect; buffer; repeater insertion; delay; crosstalk; VLSI.

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1. Introduction

Increasing number of transistors in the same area is creating problems in integrated circuits (ICs). The longer length of interconnects increases the delay which affects the performance of ICs. To reduce the delay, the interconnects are divided into shorter segments by inserting repeaters which is called repeater insertion. Boostable repeaters are also used to improve the speed of interconnects, which can raise the internal voltage rail to improve the switching speed. Apart from repeater insertion, the performance can be improved by shielding the interconnects. Basically two types of shielding are there, active shielding and passive shielding. In case of passive shielding the shield wires are tied to ground or power lines, in active shielding the guard line is driven with the same buffers where the source is same as the desired line. Resistance and capacitance of the interconnect depends on wire geometry, i.e., the height, width

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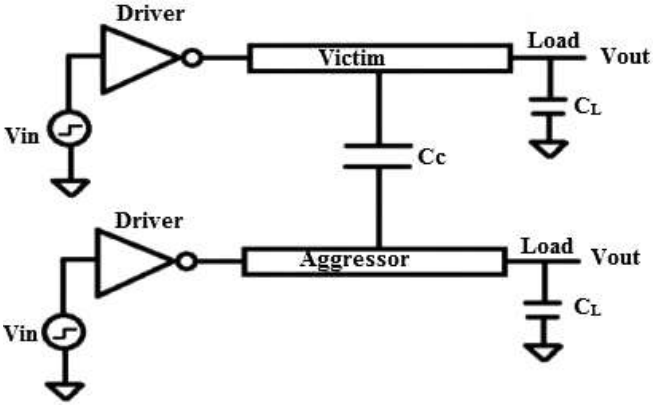

Fig. 1. Crosstalk in interconnects.

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and spacing. Shrinking of wire width increases the resistance, so the wire width has to be increased to reduce the resistance, which may lead to increase in capacitance, which causes the delay and power dissipation.

The delay of a wire grows quadratically with respect to the length; the signal delay tends to be dominated by RC effect.[1] The better option of reducing RC delay is to use better interconnect materials. Carbon nanotubes have lesser resistivity compared to copper, so they act as better interconnect materials for reducing the delay. Based on the applications it is impossible to avoid long wires, for example in case of address lines in memories.[1] So these long wires lead to excessive propagation delay. Scaling of interconnects is also essential when number of transistors are more in the same area, otherwise this may lead to crosstalk. Crosstalk effect also induces delay in signal transmission. When two transmission lines are in parallel as shown in Fig. 1, switching transients in one line which is called aggressor may induce a coupling effect to another line called victim. This coupling leads to a coupling capacitance between the aggressor and victim line, and the victim line will try to induce a delay into the aggressor line, which is called the crosstalk induced delay.

Unwanted coupling can cause signal integrity problems and voltage spikes at the output. Impact of parasitics on crosstalk noise and delay was discussed in detail.[2]

2. Performance Comparison of CNT Interconnects with Copper Interconnects

The electrical and mechanical properties of carbon nanotubes are better as compared to the copper. Since the conductance of CNT is more compared to copper, it can be a better candidate as interconnect in ICs. CNTs are available in different configurations as bundles and it is possible to adjust the metallic tube ratio, bundle dimensions, etc. These adjustments can lead to reduce resistance which has more impact on

delay. CNT bundles are preferred since the resistivity of a single CNT is higher. It has been shown that, Mixed CNT bundle interconnects using CNT-FET as driver operates with low power and high speed compared to a copper interconnect with CMOS as driver.[3] Table 1 shows the properties of SWCNT and MWCNT as compared to copper material.

Due to the higher current density of CNT materials, the electro migration will be lesser effective than copper interconnects. Alam *et al.*[5] have compared the capacitance of copper and CNT bundles for intermediate and global interconnect levels. The capacitance values are 1.13% lesser in case of intermediate interconnects and 1.27% lesser in case of global interconnects for CNTs as compared to Cu. Delay and power dissipation are directly proportional to capacitance. Reduction of capacitance in CNT bundles leads to high speed and low power interconnects. Performance of SWCNT bundle interconnects is shown to be better compared to copper interconnects at giga scale and tera scale operating speeds.[6,7] SWCNT bundle interconnects provide lesser power dissipation and more improvement in delay at global lengths compared to the conventional copper interconnects,[8] and SWCNT bundle interconnects have lower signal delay with technology scaling.[9]

Buffer insertion in copper interconnects leads to increase in power dissipation compared to SWCNT bundles. Ceyhan *et al.*[10] have compared the SWCNT bundles with copper and shown that the resistance per unit length of the SWCNT bundles are lesser for increase in wire width. Individual SWCNTs can also compete with minimum sized copper interconnects.

Repeater insertion in MWCNT interconnects effectively reduce the time delay than repeater insertion in Copper interconnects.[11,12] The optimum numbers of repeaters required for MWCNT interconnects are lesser than copper interconnects at all the levels. Table 2 shows the comparison of MWCNT and copper interconnects for different technology nodes at local, intermediate and global levels. The delay and the optimum number of repeaters are lesser for MWCNT interconnect with an increase in optimum size of the repeater. Cross talk induced delay generated by MWCNT interconnects are comparatively lesser than copper interconnects.[13] In ICs, dynamic power dissipation is directly proportional to the square of the operating

Table 1. Properties of carbon nanomaterials relevant to VLSI interconnects (see Ref. 4).

	Copper	SWCNT	MWCNT
Maximum current density (A/cm^2)	10^7	$> 10^9$	$> 10^9$
Melting point	1356	3800	3800
Tensile strength (GPa)	0.22	22.2 ± 2.2	11–63
Thermal conductivity (10^3W/m-K)	0.385	1.75–5.8	3
Temperature coefficient of resistance ($\times 10^{-3}$/K)	4	< 1.1	-1.37
Mean free path	40	$> 10^3$	2.5×10^4

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Table 2. Comparison of copper and MWCNT interconnects.

Technology node	Material	Length	Delay variation	Optimum no. of repeaters	Optimum size of repeater
14 nm[11]	MWCNT	Global level	(40–1100)ps	10	38
		Intermediate level	(5–1100)ps	N. A.	N.A
		Intermediate level	(150–200)ps	12	35.6–38
	Copper	Intermediate level	(200–580)ps	38	19.6
22 nm[11]	MWCNT	Global level	(125–200)ps	2	275.4
	Copper	Global level	(200–420)ps	7	164.8
45 nm[12]	MWCNT	Global level	(10–450)ps	5	
		Intermediate level	(3.5–11)ps		
		Local level	(2.2–2.85)ps		
	Copper	Global Level	(20–1800)ps	11	
		Intermediate level	(3.8–17)ps		
		Local level	(2.15–2.7)ps		

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voltage. Operating the device at higher voltages may reduce the delay, but leads to more power consumption. Most of the portable devices and sensor networks require low power to minimize the energy consumption. Minimizing the energy consumption leads to longer battery life. Ultra-low power applications are in demand for reduced power dissipation. Low power can be achieved by scaling the supply voltage below the threshold voltage. Scaling the supply voltage also leads to increase in delay.

Many researchers focused on operating the interconnects at sub threshold voltage levels.[14–17] Pable *et al.*[14] have shown that the increase of global interconnect resistance and driver resistance at the sub threshold level affects the performances of interconnect. They have also shown that performances of SWCNTs are better than copper at short and intermediate interconnect lengths, but in global interconnects at deep sub threshold conditions individual SWCNTs are better, compared to copper which is only better at moderate sub threshold conditions.[15] The overall performances of SWCNTs are far better than copper in most of the sub threshold operating regions for all interconnect lengths. Their work demonstrated that the individual SWCNTs preferable at sub threshold conditions. Jamal *et al.*[16] have shown that the individual SWCNTs are preferable as interconnects for high speed and less energy dissipation at sub threshold operating voltage. Optimizing the interconnect drivers to operate the FPGA at near sub threshold region, and the possibility of inserting repeaters and suitability of CNT as interconnect were done.[17] Crosstalk is another concern in VLSI interconnects. A randomly distributed mixed CNT bundle is presented for the analysis of crosstalk induced delay.[18] Further, in-depth analysis of modeling of mixed CNT bundles[19,20] and additional parameters of inter-CNT capacitance and tunneling conductance is also presented.[21] DWCNT bundle interconnects are more suitable than SWCNT bundle interconnects for reduction of crosstalk.[22] Performances of interconnects are also affected by increase of temperature. Thermal Conductivities of CNTs are more than copper as shown in Table 1. CNTs can operate with a nominal level even at higher temperatures. Crosstalk noise

voltage levels in CNT is lower than the copper conductors, when there is a rise in interconnect temperature.[23] Considering the inductive effects of copper and CNTS, bundled SWCNT interconnect based buffering can effectively reduce the delay with optimized number of buffers.[24] The works show that individual SWCNTs can be preferred for sub threshold operations, and MWCNTs are more suitable for repeater insertion, which has optimum number of repeaters with lesser delay.

3. Repeater Insertion

Lengthy interconnects can be made into shorter segments by introducing the intermediate buffers called repeaters.[1] Repeater insertion is a common technique for driving long global interconnects.[25] Optimal number of repeaters and repeater size has to be designed such that, the delay due to repeaters must not increase the overall interconnect delay. The optimal number of repeaters that minimizes the overall delay can be given by[1]

$$m_{opt} = L\sqrt{\frac{0.38rc}{t_{pbuf}}} = \sqrt{\frac{t_{pwire(unbuffered)}}{t_{pbuf}}} \tag{1}$$

and the minimum delay is given by[1]

$$t_{p,opt} = 2\sqrt{t_{pwire(unbuffered)}\, t_{pbuf}}\ , \tag{2}$$

when the delay of individual wire segment is made equal to that of repeater. Here t_{pbuf} is the fixed delay of repeaters.

3.1. *Algorithms and methodology for repeater insertion*

Various algorithms for repeater insertion has been introduced to reduce the delay in copper interconnect. Most of the repeater insertion techniques are concentrated on reducing the delay, but noise also affects the performance of the global interconnects. Charles *et al.*[26] presented a buffer insertion technique using three algorithms for noise avoidance in single sink, multiple sink and simultaneous noise and delay optimization. Using this algorithm they have shown that buffer insertion can provide a suitable environment for simultaneous optimization of timing and noise. Routing in ICs can minimize the total wire length and number of vias. Therefore, routing can be used to complete all the connections without increasing the chip area. The constraints of routing in IC's are placement of cells, number of routing layer requirements. Macro cells in the integrated circuits are useful for routing of wires into that, but they act as obstacles for buffers. Maze Routing Algorithm was used to find a shortest connection between the source and destination node in ICs.

Muhammet *et al.*[27] proposed a scalable Maze routing algorithm which satisfies the exact constraints for routing, but it does not provide a solution for buffer insertion. Both buffer insertion and routing are necessary for optimization in interconnects.

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Another work by Hai Zhou *et al.*[28] introduced a new algorithm which solves, both Maze routing and buffer insertion problems, by considering the buffer location restrictions points in the macro cells. The objective of optimal buffer insertion is to find the exact location to insert buffers which satisfy the delay constraints. A fast algorithm to compute the optimal buffer insertion for multiple pin nets was identified, which also reduces the buffer cost and improves the running time[29] and it does not identify the exact buffer location points. Since macro cells act as obstacles for buffer insertion, buffer insertion at those points are difficult. Identifying the exact location of buffer is necessary.

Bagheri *et al.*[30] have introduced an algorithm to detect the optimized buffer size and best location for buffer insertion. Here the delay and power are considered as two components, early turn delay and early turn power, end-to-end delay and end-to end power. This technique detects the early turn points as proper location for buffer insertion.[30] Signals through the entire chip passes through n number of clock cycles requires pipelined interconnects, which are designed to reach the latency constraints. A new latency aware technique for the concurrent insertion of repeaters by considering the clock skew in pipelined interconnects were designed to minimize the overall latency of propagated signals.[31] In clock networks, a new methodology for design space is constructed for the interconnects.[32] A new buffer model using alpha power law was proposed which have less error compared to conventional model. The model was improved by taking the overshoot effect into consideration.[33] Alaa *et al.* have designed an improved RC model for buffer insertion, which reduces the delay of interconnects using lesser and smaller buffers. They also compared various RC models and showed that π configuration yields better accuracy.[34] Supply voltage and threshold voltage also play a major role in the design of interconnects, reducing the supply voltage leads to delay, and improves the energy efficiency.

Zarrabi *et al.*[35] has designed the interconnections with minimum energy requirements by considering the supply voltage and threshold voltage of device. Based on input transition time, an equation for buffer sizing was derived to get the number of repeaters and driver size for optimized delay.[36] Most of the repeater insertion techniques were used as serial repeaters. Performance of parallel repeaters is better than serial repeaters.[37,38] For high speed signaling, parallel repeaters are more suitable. A new mathematical modeling for parallel repeater insertion in SoC interconnects were derived by taking the repeater pull down resistance in parallel with the interconnect.[37] Regeneration techniques in serial and parallel repeaters were compared. A better speed and area for parallel regeneration is achieved for longer lengths.[38] Performance of interconnects can also degrade due to the increase of temperature in integrated circuits. Temperature dependent model of various repeaters and drivers were investigated.[39–41] Alizadeh *et al.*[39] have identified that in driver and repeater models high temperature leads to slow response of repeaters and low temperature leads to crosstalk noise.

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3.2. *Power optimization in interconnects*

Based on Moore's law, the numbers of transistors in integrated circuits are getting doubled for every eighteen months. Scaling of transistors leads to short channel effects, leakage currents, problems in controlling the threshold voltage of transistors. Similarly the feature size reduction also affect the interconnects in terms of delay and power dissipation. Power optimization is more important in integrated circuits due to the advancement of low power devices. Power optimal repeater insertion techniques for global buses were addressed by Fatemi *et al.*[42] They used MTCMOS technique to calculate the repeater size and repeater distance. Here leakage power consumption is reduced with a small delay penalty. The authors[42] have concentrated only on leakage power reduction, and still the total power dissipation may increase. A new methodology was developed to calculate the repeater size and interconnect length which minimizes total power dissipation with a delay penalty. Since all the global interconnects may not be in the critical path, a small delay penalty can be tolerated on the noncritical paths.[43] An optimization technique to reduce delay, delay variation, power consumption in interconnects was designed and also a design space was obtained to reduce the complexity in clock networks.[32] Changes in operating voltage or operating frequency induce power dissipation. Increase in frequency of switching in a transistor causes more dynamic power dissipation.

Zarrabi *et al.*[44] have designed interconnects for minimum energy requirements by considering the dynamic output resistance characteristics of repeaters for all the operating states. Repeaters can reduce the propagation delay and signal declaration. Dynamic power dissipation occupies 50% of total interconnect power dissipation. It is mainly due to repeaters charging and discharging the interconnect. Among these, 90% of this power dissipation occurs particularly in 10% of the interconnects.

Most of the works were concentrated on design of repeaters, static power dissipation and dynamic power dissipation for fixed loads. Changes in output loading of the transistors vary dynamic power dissipation. Based on the loading conditions the repeater or driver can be changed. Weerasekera *et al.* have designed a smart repeater for on-chip interconnects driving capacitive coupled interconnects and energy saving is achieved by maintaining interconnect loads relatively constant.[45] Electro migration (EM) is another issue in the VLSI interconnects which affects the reliability, and even it can cause failure of a circuit. Electro migration is the forced movement of metal ions due to electric field. In on-chip interconnects it causes wire resistance to increase under stress and it limits the maximum current densities. When the resistance increases to certain degree, it affects the chip performance or even causes malfunction. A scheme for trade-off between power integrity and EM reliability was met by investigating the natural redundancy of power grid. Cost of improving power grid EM reliability is also reduced.[46]

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3.3. *Approaches in repeater insertion*

An analytical model for repeater size and repeater insertion lengths for a particular technology and architecture was introduced.[25] Based on this model, new approaches were introduced in repeater insertion techniques.[28,33,47,48] Repeaters are used to reduce the delay and restore the signal. Repeaters also have some switching time that contributes to signal delay. So, sizing of repeater has to be done efficiently by considering its delay. Under normal circumstance, CMOS inverters are used as repeaters because CMOS inverters have fewer transistors. Charging and discharging is fast and the signal has to pass through fewer transistors. Proper sizing of CMOS inverters reduces delay and power dissipation. CMOS inverters have more static power dissipation.[1] Crosstalk is another issue in closely packed ICs which increases delay as discussed. Schmitt trigger is another approach which has lower threshold voltage. Due to this, they have lower rise time for the signals, which reduces the delay and noise glitches. Schmitt trigger can respond faster for a slowly changing input. Schmitt trigger buffers perform better compared to CMOS inverter buffers for delay, power dissipation and crosstalk noise.[47] Another approach of using Schmitt trigger as buffer reduces the crosstalk and delay for frequencies of up to 20 GHZ.[49]

These works show that the response of Schmitt trigger is faster due to lower threshold voltage. Optimizing the global interconnects for power delay product produces a much smaller increase in both power and delay as compared to separately optimizing power and delay. If the length of the interconnect increases, the difference in optimum width for minimum power and minimum delay also increases. Magdy *et al.* have introduced power delay area product in a repeater system by considering system area[50] and neglecting crosstalk. Reducing the distance between two parallel interconnects due to closely packing also leads to more crosstalk. Optimization has to be done by considering delay, power and crosstalk.

Performance of power delay crosstalk product is compared with power delay product. Power delay crosstalk product is best suited to determine optimum number of repeaters for reducing power, delay and crosstalk.[51] When transistor performs more switching, it leads to more dynamic power dissipation. Due to this, overheating of the chip occurs which reduce the lifetime of the chip. Power dissipation increases with technology scaling. This is due to the dominating of leakage current components. A low power transmission gate (LPTG) based CMOS buffer circuit was designed, which has less leakage components and reduces the power dissipation with a delay penalty.[48] A smart repeater minimizes delay and jitter for capacitively coupled global interconnects. Transmission gates and CMOS inverters were used to alter the drive pattern dynamically that depends on bit pattern.[45] The authors[45,48] have concentrated on different approaches using transmission gates to reduce the leakage power component in repeaters. A new methodology is proposed by modeling the repeater pull-down resistance in parallel with the interconnect. This provides optimized design, such as position and sizes of repeaters required for interconnect

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regeneration.[37] Capacitive crosstalk in parallel buses were analyzed and the expression for delay and buffer size were derived.[52] Simultaneous buffer insertion and uniform wire sizing is performed through a proposed cost function for optimization of delay and crosstalk.[53]

3.4. *Boostable repeaters and drivers*

Power efficiency is one of the main challenges in nanometer regime. Circuit aging and process variations are the major difficulties in nanometer process, still there are concerns on reducing variation effects. Boostable repeaters can be used to boost the switching speed. Boostable repeaters can raise its internal voltage rail to boost its switching speed. A boostable repeater which achieves a fine grained voltage adaptation was designed.[54] A novel boosting structure has been designed using double gate all around (DGAA) transistors which plays an important role in high speed ICs for speeding up the signal propagation in critical path.[55]

A capacitive boosted buffer technique for energy efficient variation tolerant subthreshold interconnects has been introduced. The proposed boosted buffer improves boosting efficiency to realize delay and power reduction.[56] Booster can be used for driving the bidirectional lines. Less number of boosters are required to drive the interconnect with same length, area and power. Optimization of booster is also necessary for delay and area reduction. A new rule was derived for insertion and sizing of boosters, which determine the number of boosters that can save area, power to obtain the speed over repeaters.[57] A performance boosting technique for delay insensitive on-chip interconnects was presented and, this technique leads to high throughput and power efficient communication of signals with delay variation insensitivity.[58]

Boosting of drivers can also improve the signal transition compared to boostable repeaters. Optimization of driver transistors can have more impact on delay. Ho *et al.*[59] have designed a high boosting pre-driver and compared with conventional repeater at sub-threshold supply voltage. The proposed driver has higher concentration at process and temperature variation than conventional repeaters and reduced the sensitivity on temperature fluctuations. The works were done for boosting the signal speed by introducing the boosting techniques at driver and repeater stages of interconnect.

4. Other Optimization Techniques in Interconnects

Crosstalk between two parallel lines increases when the lines run parallel for higher length.[1] Shielding in high speed integrated circuits is a common way to reduce crosstalk noise. Shielding is placing ground or power lines at the sides of a victim signal line to reduce noise and delay uncertainty. Crosstalk between two coupled interconnect is neglected when a shield is inserted between the lines. Shield lines can

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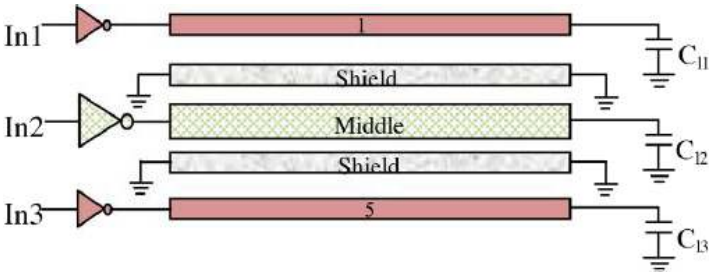
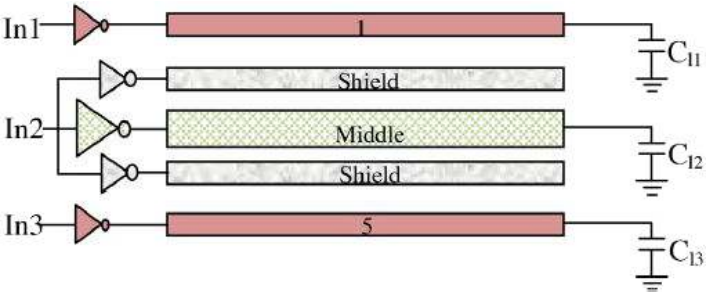


(a) Passive shielding method (see Ref. 64)



(b) Active shielding method (see Ref. 64)

Fig. 2. Passive and active shielding methods.

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also increase noise coupling due to power/ground noise.[60] Shield line isolates the voltage switching activities of the neighboring lines due to switching capacitance. Two types of shielding methods have been developed — active shielding[61] and passive shielding.[62]In passive shielding, power or ground lines are routed as shield lines between critical interconnects to minimize the noise coupled between aggressor-to-victim line. Active shielding use dedicated shield lines with switching signals. Performance of active shield in reducing crosstalk is better than passive shield but requires additional area and consumes more power. Performances of resource based simultaneous shield and repeater insertion are better compared to only shielding or only repeater insertion which can optimize either delay or power.[63] Actively shielded wires have better performance in terms of delay and signal slopes compared to passively shielded wires at the expense of higher power consumption.[62] The technique has to be chosen based on the parameters to be optimized, i.e., area, power, and delay. Mehri *et al.*[64] have investigated that passive shielding (Fig. 2(a)) have a better resistance against electromagnetic waves, which reduces crosstalk, and active shielding (Fig. 2(b)) is the better choice for optimizing delay.[64]

A crosstalk noise model is used to evaluate the effectiveness of shield insertion. A shield line in the vicinity of signal line which can reduce inductive coupling. A new shield insertion technique is investigated by taking the shield line for every global line

in the upper metal layers for controlling crosstalk noise.[61] Surfing interconnect is a pipeline technique which is designed to attenuate timing uncertainty to allow more aggressive timing in noisy environment. It is used for wave pipelined serial interconnect to increase the data transfer rate. Two novel surfing techniques using uniform and nonuniform repeaters for differential wave pipelined serial interconnects were introduced. A controllable inverter pair is used for higher data transfer rate through differential on-chip signaling interconnects.[65]

5. Optimization in Carbon Nanotube Interconnects

The individual SWCNTs have a ballistic resistance of 6.45 kΩ. To reduce the impact of single SWCNT, bundle of SWCNTs in parallel are required to provide high conductance. Optimization techniques used for copper interconnects can be applied to carbon nanotube interconnects. Repeater insertion in CNT interconnect is more feasible as compared to copper interconnects. Performance of CNT bundle interconnect at global level is better compared to copper interconnects.

The number of repeaters and the repeater size required for the same interconnect length is lesser compared to the copper interconnect.[66] Insertion of repeaters in MWCNT interconnects can effectively reduce the total time delay. A closed form expression to estimate the time delay of MWCNT interconnect by repeater insertion is presented.[11]

The number of repeaters required in MWCNT interconnects for the same dimension is lesser to that of copper interconnects.[11,12] A semi analytical delay estimation model is proposed which can perform a fast analysis of MWCNT global interconnects in terms of delay, buffer insertion and crosstalk. At global and intermediate interconnect levels MWCNT is faster compared to copper interconnect.[12] Optimal number of repeaters remains unchanged with the variation of repeater size. Bundled SWCNT and MWCNT have few number of repeaters compared to copper.

Contact resistance of MWCNT is comparably higher than SWCNT. Impact of contact resistance has to be considered for MWCNT for optimal repeater insertion, since it is very sensitive to variation of contact resistance.[67] Crosstalk in carbon nanotube interconnects can be reduced by using semiconducting CNTs at the periphery and metallic CNTs in the core of CNT bundle.[68]

Temperature is another issue that affects the performance of interconnects. Temperature dependent analysis shows that copper interconnects are faster than CNT interconnects at high temperatures.[40] The performances of MWCNT bundle are better in power, delay and power delay product than SWCNT bundle interconnects.[41]

6. Conclusion

The optimization techniques required for interconnects are studied here. Most of the optimization techniques were investigated earlier for copper interconnects.

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The optimization techniques for "repeater insertion" in CNTs can give better results compared to copper. The techniques like shielding, skewing, surfing for a pipelined interconnect were not implemented for CNT interconnects till date as per our knowledge. Repeater insertion with shielding in CNT interconnects can also provide a better performance. Compatibility of silicon with carbon materials can produce better optimization. These optimization techniques can be applied to different configuration of CNTs as well.

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