Real Time Design and Implementation of FPGA Based Timing and Control System for Wireless Radar Communication

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Real Time Design and Implementation of FPGA Based Timing and Control System for Wireless Radar Communication

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Abstract. This paper introduces real time application of FPGA based Timing Control Signal Generation card for Active Phased Array Radar Transmit Receive modules wireless radar communication. Active phased array radars usually have Transmit-Receive (TR) modules located near to the antenna elements and all the TR modules are to be synchronized for proper operation of the radar system. The TCSG is the heart of radar system which is designed to provide interface for digital controls, analog parameter monitoring, and timing and control signals generation required for 1 kW TR Module operation. The main objective of TCSG is to control and monitor the field located TR modules remotely from the control and instrumentation room, usually far away from the antenna field. Each TCSG card is provided with unique IP address and port number to distinguish each card though they perform same kind of operations. After remote connection establishment, the TCSG card responds to the commands given for controlling or monitoring the TR module parameters. A PC based user interface allows sending controls and monitoring the health of the TR modules. The functionality of the TCSG card is verified with a test bench setup and the results shows that the TCSG card is working properly for all the user parameters. The proposed framework comprises of detailed design, architecture, visualization, implementation and integration on a 1 kW high power TR module for the radar communication. Simulation of various control pulses for radar real time operations are carried out using Vivado and updated to the real time application using Artix-7 FPGA.

Keywords: Artix-7 FPGA, TR-Module, Radar, Vivado, Analog to digital Converter (ADC), Ethernet PHY

1. Introduction

Active Phased Array Radars [1] have become the modern radar systems since their architecture overcome the major problems with the passive array. The active array radars have dedicated transmit-receive (TR) modules [2] for each antenna which are distributed in the antenna array field. The complexity of such radar lies in achieving the synchronous operation of the TR modules as they have to generate all the required pulses for the proper operation. National Atmospheric Research Laboratory (NARL) has indigenously developed and realized Active Array MST radar system with the latest technologies, such as state-of-the-art high power solid state Transmit-Receive modules (TRM)with

Atrix Field-Programmable Gate Array (FPGA) [3] based distributed Timing and Control Signal Generator card (TCSG), distributed control signal system to each TRM through optical fiber. Atrix-7 based TCSG system card located in the TR modules, receives the master reference pulse (IPP) from the master TCSG located in the control and instrumentation room and generates all the pulses such as the phase shift, digital attenuator, transmit (Tx), blanking and gating for power amplifier required for the normal operation of the TR module. Atrix-7 FPGA has both analog and digital parameter monitoring facility for monitoring the health of the TR modules. The communication between the radar control system and Artix-7 based FPGA is through the optical Ethernet interface. The FPGA generates real time pulses according to the experimental specifications file (ESF) provided by the user via radar controller system. Implementation of Artix-7 FPGA in the TR module control card to generate the control pulses and sample outputs are discussed in this paper.

2. Methodology and design

TCSG Card is an Artix7 XC7A35T with 33,280 logic cells FPGA based board, which provides interface for digital controls, analog parameter monitoring and timing generations required for the normal operation of the TR module. Artix-7 TCSG Card hardware is provided with about 27 digital I/O lines (for controlling and monitoring), four Analog parameters monitoring and Optical Ethernet interface for remotely controlling or monitoring a particular TR Module. All the parameters are controlled and monitored using Ethernet based protocol from radar controller PC. Each Artix-7 TCSG card is provided with a unique IP and Port No. to distinguish each card though they perform same kind of operations. After remote connection establishment the Artix-7 TCSG card will respond to the commands given for controlling or monitoring the RF parameters.

Artix-7 TCSG card is provided with Clock (16 MHz), IPP +5V (DC) as inputs. TCSG card will generate four pulses for TR module operation and: Transmit Receive control, RF on/off, Cover Pulse, Blanking Control with respect to IPP reference. It will also provide controls for phase shifter (6bits) [4], attenuator (5bits) and +60V ON/OFF (one bit) of RF Circuit remotely using Optical Ethernet. TCSG monitors Power supplies; +60V, +28V and +5V (3bits) of the RF Circuit. This card generates interlock condition by monitoring five TTL parameters: VSWR, Excess RF IN, Excess Duty, two Junction Temperatures and monitors Forward Power and Reverse Power of the TR Module.

TCSG has got other features like In System Programmability, Watchdog functionalities. The former one is implemented using Ethernet Connectivity to erase and reprogram the Serial Flash, and other is implemented using a Microcontroller which will operate independently. Three 8-bit ADC channels of Microcontroller are used for analog parameter monitoring. The design of Artix-7 based FPGA is shown in the Figure.1, which includes the following components. The Xilinx Artix-7 XC7A35T FPGA in a 324 pin LFBGA package with 33,208 logic cells and about 210 user I/O lines are used to make the TCSG card. It has 256MB of DDR3 SDRAM, 16 data interfaces with a clock speed of 166.667 MHz Apart from the DDR3, it has 128MB of SPI serial Flash memory, which store the FPGA configuration and MicroBlaze code shadowing. The communication between the Radar controller and the Artix-7 FPGA is made via EthernetPHY. ATMEGA16L 8-bit microcontroller with three ADC channels with reference voltage 2.5V is also embedded in the TCSG card.

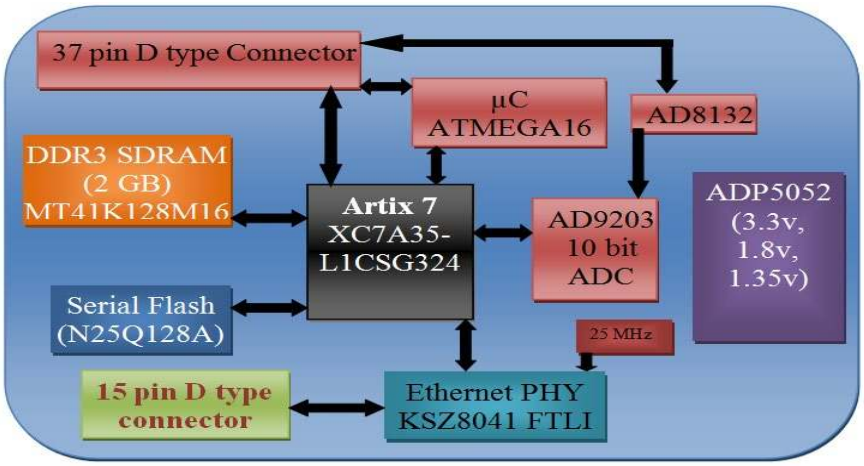

Figure 1. Complete block diagram of Artix-7 FPGA control card

3. Hardware implementation

3.1. EthernetPHY

The communication between the Radar Controller and TCSG is implemented using 10/100 Ethernet PHY [5] with media-independent interface (MII) support whose Ethernet media access control (MAC) is implemented in FPGA. Ethernet PHY uses an external 25MHz clock generated from FPGA for it operation.The Ethernet PHY interface is shown in the figure. 2

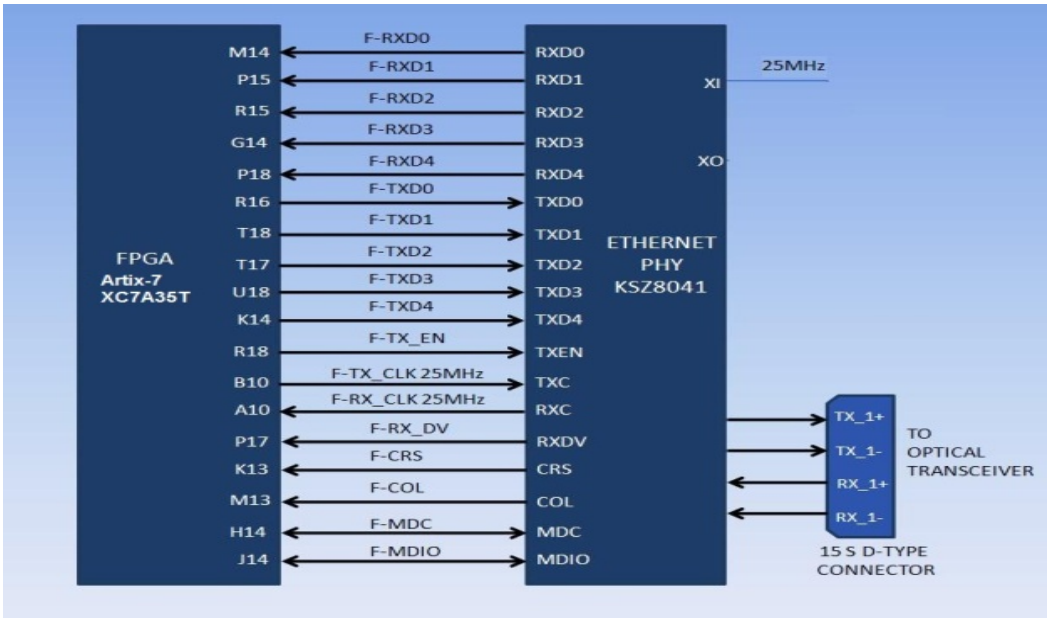

Figure 2. Ethernet PHY (KSZ8041FTLI) interface circuit on the TCSG card

The error–free transmission between FPGA and media access control (MACs) [6] is achieved via EthernetPHY KSZ8041FTLI. The EthernetPHY acts as a bridge between the MAC and FPGA by controlling the Ethernet transmits and receive data rate.
Ethernet PHY uses an external 25MHz clock generated from FPGA for its operation. EthernetPHY can be used for Optical as well as Copper Ethernet based interfaces. EthernetPHY provides high speed transceivers for higher band width support.

3.2. Analog to Digital Converter (ADC)

The Coupled forward power received from the TR modules is given as an input to the single ended AD 8132 and the amplified differential output is received from the output pin. This differential output is given to the AD 9203 multistage 10 bit ADC [7] as an input. This analog input is converted to a 10 bit (D0-D9) digital output and which is fed to the Artix-7 FPGA as an input signal for forward power level measurement. ADC interface with other circuit on the TCSG card is shown in figure. 3. This ADC is working on 20MHz clock frequency, with 40Msps sampling rate.

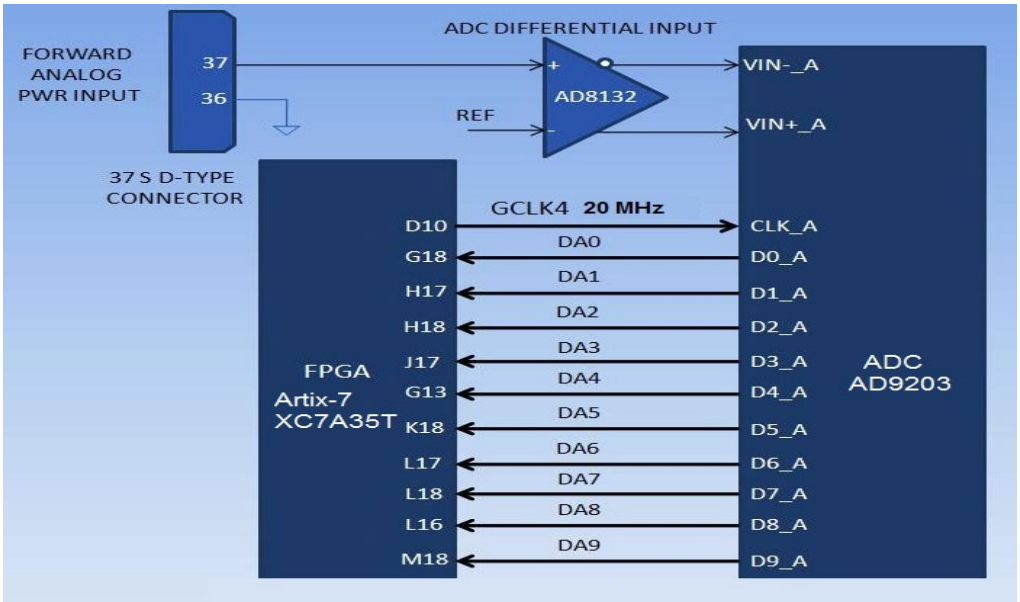

Figure 3.ADC interface with other circuit on the TCSG card

3.3. Micro-controller

ATMEGA 16L 8-bit microcontrollers [8] is used to read out the 60V DC voltage level and junction temperatures of the power amplifier MRF157 (pair) at the TR module as a monitoring circuit. In order to perform this, the 60V from the TR module is taped and it is step down to 3.3V by a potential divider circuit. This voltage and a reference voltage of 2.8V are given to the single supply quad comparator IC LM339m via pin no. 7 and 6 respectively. After comparing the two input voltages levels the non-inverting comparator output via pin no.1 given to the ATMEGA 16L in the microcontroller via pin no. 37. This voltage level is compared with the pre-defined voltage levels in the Artix-7 FPGA memory and it displays the corresponding voltage at radar controller via EthernetPHY. Figure.4 shows the Microcontroller interface with Artix-7 FPGA.

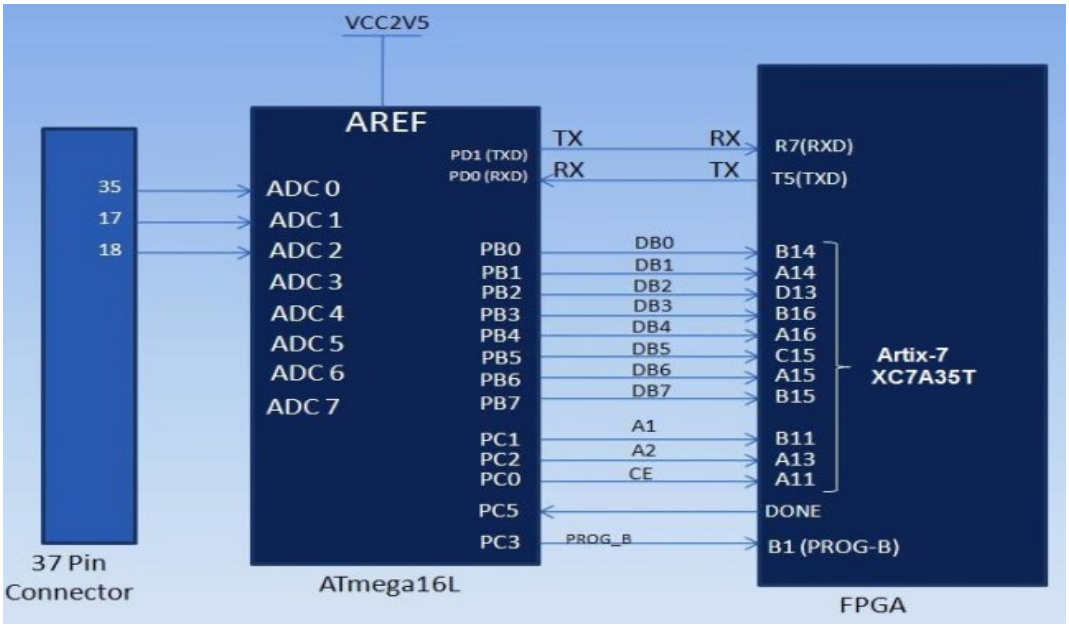

Figure 4. Microcontroller interface with Artix-7 FPGA

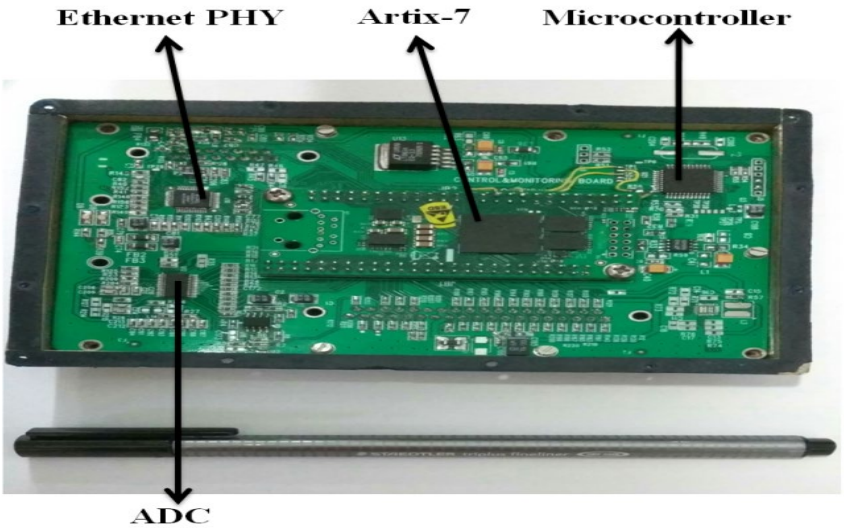

Figure 5. Hardware implementation of Artix-7 FPGA based control card

Figure.5 shows that hardware implementation of Artix-7 FPGA based control card which includes micro controller, Ethernet PHY, ADC and other circuitry. The junction temperatures of the MRF 157 power amplifier of both the IC's at TR module is continuously measured by positive temperature coefficient thermistor. This output is fed into the Low Power Programmable Temperature Controller (LPPTC) IC TMP01FS through pin no.5. The corresponding voltage level from the LPPTC is given to the microcontroller via pin no.35 and 36 respectively. These voltage levels are compared with the predefined values in the microcontroller and it will display the corresponding temperature in the radar controller PC. Figure.6 shows the Temperature scale and real time measurement.

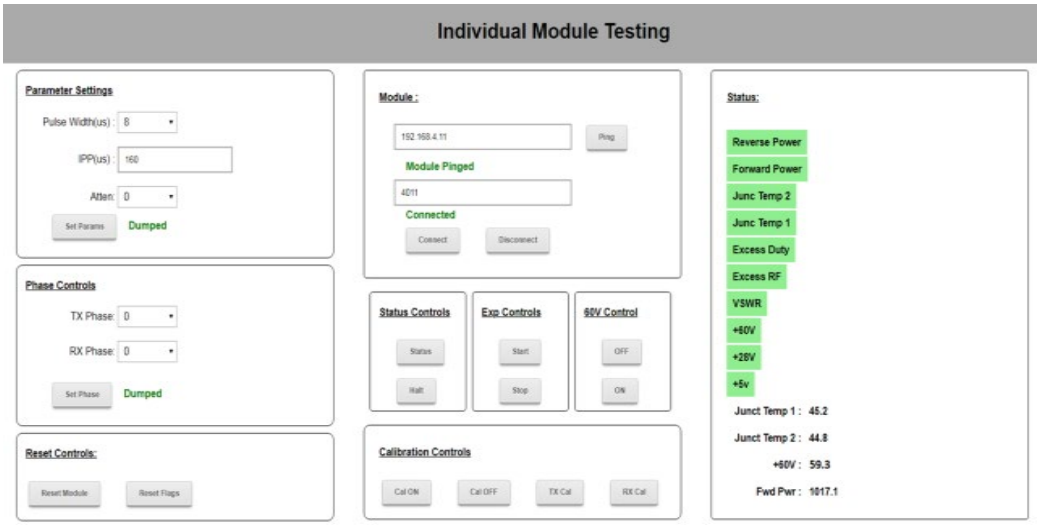

Figure 6.GUI screenshot of individual TR module testing

4. Microblaze microcontroller system software

All the peripherals (e.g. Ethernet PHY, UART), memory (e.g. HYPERRAM) and interfaces are implemented in MicroBlaze soft-core [9] CPU using Xilinx Platform Studio (XPS). There are two ways to setup FPGA architecture using an embedded MicroBlaze processor.

1. MicroBlaze be the top level of the design and add custom VHDL code as a MicroBlaze peripheral.
2. Custom VHDL [10] logic is the FPGA top level design and instantiate the MicroBlaze as a component.

The FPGA in the TCSG card is intended to be a logical array, which needs a CPU for some control or communication functions hence the second method is followed for FPGA architecture. The embedded processor system is then instantiated as a component in the top level VHDL design which is written in ISE Project Navigator. To communicate between Micro Blaze processor and top level VHDL design, a GPIO block is created in MicroBlaze as a memory address map and connected those signals in VHDL top level wrapper to do write/read from VHDL design. The proposed architecture is synthesized using Vivado 2017.4and is implemented on Artix-7 XC7A35T-2CSG324C customized FPGA board. The necessary software for this design is written using VHDL Behavioralmodeling for top level wrapperand C language is used for programming MicroBlaze processor, includes special C commands belongs to MicroBlaze's cores in addition to the conventional C language. Finally the combined bit file is downloaded to FPGA and initial simulations are carried out in Vivado.

5. Simulation and Results

Micro The output from the Artix-7 FPGA should be validated before implementing it in the real time operation. This has been achieved by carrying out simulations using the Vivado [11]. The simulated output from Vivado is shown in the figure. 7.

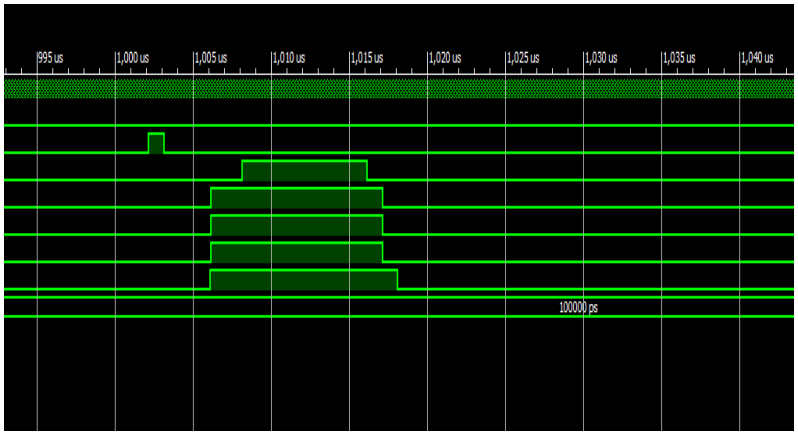

Figure 7. Simulated output from Vivado.

Artix-7 FPGA real time outputs of IPP, Tx pulse and Gate bias pulse for MRF157 power amplifier, RF ON/OFF, blanking pulse [12][13], T/R control and phase shifter are shown in figure.8 and figure.9.

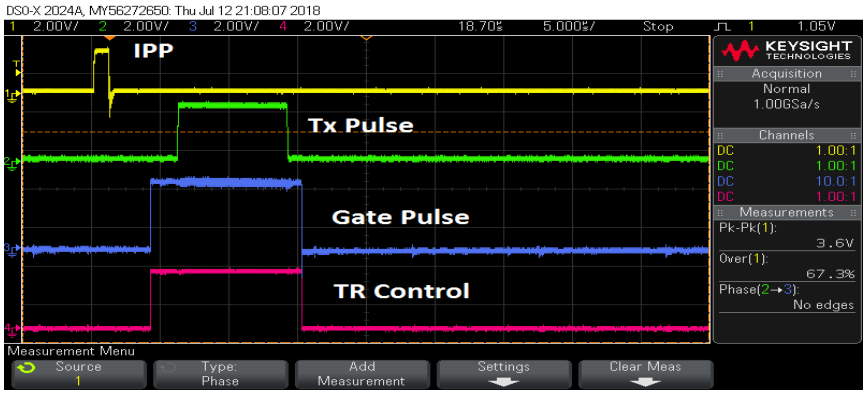

Figure 8. Real time output from Artix-7 FPGA

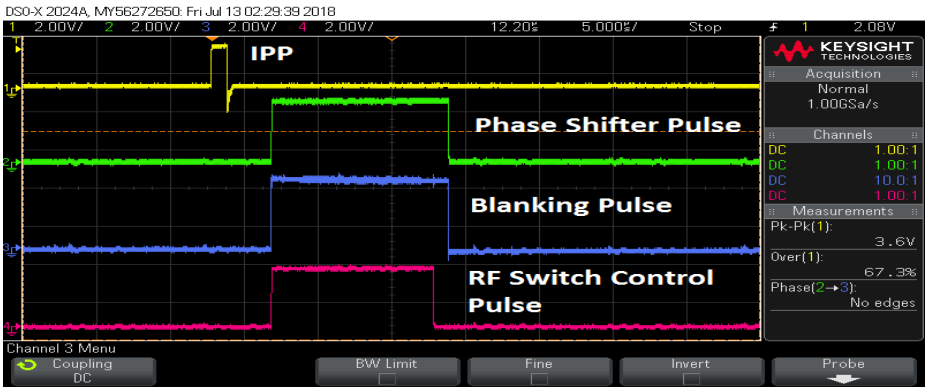

Figure 9. Real time output from Artix-7 FPGA

The messages are sent in JSON format and the message telemetry is storage in storage endpoint server for further analysis. The IoT hub can be connected to less than 100 devices (in simulation) and handles MQTT, HTTP protocols. The refresh time to update device state is also set in the configuration file.

6. Implementation details

The design and configuration of Artix-7 FGPA is tested and satisfactory performance has been noted. Thus, the Artix-7 FPGA is embedded in the TR module for the real time operation [14]. Individual 1kW TR module is shown in the figure. 10 and the hardware is shown in figure. 11.

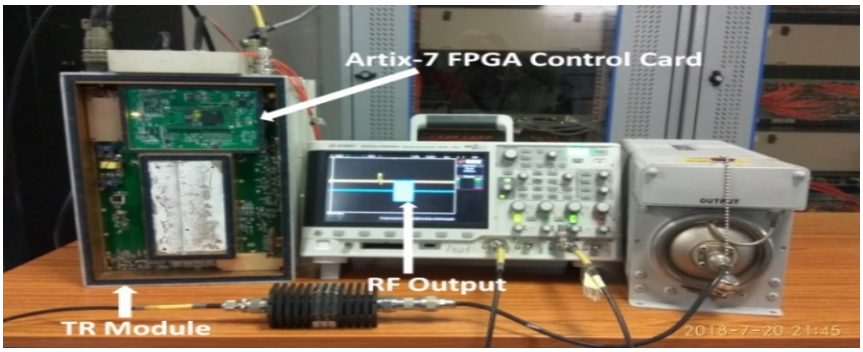

Figure 10. Individual 1kW TR Module

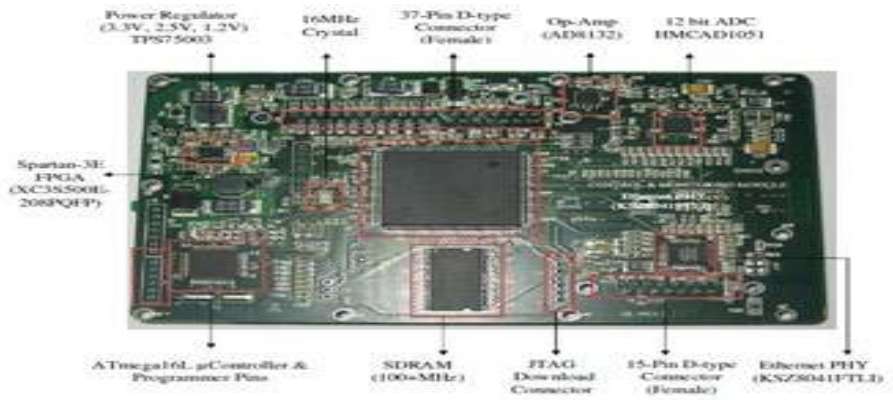

Figure 11. Hard ware picture

Functionality of the card is thoroughly tested with test bench setup equivalent to real time system. The results are found to be satisfactory as shown in figure.12.

Figure 12. Existing TCSG card Spartan 3E based

7. Conclusion

In this paper the full potential of Artix-7 FPGA in generation of control pulses is presented. Atrix-7 FPGA successfully embedded in the TR module for the real time operation. Ethernet PHY is used for the communications between the radar controller and the field located TR module. Fast and robust radar operation can achieve through the Artix-7 FPGA based control card.

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