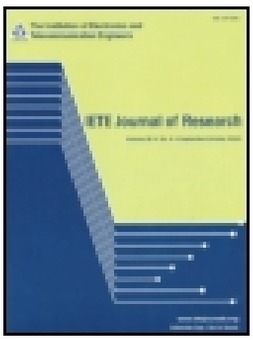

IETE Journal of Research

ISSN: 0377-2063 (Print) 0974-780X (Online) Journal homepage: http://www.tandfonline.com/loi/tijr20

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To cite this article: A. Karthikeyan & P.S. Mallick (2017): Transmission Gate as Buffer for Carbon-Nanotube-Based VLSI Interconnects, IETE Journal of Research, DOI: 10.1080/03772063.2017.1351316

To link to this article: http://dx.doi.org/10.1080/03772063.2017.1351316

Published online: 23 Aug 2017.

IETE JOURNAL OF RESEARCH, 2017
https://doi.org/10.1080/03772063.2017.1351316

Transmission Gate as Buffer for Carbon-Nanotube-Based VLSI Interconnects

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ABSTRACT

In this paper, we propose transmission gates (TGs) as buffers/repeaters for carbon nanotube (CNT)-based VLSI interconnects. Various performance metrics of the TG buffer, viz. propagation delay, crosstalk-induced delay, power dissipation, and power-delay product under super-threshold and sub-threshold conditions are analysed. Performance analysis of TG buffers with CMOS inverter buffers at various interconnect lengths and buffer insertion intervals is done. We have also analysed the performance of Single-wall carbon nanotube (SWCNT) bundle and three different configurations of mixed CNT bundles. By comparing the power-delay product of both the buffers, it is found that TG buffers are more suitable for applications in CNT-based integrated circuits.

KEYWORDS

Transmission gates; Inverter; Buffer; Delay; Power dissipation; CNT interconnects; Power-delay product

1. INTRODUCTION

Transmission gates (TGs) are well known for their applications in analogue switches, signal isolators, and logic circuits in microelectronic chips [1]. Their unique properties like immunity to input noise, good output swing, and less power dissipation make them ideal for low-power applications, especially as buffers in VLSI interconnects. Recent work shows low-power buffer design using four TGs inserted in an inverter circuit [2]. A new method is developed to calculate the repeater size and interconnect length to minimize the total interconnect power dissipation using CMOS inverter as repeater [3]. A smart driver using TGs has been preferred for repeater insertion [4]. The insertion of repeaters for three types of interconnects was compared by considering the impact of contact resistance [5]. Other than this, TGs have not got attention as buffers or repeaters in carbon nanotube (CNT)-based VLSI circuits, till date. CNT-based interconnects have gained prominence as the next-generation VLSI interconnects [6].

In this paper, we consider the design of a buffer circuit for CNT interconnects, made of TGs, and investigate its characteristics, viz. delay, power dissipation, and the power-delay product (PDP). We then compare the performance of CMOS inverters and transmission gate buffers for Single-wall carbon nanotube (SWCNT) bundle and mixed CNT bundle configurations. First, we discuss the working and operation of TG buffer circuit and then explain how it can act as a buffer in CNT-based VLSI interconnects.

2. TRANSMISSION GATE BUFFER

2.1 Transmission gate

A transmission gate (Figure 1(a)), or analogue switch, is defined as an electronic element that selectively blocks or passes a signal level from the input to the output. Also, it is known that an nFET and pFET cannot pass a strong logic 1 and logic 0 voltages, respectively [1]. So, by connecting the two devices in parallel, the full voltage range from 0 V to V_{DD} can be transmitted.

A TG buffer is designed with two TGs: TG1 and TG2 connected in series as shown in Figure 1(b). A CMOS inverter is used for complementary inputs to the gate terminals of the two TGs. When V_{in} is high, TG1 is ON as both the transistors are powered by the input signal and logic 1 is transferred to V_{out}. In the same fashion, when V_{in} is low, TG2 is ON due to the complementary inputs from the inverter, thereby transferring logic 0 to V_{out}. So a TG can take a weak signal from interconnect, buffer it, and transmit to the next interconnect stage. Based on this principle, we propose to use the TG as a buffer in CNT-based VLSI interconnects.

2.2 ESC modelling of SWCNT bundle interconnects

SWCNT-based equivalent single conductor (ESC) model was used to predict the time-domain performances of interconnects [7]. Another model using multi-ESC (MESC) was proposed for the transient analysis of coupled interconnects using SWCNT bundles or MWCNTs

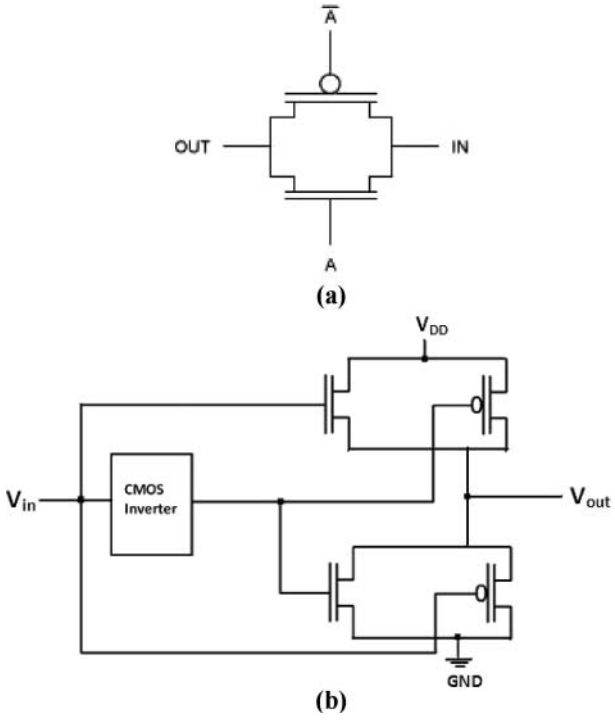

Figure 1: (a) Transmission gate. (b) TG buffer circuit

[8]. Performances of mixed CNT bundle interconnects for various configurations were analysed using ESC model [9,10]. Dynamic crosstalk for the mixed CNT bundle interconnects has been analysed, using ESC model for bundled SWCNT and MWCNT [11] and for MWCNT bundles with different number of shell arrangements [12]. A novel ESC model using square matrix approach shows that the delay reduces for the highest number of shells in MWCNTs [13]. ESC model is also used for the analysis of mixed CNTs of different tube densities [14]. Impact of intershell tunnelling conductance using ESC model [15] and imperfect contact resistance are investigated using ESC and multiconductor circuit (MCC) model [16]. ESC model has been used for the analysis of delay, crosstalk, and power dissipation. Most of these works were concentrated on CNT interconnects using ESC model. Our proposed work uses the ESC model for the SWCNT bundle interconnects. Here the comparison of TG as buffer and CMOS inverter as buffer using ESC model of SWCNT bundle interconnects was analysed. Analysis of the behaviour of TG must be accompanied with benchmarking of its performance. So, we choose CMOS inverter-based buffers [17] for comparing its delay, power dissipation, and the PDP with that of TG buffers. We analyse the behaviour of TG and CMOS inverter in an SWCNT bundle interconnecting as driver and load as shown in Figure 2(a). We also analyse the behaviour of TG and CMOS inverter as buffers. The ESC model of SWCNT bundle is

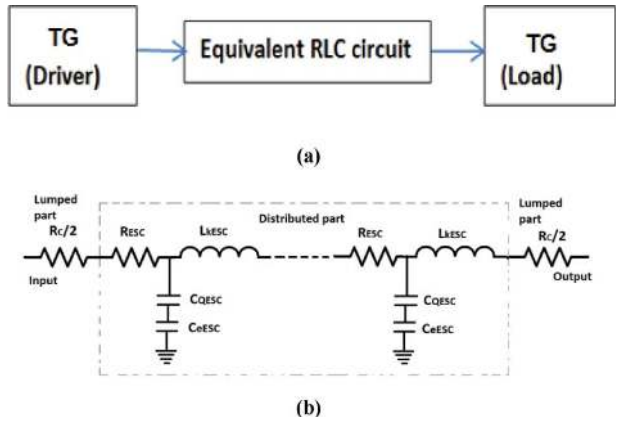

Figure 2: (a) TG as load and driver. (b) ESC model of CNT

shown in Figure 2(b). It is now well known that cNTs have emerged as the choice of interconnect for next-generation integrated circuits. So, we consider an SWCNT bundle shown in Figure 3, which consists of height and width as H_B and W_B that have a diameter of d = 1 nm and spacing between CNT is 0.34 nm. The centre-to-centre distance between neighbouring CNTs is S = 1.34 nm. h is the distance of SWCNT bundle from the ground plane.

The number of SWCNTs in the bundle was computed based on Equation [10]:

$$n_{\text{CNT}} = \begin{cases} n_W n_H - (n_H/2) & n_H \text{ is even} \\ n_W n_H - [(n_H - 1)/2] & n_H \text{ is odd} \end{cases} \quad (1)$$

where

$$n_W = \left[\frac{W_B - d}{S}\right] \quad \text{and} \quad n_H = \left[\frac{H_B - d}{S}\right] \quad (2)$$

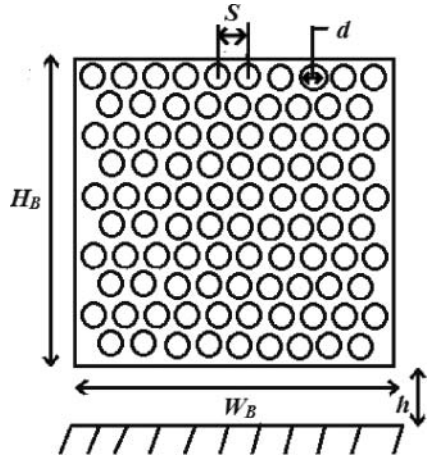

Figure 3: SWCNT bundle from the ground plane

n_W and n_H represent the number of rows and columns, and n_{CNT} is the total number of SWCNTs in the bundle.

The ESC resistance of a bundle with conducting SWCNTs is given by

$$R_b = \frac{R_{SWCNT}}{n_B} = \frac{R_C + R_Q}{n_B} + \frac{R_Q}{n_B}\frac{L}{\lambda_{eff.AC.OP}} \tag{3}$$

where R_C is the diameter-dependent imperfect metal-contact resistance, R_Q is the intrinsic quantum resistance of a CNT which is 6.45 kΩ/μm and is described earlier, n_B is the number of CNTs in the bundle, λ_{eff} is the effective mean free path considering the temperature-dependent acoustic (AC) and optical (OP) phonons. The intrinsic quantum capacitance of a CNT that arises due to the density of states (DOS) at Fermi level is given as [18]

$$C_Q = \frac{4e^2}{h\upsilon_F} = 400 \text{ aF/μm} \tag{54}$$

Further, the electrostatic capacitance between the CNT bundle and the substrate must be considered. So, the total equivalent single conductor capacitance associated with a bundle of CNTs is given by

$$C_{ESC} = \left(\frac{1}{C_{eESC}} + \frac{1}{C_{QESC}}\right)^{-1} \tag{5}$$

where $C_{QESC} = 4n_B C_Q$ and $C_{eESC} = \frac{2\pi\varepsilon}{\cosh^{-1}(y/d_g)}$; y is the distance between the centre of CNTs facing the ground, d_g is the diameter of those CNTs in the bundle. Lastly, the equivalent single conductor kinetic inductance of a CNT bundle is given as

$$L_{kESC} = \frac{L_k}{n_B} \tag{6}$$

where

$$L_k = \frac{h}{2e^2\upsilon_F} = 8 \text{ nH/μm} \tag{7}$$

A pulsed signal of width 2 ns and duration of 4 ns with small rise and fall time of 0.001 ns is given as input. By selecting small values of rise time and fall time, we were able to analyse the output pulse accurately. The simulation is carried out for 1 GHz input frequency using Silvaco Smart SPICE. Performance analysis was carried out for various metrics as discussed below.

2.3 ESC modelling of mixed CNT bundle interconnects

Mixed CNT bundles are the combination of SWCNT and MWCNT bundles. Here we have done the analysis using mixed CNT bundles. Figure 4 shows the ESC modelling of mixed CNT bundle interconnects. Performance of mixed CNT bundle interconnects is better than the SWCNT and MWCNT bundle-based interconnects [19]. Crosstalk-induced delay for a mixed CNT bundle is lesser than SWCNT or MWCNT bundles [20]. Performance of CNT bundles is investigated and shown that mixed CNT bundles are more tolerant to process variations at global interconnect lengths [21].

The ESC models are analysed by the total number of conducting channels (N_{tot}) of SWCNTs or MWCNTs in a bundle. The N_{tot} can be expressed as

$$N_{tot} = \sum_{j=1}^{n_{CNT}} N_j; \quad \text{where} \quad N_j = \sum_{j=1}^{n_s} N_i D_i \tag{8}$$

n_s represents the number of shells in MWCNT, n_{CNT} represents the total number of SWCNTs or MWCNTs in a bundle.

The equivalent contact resistance of CNT bundle can be expressed as

$$R_{c,ESC} = \left[\sum_{j=1}^{n_{CNT}} \left(\sum_{i=1}^{n_s} \left(\frac{R_{q,i}}{2N_i} + R_{mc,i}\right)^{-1}\right)\right]^{-1} \tag{9}$$

The equivalent scattering resistance r_{ESC} in *p.u.l* can be expressed as

$$r_{ESC} = \left[\sum_{j=1}^{n_{CNT}} \left(\sum_{i=1}^{n_s} \frac{2N_i}{R_{q,i}}\lambda_{mfp,i}\right)\right]^{-1} \tag{10}$$

The equivalent quantum capacitance of the CNT bundle can be expressed as

$$c_{q,ESC} = 2N_{tot}c_{q0} \tag{11}$$

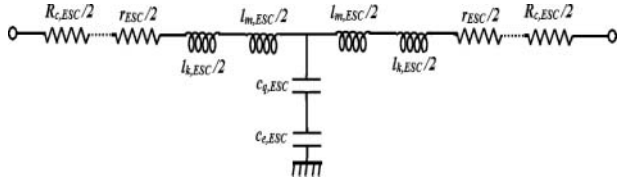

Figure 4: ESC model of mixed CNT bundle interconnect [14]

The equivalent electrostatic capacitance $C_{e,\mathrm{ESC}}$ is due to the potential difference between the CNT bundle and the ground plane. The $C_{e,\ \mathrm{ESC}}$ can be expressed as

$$c_{e,\mathrm{ESC}} = \frac{2\pi\varepsilon_0\varepsilon_r}{\cosh^{-1}[(D_\mathrm{s} + 2h_t)/D_\mathrm{s}]} \times N_x, \tag{12}$$

where N_x represents the number of SWCNTs or MWCNTs facing the ground plane. The equivalent kinetic ($l_{k,\ \mathrm{ESC}}$) and magnetic inductances ($l_{m,\mathrm{ESC}}$) in *p.u.l* can be expressed as

$$l_{k,\mathrm{ESC}} = \frac{l_{k0}}{2N_\mathrm{tot}}, \tag{13}$$

$$l_{\mathrm{m.ESC}} = \frac{1}{N_x}\left[\frac{\mu_0}{2\pi}\cosh^{-1}\left(\frac{D_\mathrm{s} + 2h_t}{D_\mathrm{s}}\right)\right] \tag{14}$$

Three different bundle configurations of SWCNTs and MWCNTs in a mixed CNT bundle as shown in Figure 5 are considered for analysis [10]. MCB-I has a random distribution of SWCNTs and MWCNTs in the bundle. MCB-II has the distribution of SWCNTs placed at the periphery to the centrally located MWCNTs. MCB-VI has the distribution of SWCNTs at the centre and MWCNTs at the periphery. The interconnect parasitics of various bundle topologies are shown in Table 1.

3. DELAY AND POWER DISSIPATION ANALYSIS

3.1 Delay analysis

Signal integrity in VLSI interconnects is of paramount importance as the data must be faithfully transmitted to the next section. Simulations were done based on the ITRS recommendations at 22 nm technology node [8]. We have analysed the crosstalk-induced delay for the buffers using the ESC model of SWCNT as shown in Figure 2(b). An RC circuit with R = 300 Ω and C = 1 fF, which induces crosstalk at the input signal, is used. The alternating action of TG1 and TG2 is coupled with the parallel connection of the FETs that suppresses the crosstalk noise. However, the crosstalk-induced delay is slightly more for TG at 0.303 ps as compared to the CMOS inverter delay of 0.18 ps for both sub-threshold and super-threshold conditions. Later, we carry out the analysis with TG and CMOS inverter, respectively, and the driver and buffer of the interconnect using ESC model of mixed CNT bundle is shown in Figure 4. The analysis is performed for different bundle configurations [10] of SWCNTs and MWCNTs in mixed CNT bundle as shown in Figure 5. Figure 6(a) and (b) shows the propagation delay of CMOS and transmission gate,

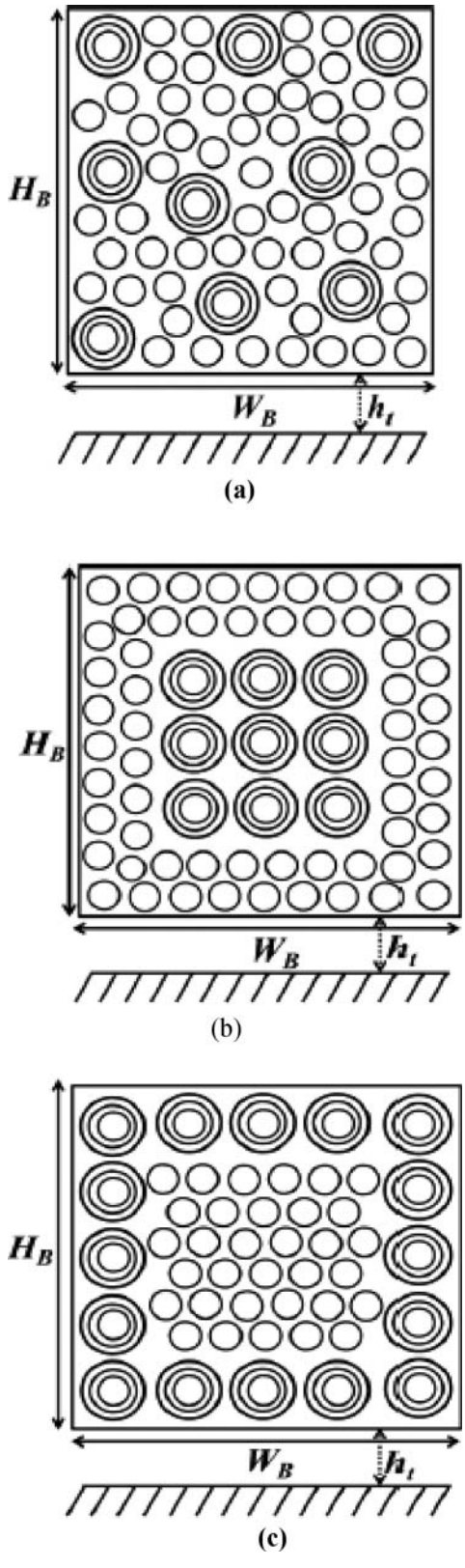

Figure 5: Three different bundle configurations of SWCNTs and MWCNTs in (a) MCB-I, (b) MCB-II, (c) MCB-VI [10]

Table 1: Interconnect parasitics for the different CNT bundle topologies [10]

Interconnect parasitics	SWB	MCB-I	MCB-II	MCB-VI
R_{cESC} (KΩ)	3.20	3.22	3.20	3.20
r_{ESC} (Ω/μm)	1.49	1.28	1.13	0.79
L_{kESC} (pH/μm)	3.73	2.84	2.12	1.21
L_{eESC} (pH/μm)	44.06	57.21	25.04	35.28
C_{qESC} (pF/μm)	0.96	1.09	1.46	0.83
C_{eESC} CM(aF/μm)	584.84	342.34	584.84	62.83

respectively, for various interconnect lengths at super-threshold (V_{DD} = 1 V) region. Figure 7(a) and (b) shows the propagation delay of CMOS and transmission gate, respectively, for various interconnect lengths at sub-threshold (V_{DD} = 0.5 V) region. In all the cases, it can be seen that the delay increases with the wire length. However, the increase in propagation delay of the TG when compared to the inverter is due to more (six) number of FETs in TG as compared to four FETs in an inverter. It is also observed that there is a reduction in delay for

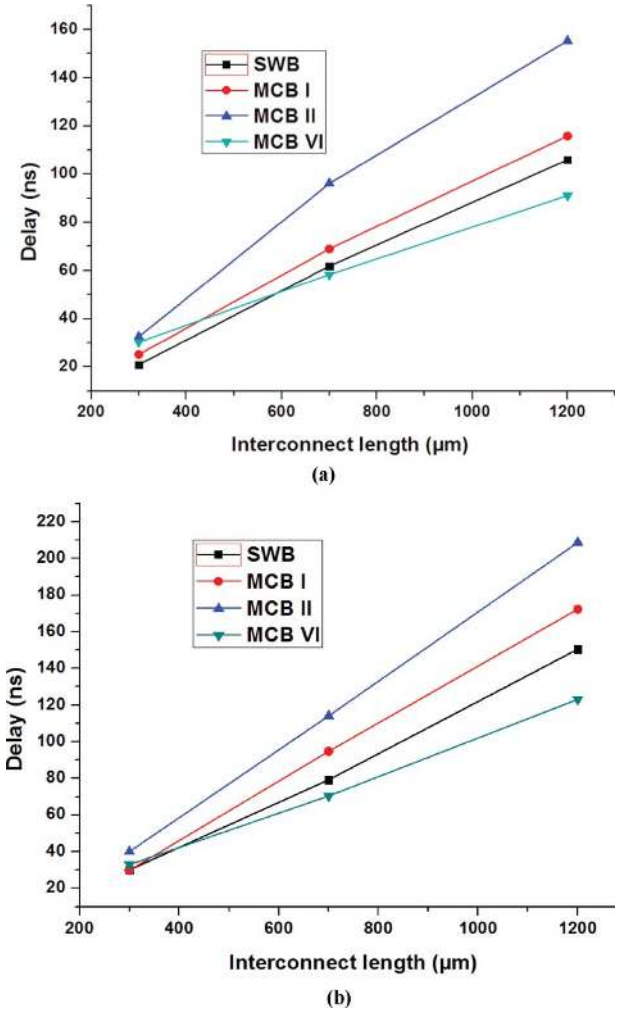

Figure 6: (a) Delay of interconnects using CMOS driver at various interconnect lengths for super-threshold region. (b) Delay of interconnects using transmission gate driver at various interconnect lengths for super-threshold region

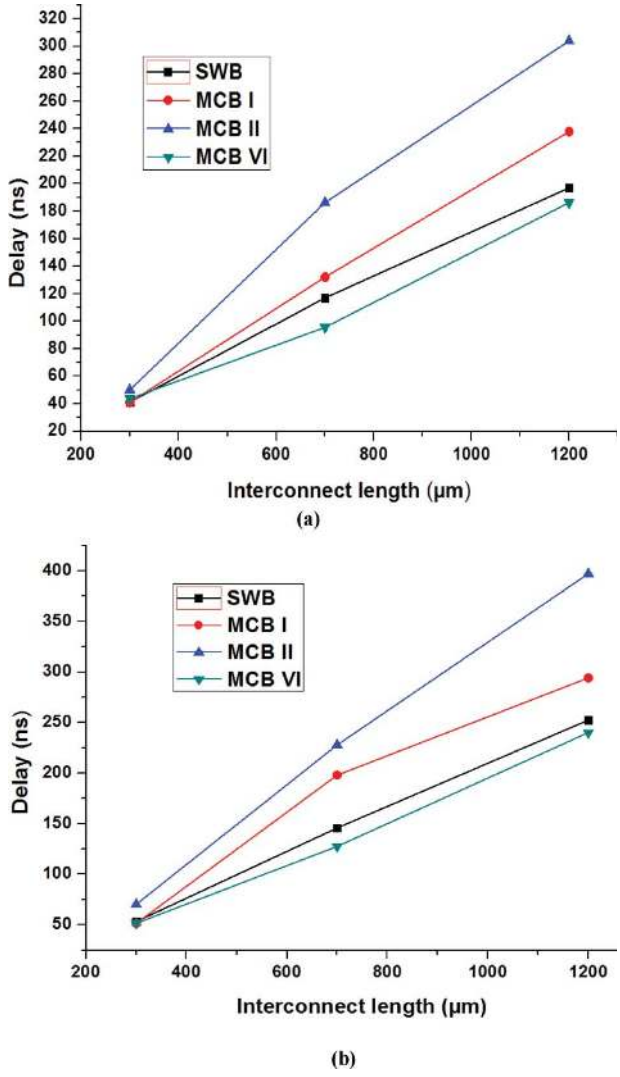

Figure 7: (a) Delay of interconnects using CMOS driver at various interconnect lengths for sub-threshold region. (b) Delay of interconnects using transmission gate driver at various interconnect lengths for sub-threshold region

MCB VI, where the MWCNTs are placed at the periphery of the centrally located SWCNT. MCB VI is also suitable for global interconnects for reduced delay in case of CMOS drivers or transmission gate drivers. MCB VI also has lesser delay in both super-threshold and sub-threshold operating regions. Buffer insertion is a common technique for the reduction of delay in the Interconnects.

The delay in an interconnect is linearly proportional to the square of its length [1]. Operating the devices at sub-threshold is necessary for low power consumption [22]. Low-power operation may increase the delay of the signal in global interconnects. Inserting buffer is necessary to reduce the length of the interconnects. Figure 8(a) and (b) shows the delay of interconnects using CMOS and transmission gate as buffers, respectively, for various

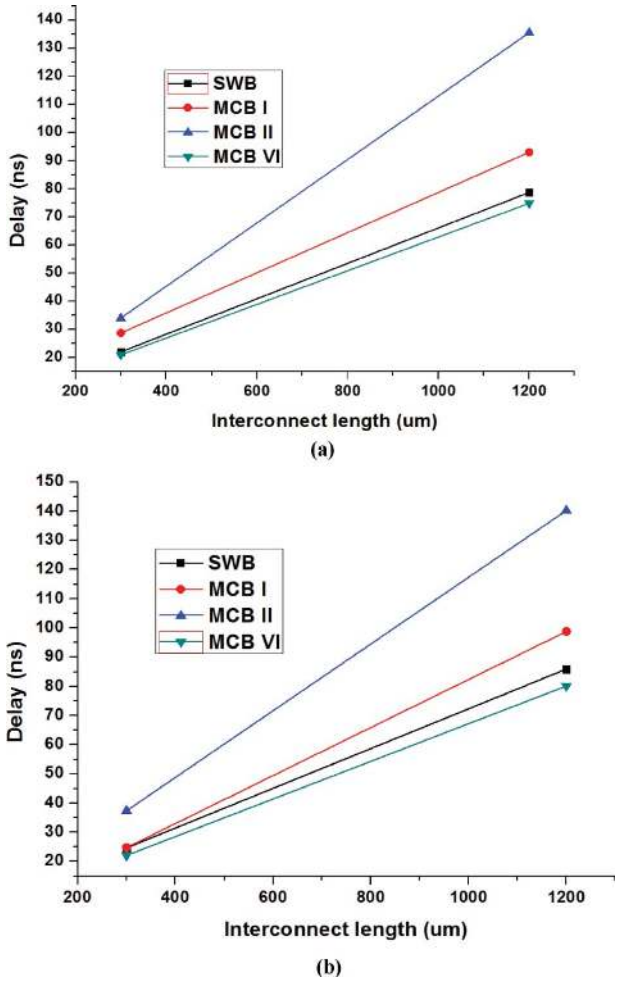

Figure 8: (a) Delay of interconnects using CMOS inverter as buffer at various interconnect lengths for super-threshold region. (b) Delay of interconnects using transmission gate as buffer at various interconnect lengths for super-threshold region

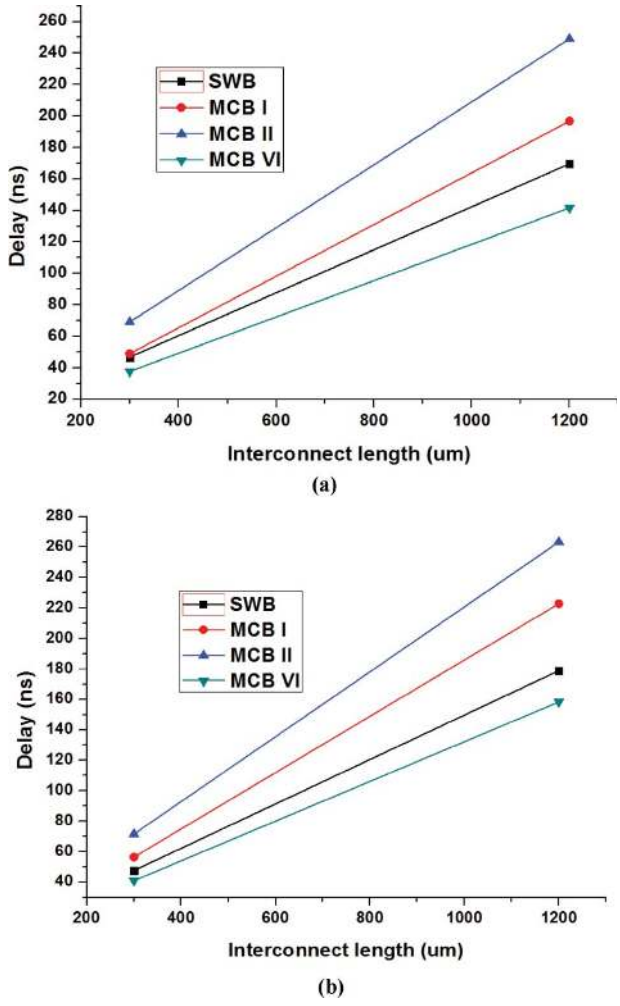

Figure 9: (a) Delay of interconnects using CMOS inverter as buffer at various interconnect lengths for sub-threshold region. (b) Delay of interconnects using transmission gate as buffer at various interconnect lengths for sub-threshold region

bundle configurations of interconnects at super-threshold region. Figure 9(a) and (b) shows the delay of interconnects using CMOS and transmission gate buffers at sub-threshold region. In both the cases, the delay is slightly more for transmission gate buffers. Comparing the delay of interconnects with buffers and without buffers, transmission gate buffers have more reduction of delay compared to transmission gate as drivers, but the overall delay is more for transmission gate buffers compared to the CMOS inverters as buffers. The delay of mixed CNT bundle configuration MCB VI is lesser in both the cases. Performance of CMOS inverters in terms of delay is better than the Transmission gate at any operating regions. After buffer insertion, the performance of MCB VI which has a distribution of MWCNTs in the periphery and SWCNTs at the centre has lesser delay than other configuration due to the low parasitic resistance and inductance [10]. Here all the shells of MWCNTs conduct which leads to lesser delay.

3.2 Power dissipation analysis

Power dissipation is an important issue in integrated circuits. Both transistors and interconnects dissipate power due to current conduction (static power) and switching action (dynamic power). However, interconnects dissipate more power due to high resistance at scaled technologies. So, there is a need to compensate power dissipated by interconnects. Power dissipation increases for the increase in the length of the interconnect. By inserting buffers, we can maintain the output power at desired levels for various lengths.

More specifically, local interconnects have lesser power dissipation compared to global interconnects. Figure 10(a) and (b) shows the power dissipation of CMOS buffers and transmission gate buffers at super-threshold region. Comparing both the cases, the power dissipation of transmission gate buffer is lesser than the power dissipation of

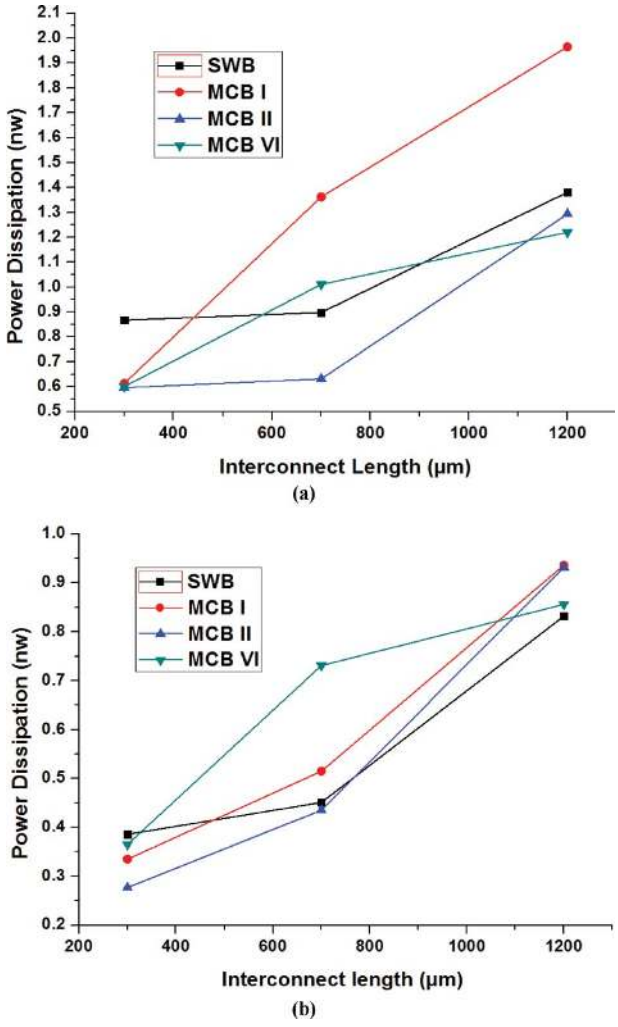

Figure 10: (a) Power dissipation of CMOS driver for super-threshold region. (b) Power dissipation of transmission gate driver for super-threshold region

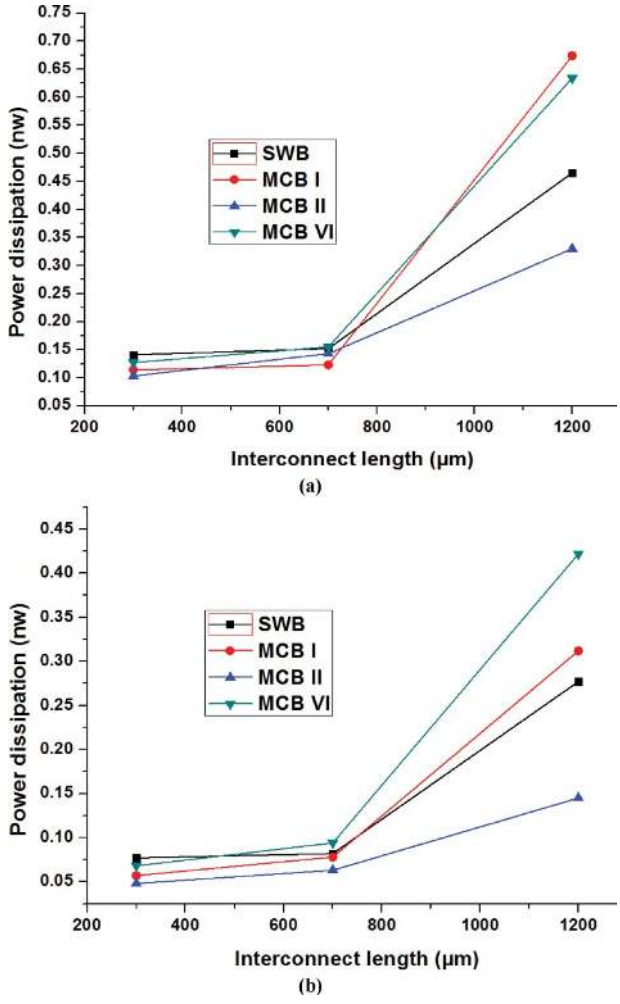

Figure 11: (a) Power dissipation of CMOS driver for sub-threshold region, (b) Power dissipation of transmission gate driver for sub-threshold region

CMOS buffer. Figure 11(a) and (b) shows the power dissipation of CMOS driver and transmission gate driver during sub-threshold region of operation. Power dissipation at sub-threshold region of operation is still lesser for transmission gate compared to CMOS driver. CMOS buffers and transmission gate buffers are inserted for reducing the delay and power dissipation. Tables 2 and 3 show the power dissipation of CMOS and transmission gate buffers at super-threshold region and sub-threshold region, respectively, with the buffer insertion intervals. In both the cases, the power dissipation of transmission gate buffers is lesser. Insertion of buffers may reduce the propagation delay but the power dissipation slightly increases due to the additional transistors.

During faster switching conditions, CMOS inverter buffers dissipate more power due to short circuit. Transmission gates have parallel connection of transistors. While fast switching of the logic signal, one of the transmission gates TG1 or TG2 is ON at a time. The chances of short circuit are lesser, due to that transmission gates have lesser power dissipation.

The power dissipation of transmission gate buffer is lesser than the CMOS buffer. Voltage scaling is necessary for reducing the power dissipation [2].

Table 2: **Power dissipation at super-threshold region for CMOS buffer and transmission gate buffer**

Type of bundle [10]	Buffer insertion interval (um)	Power dissipation (nW)	
		CMOS buffer	Transmission gate buffer
SWB	100–100–100	0.790	0.475
MWB I		0.620	0.251
MWB II		0.512	0.413
MWB VI		0.766	0.609
SWB	400–400–400	1.795	1.452
MWB I		1.964	1.660
MWB II		1.548	1.422
MWB VI		1.952	1.758

Table 3: Power dissipation at sub-threshold region for CMOS buffer and Transmission gate buffer

Type of bundle [10]	Buffer insertion interval (um)	Power dissipation (nW)	
		CMOS buffer	Transmission gate buffer
SWB	100–100–100	0.082	0.054
MWB I		0.159	0.041
MWB II		0.070	0.071
MWB VI		0.101	0.091
SWB	400–400–400	0.295	0.249
MWB I		0.242	0.198
MWB II		0.094	0.041
MWB VI		0.281	0.218

During sub-threshold operation, the power dissipation is lesser than the super-threshold operation. The performances of transmission gate buffers are better than CMOS as buffers in both super-threshold and sub-threshold regions. In the sub-threshold region, buffer insertion using transmission gate is more feasible. By comparing the power dissipation in both the operating regions, mixed CNT bundle MCB II with transmission gates as drivers or buffers has lesser power dissipation. The capacitance of MCB II which has SWCNT bundles at the outer and MWCNTs at the inner is lesser, since all the shells of MWCNTs cannot conduct, and lesser capacitance leads to lesser power dissipation.

4. POWER-DELAY PRODUCT

The ultimate factor that can measure the performance of a TG buffer is its PDP. We calculate the PDP as the product of power dissipated and the delay of interconnect. PDP is calculated with and without buffer insertion for the interconnect at various lengths at super-threshold and subthreshold conditions. Figure 12(a) shows the PDP of CMOS inverter and transmission gate as driver in super-threshold region. Figure 12(b) shows the PDP of CMOS inverter and transmission gate as buffer in super-threshold region of operation. Figure 13(a) shows

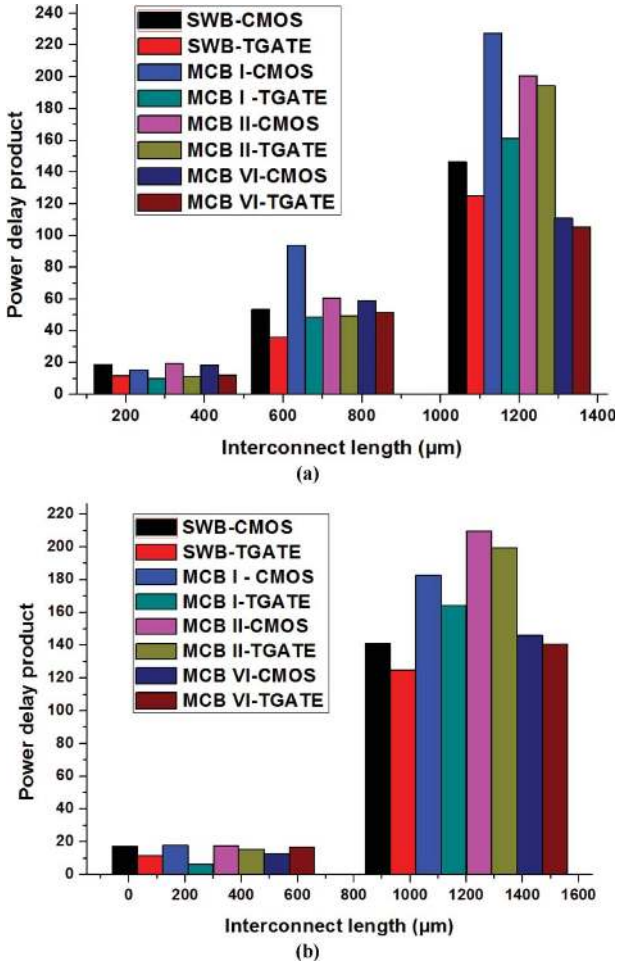

Figure 12: (a) Power delay product of CMOS inverter and transmission gate as driver in super-threshold region. (b) Power delay product of CMOS and transmission gate as buffer in super-threshold region

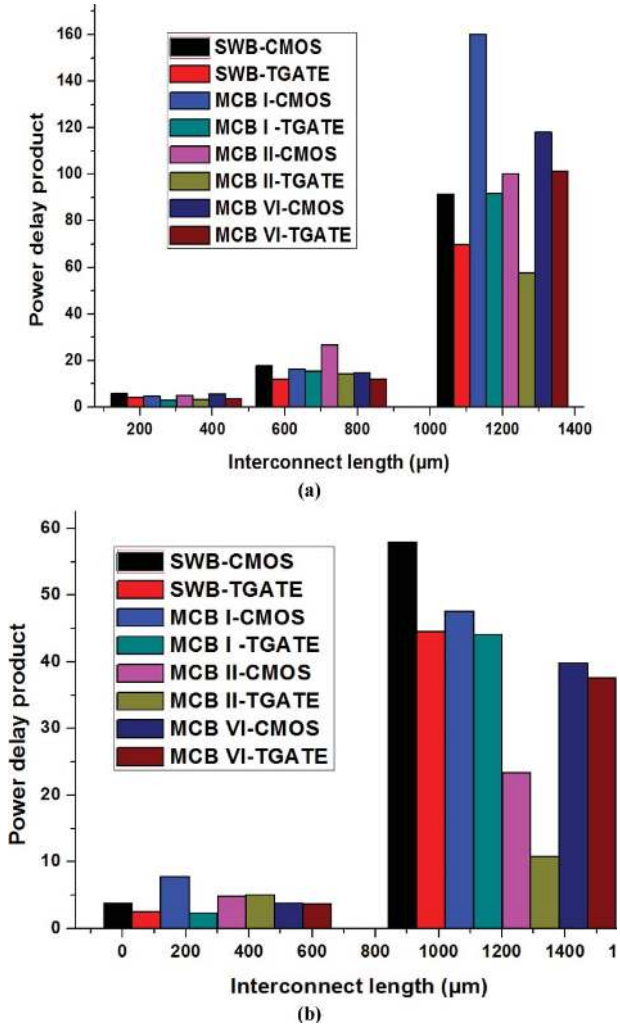

Figure 13: (a) Power delay product of CMOS inverter and transmission gate as driver in sub-threshold region. (b) Power delay product of CMOS and Transmission gate as buffer in sub-threshold region

the PDP of CMOS inverter and transmission gate as driver in sub-threshold region. Figure 13(b) shows the PDP of CMOS inverter and transmission gate as buffer in sub-threshold region of operation. PDP of transmission gate buffer is lesser for all the different configurations of CNT bundles. Mixed CNT bundles outperform SWCNT bundle in terms of delay. MCB VI has lesser delay in all the cases; MCB II has lesser power dissipation and also has lesser PDP with transmission gate as buffer or driver at sub-threshold conditions. Transmission gate buffers perform better in all the three levels of interconnect, and more suitable for mixed CNT bundle interconnects at the global level for sub-threshold operation. However, as the technology progresses, integrating a few thousand more transistors for TG-based circuits as compared to CMOS inverter-based circuits is not a major problem.

5. CONCLUSION

This paper proposes the utilization of TG buffers for CNT-based interconnects for VLSI circuits. Performance metrics like delay, power dissipation, and power delay product are analysed and compared at various interconnect lengths ranging from 300 to 1200 μm. CMOS buffers and TG buffers are implemented for SWCNT bundles and mixed CNT bundles. From the PDP analysis, we found that TG buffers are more suitable for sub-threshold applications in global interconnects (l = 1200 μm) and also more suitable for mixed CNT bundle interconnects.

DISCLOSURE STATEMENT

No potential conflict of interest was reported by the authors.

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