Journal of ELECTRONIC MATERIALS
https://doi.org/10.1007/s11664-019-07431-z

Triangular Carbon Nanotube Bundle Interconnects for Subthreshold VLSI Circuits

P. UMA SATHYAKAM[1,2] and P.S. MALLICK[1,3]

1.—School of Electrical Engineering, Vellore Institute of Technology, Vellore, Tamil Nadu 632014, India. 2.—e-mail: umasathyakam.p@vit.ac.in. 3.—e-mail: psmallick@vit.ac.in

Triangular carbon nanotube (T-CNT) bundles are proposed as long interconnects for subthreshold VLSI circuits. The performance of subthreshold interconnects depends on the intrinsic quantum and electrostatic coupling capacitances of the interconnects. Proposed T-CNT bundles have the most optimum geometry that give least possible coupling capacitance between adjacent wires in an IC. First, we describe the T-CNT bundle models and of traditionally used square/rectangular CNT bundles for comparison. The subthreshold output current of an inverter is modelled, and hence, we find the optimum transistor widths for nFET and pFET that drives the subthreshold interconnects. This is carried out by the current-over-capacitance ratio approach, where the subthreshold current and the transistor output capacitance are considered. Then, we model the interconnects using equivalent single conductor models and find their propagation delay and power dissipated. The performance factors such as crosstalk-induced delay, power delay product and victim noise levels of capacitive coupled interconnects of T-CNT bundles are compared to traditionally used square/rectangular CNT bundles for lengths ranging from 500 μm to 2000 μm. We find that T-CNT bundles outperform square/rectangular CNT bundles.

Key words: Carbon nanotubes, crosstalk, interconnects, noise, subthreshold, VLSI circuits

INTRODUCTION

Subthreshold operation of integrated circuits (ICs) is the current requirement of the portable electronics industry.[1,2] The design perspective of next generation devices and interconnects is shifting from performance centric approach to low-power-operation centric approach.[3,4] This is because today's market is driven by portable consumer and medical electronic devices that must consume less power as they operate on batteries. Futuristic Field Programmable Gate Arrays (FPGAs) are also found to be ideal candidates for low power interconnects.[5] However, interconnects have become the performance deciding factor in integrated circuits due to their scaling down, which increases their resistivity.

Further, scattering of electrons due to grain boundaries, edge roughness and phonons can drastically reduce the reliability of interconnects. So, it is perceived that scaled down interconnects cannot perform satisfactorily at subthreshold voltages.[3] As the dimensions shrink, it is better to reduce the operating voltage, which decreases current density thereby reducing the risk of self-heating in ICs. For copper interconnects, whose aspect ratio is considered 2 for global interconnects at scaled technologies, the wire capacitance (C_W) and the wire resistance (R_W) dominates over the driver capacitance (C_{driv}) and driver resistance (R_{driv}) at subthreshold voltages.[3] This is not desirable and lead to higher delay in interconnects.[3]

(Received April 1, 2019; accepted July 4, 2019)

Published online: 16 July 2019

In the case of carbon nanotube (CNT) interconnects, the diameter and tube separation effects the resistance and capacitance of the CNT bundles.[6] The capacitance of a CNT bundle increases as the diameter of the CNTs in the bundle increase. This is because the number of conducting channels increases with diameter.[6] Moreover, the tube separation influences the overall resistance of the CNT bundle. If the tube density is greater, the resistance of the bundle decreases and vice versa.[6]

Recently, many works are done on modeling and crosstalk analysis of CNT bundle interconnects.[7–12] It was found that CNT interconnects can suffer from crosstalk-induced delay and noise at highly scaled down technologies. Further, at subthreshold voltages, CNT interconnects operate very slowly due to the small currents in them.[13–15] So, it is necessary to design CNT bundle interconnects that carry maximum current and have minimum crosstalk during subthreshold operation.

Many techniques are proposed for improving the performance of interconnects at subthreshold currents. Current mode signaling was found to improve the performance of interconnects when the receivers are designed with low impedance.[14] Shielding of interconnects was also found to be helpful in reducing the crosstalk in interconnects.[15] Polymer-based ultra-low-k dielectrics can be used to reduce the coupling capacitance between CNT interconnects.[16] CNT/air-gap interconnects are also possible in this regard.[17] Nevertheless, one of the biggest advantages of CNT bundles is that, unlike Cu wires, CNTs can be arranged in different shapes such as circular, triangular, hexagonal and so on, in a CNT bundle. Among these geometries, the triangular cross section CNT bundles, when placed adjacently, are least coupled capacitively.[18] This is very important as the coupling capacitance and hence the crosstalk-induced delay can be reduced significantly in CNT interconnects.[10] Further, recent work by Wang et al.[19] shows the fabrication of "V" shaped trenches by dry etching on Si substrate for device applications. So, CNT bundles can be grown in "V" shaped trenches on Si substrates so that they can be used as triangular cross sectioned interconnects. Further, dielectrophoresis based separation of metallic CNTs from semiconducting CNTs, and precise placement of CNTs on substrate was done by many people.[20–23]

Other experimental works by Ciofi et al.[24] to redesign copper interconnects by reducing the bottom width of the wire showed some improvements in delay. However, extensive reduction of the base width leads to grain boundary scattering and temperature induced reliability problems. Further, this leads to severe resistance related breakdown problems at sub-7-nm nodes.[20] Also, fabrication of such structures using copper will be a challenging task and it will only increase the process steps in IC manufacturing which may increase the cost also. Other than this, no other works are reported to date that detail the redesigning of VLSI interconnects.

In this paper, we address the two problems of high wire capacitance and low speed conduction at subthreshold voltages. Firstly, we propose triangular CNT bundles (T-CNT) as subthreshold interconnects where the wire capacitance (C_W) of triangular CNT bundles is lesser than the traditionally used square/rectangular CNT bundles.

Secondly, we find out the optimum nFET and pFET transistor widths that is suitable for subthreshold operation, using the current over capacitance (COC) approach. These width optimized transistors are used to drive T-CNT bundles at subthreshold voltages.

In "CNT Bundle Geometry", we describe the T-CNT bundle geometry. The subthreshold current model is discussed in "Subthreshold Transistor Modelling". We compute the equivalent single conductor (ESC) transmission line parameters of conventional CNT bundles with aspect ratios (AR) of 1, 1.5 and 2, and that of T-CNT bundles in "ESC Modelling of Proposed Interconnects". Further, we do HSPICE analysis of the proposed bundles and find their propagation delay and the power dissipated. Electrostatic simulations of the 2D models are also shown to validate our proposed T-CNT bundle model. "Crosstalk and Noise Analysis of Proposed Interconnects" describes the performance analysis of capacitively coupled T-CNT bundle interconnects with conventional ones. We compare the crosstalk induced delay and the power delay product (PDP) for lengths ranging from 500 μm to 2000 μm at 20 nm technology node. We perform the simulations considering various cases of switching activity of the aggressor and victim wires. Lastly, we compare the victim noise levels also thereby ascertaining the robustness of our proposed CNT bundle models at subthreshold conditions. "Conclusions" concludes this paper.

CNT BUNDLE GEOMETRY

All the previous work on modeling of CNT bundle interconnects are assumed to have square or rectangular bundle geometries. This trend can be attributed to the geometry of copper interconnects which is rectangular traditionally. So, the semiconductor industry also followed the same design methodology to date.[25] However, the idea of using alternate geometries is first conceived by Moshin and Srivastava.[26] But it was not pursued later as the performance of existing square/rectangular CNT bundles is comparable or better than copper wires. However, as new trends in VLSI technology are emerging, like subthreshold circuits and low power-high performance circuits, new design trends in CNT bundle geometry is needed to meet the demands of high frequency operation as well as low power consumption.

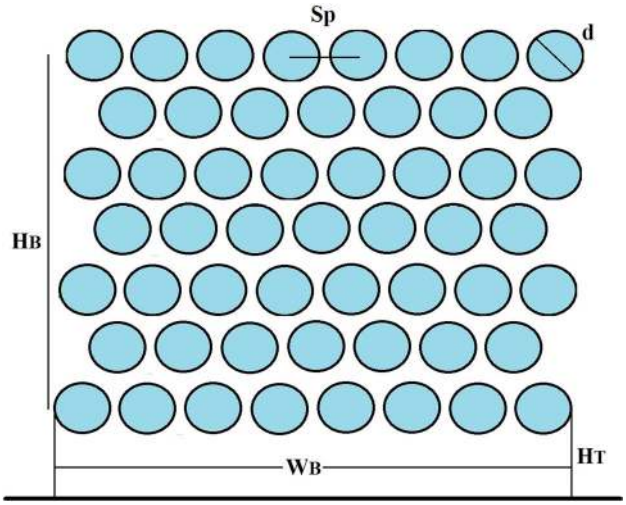

Fig. 1. Schematic of SWCNT bundle of aspect ratio = 1 placed on a substrate.

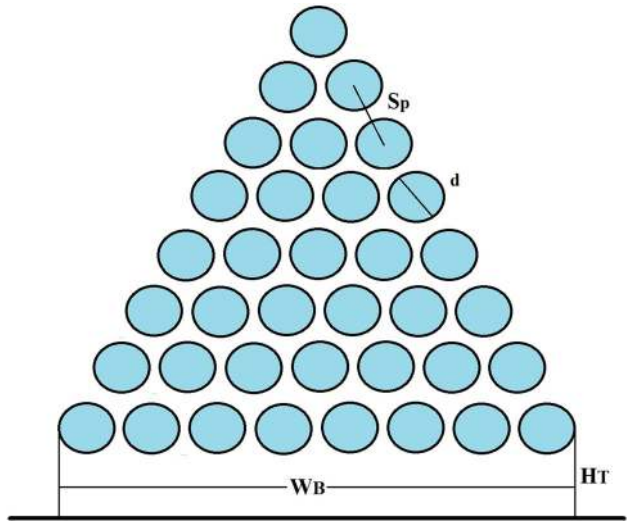

Fig. 2. Schematic of proposed triangular CNT bundle.

Square CNT Bundles

Traditionally used CNT bundle geometry is depicted in Fig. 1. The bundle is placed at a distance of h_t from the ground plane. The number of CNTs along the width (W) is n_W and the number of CNTs along the height (H) of the bundle is n_H. Each CNT is having a diameter d of 1 nm.

Then the total number of CNTs in a square bundle (n_{CNT}) can be found as

$$n_{CNT} = \begin{cases} n_W n_H - (n_H/2), & n_H \text{ is even} \\ n_W n_H - [(n_H - 1)/2], & n_H \text{ is odd} \end{cases} \quad (1)$$

$$n_W = \left\lfloor \frac{W_B - d}{S_p} \right\rfloor \quad n_H = \left\lfloor \frac{H_B - d}{S_p} \right\rfloor \quad (2)$$

where, S_p is the center to center distance of adjacent tubes and is 1.34 nm in our case, considering the van der Waals gap δ of 0.34 nm.[27]

Triangular CNT Bundles

We are motivated by the fact that T-CNT bundles, when placed adjacently over a substrate, are least capacitively coupled because of their geometric advantage. This way, the crosstalk between adjacent interconnects can be reduced. Further, this technology is more suitable for inserting repeaters to enhance signal strength at subthreshold conditions.

As depicted in Fig. 2, the T-CNT bundle has total number of CNTs in the bundle given as,

$$n_{TCNT} = \frac{n_b(n_b + 1)}{2} \quad (3)$$

where, n_b is the number of CNTs at the base of the bundle. Table I summarizes the dimensions and the number of CNTs in the bundles that are considered in this paper taken from ITRS.[25] Throughout this paper, we consider the width, W_B of all the CNT bundles to be same so that the electrostatic capacitance between the bundle and substrate remains same.

It must be noted that, as mentioned in the Introduction, CNTs are placed on substrates by dielectrophoresis and the substrate is shaped into a V shaped trench before CNTs are deposited. This actually causes the T-CNT bundles to be inverted or V shaped. However, for the sake of modelling the electrostatic capacitance effects between the bundle and the ground, we have used the triangular structure as depicted in Fig. 2.

SUBTHRESHOLD TRANSISTOR MODELLING

The factors that influence the current in a FET based inverter are the length and width of the nFET (L_N, W_N) and pFET (L_P, W_P), depletion (C_D) and oxide capacitances (C_{OX}), the subthreshold slope factor n, given by $n = 1 + C_D/C_{OX}$, the thermal voltage $V_{TH} = kT/q$, and the threshold voltage V_T. So, the subthreshold current for a transistor can be modeled as[3]

$$I_{SUB} = I_0 e^{((V_{GS} - V_T)/(nV_{TH}))}(1 - e^{(-V_{DS}/V_{TH})}) \quad (4)$$

where, $I_0 = \mu_0 C_{OX} W_P/L_P (n - 1)V_{TH}^2$ and $I_0 = \mu_0 C_{OX} W_N/L_N (n - 1)V_{TH}^2$ are the input currents in the pFET and nFET, respectively. Other leakage currents in the transistor like p–n junction leakage and gate induced drain leakage are considered to be negligible.[3] So, by fine-tuning the width of the transistors in the inverter, the desired subthreshold current that will be flowing through the interconnect can be achieved. If the width is narrowed, the threshold voltage is also reduced. This is called the inverse narrow width effect (INWE) where a transistor's threshold voltage decreases as the channel width narrows.[28] So, we find this interplay by

Table I. Interconnect geometries at 20 nm technology node[25]

Bundle geometry	Width W_B (nm)	Height H_B (nm)	Aspect ratio (AR)	Number of SWCNTs in bundle
Square	34	34	1	564
Rectangular	34	51	1.5	870
Rectangular	34	68	2	1175
Triangular	34	29.4	0.864	300

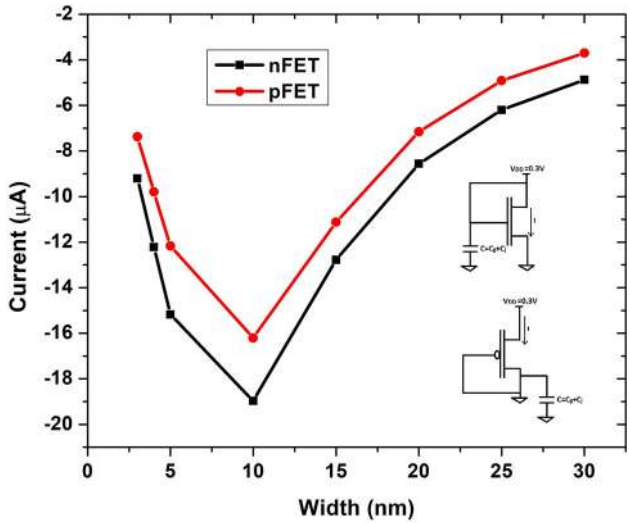

Fig. 3. Output current versus transistor width. Inset: nFET and pFET configuration.

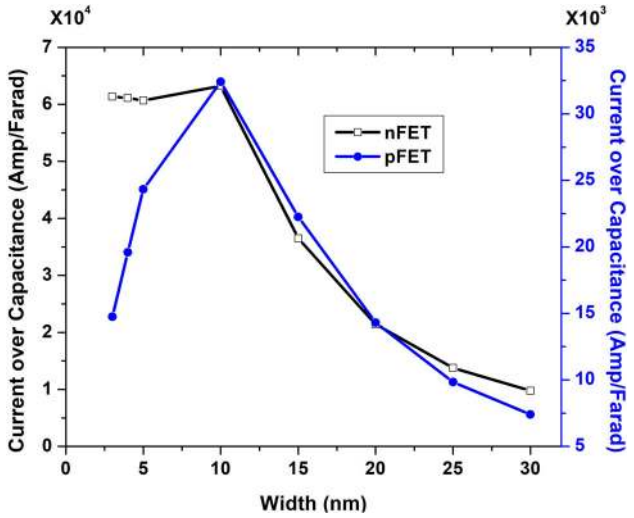

Fig. 4. Current over capacitance ratio versus width for an nFET and a pFET.

reducing the width of both nFET and pFET transistors and by finding the output current.

The current is not lowest when the width is narrowest as seen in Fig. 3. This is because, under subthreshold conditions, the current is exponentially dependent on the threshold voltage and hence may lead to unexpected current values.[28–32] As a rough estimate, we first take 10 nm as the optimum width of the transistors. However, we crosscheck our estimate from Fig. 3 with a more reliable method of finding the subthreshold width of the transistor, as explained below using the current-over-capacitance (COC) approach. The delay of a transistor is dependent on the input voltage V_{DD}, the output current I_0 and is given by

$$t_d = \frac{C_g V_{DD}}{I_0 \cdot e^{(V_{GS}-V_T)/nV_{TH}}} \quad (5)$$

where, C_g is the output capacitance of the transistor.[29] So, for high speed operations, the current must be high and the capacitance must be low. Hence, the current over capacitance ratio (COC) must be maximum, considering absolute values of current. Further, this ratio is maximum when the transistor width is around its minimum value. Hence, we find the optimum width of the driver transistors using the COC ratio.

After incorporating the output and junction capacitances,[29,30] the width of the nFET and the pFET transistors are varied for different COC. Figure 4 shows the plots of COC versus transistor width for a supply voltage of 0.3 V. The transistor output current is in the range of μA while the capacitance is of the order of nF. Thus, in our analysis, the current is the dominating factor in calculating the COC ratio. So, at 20 nm technology node, we find that the optimum width for both nFET and pFET is at 10 nm where the COC is maximum. This is in good agreement with our earlier estimate.

ESC MODELLING OF PROPOSED INTERCONNECTS

Now we perform the analysis of our proposed bundles by formulating equivalent single conductor (ESC) transmission line model. Next, we perform transient analysis of the proposed models and compare the performance of the proposed triangular CNT bundles and conventional square/rectangular bundles. As the CNT growth technology has matured in growing precise crystalline metallic SWCNTs and depositing them at desired locations by dielectrophoresis,[33] we consider that all the bundles consists of 100% metallic CNTs in them. A previous analysis was done on CNT interconnects

considering 80% metallic CNTs in the bundle.[34] We use an equivalent single conductor transmission line model (ESC-TL) in this paper to describe the conducting behaviour of SWCNT bundle interconnects. The transmission line equations of the voltage and current through an SWCNT bundle interconnect as depicted in Fig. 5, can be given as

$$\frac{\partial V(z,t)}{\partial z} + L\frac{\partial I(z,t)}{\partial t} + \mathrm{RI}(z,t) = 0 \tag{6}$$

$$\frac{\partial I(z,t)}{\partial z} + C\frac{\partial V(z,t)}{\partial t} = 0 \tag{7}$$

Considering an individual CNT in a SWCNT bundle, the number of conducting channels that contribute to its electrical conduction is given as

$$N_i = \begin{cases} aTD_i + b, & D_i > d_T/T \\ 2, & D_i < d_T/T \end{cases} \tag{8}$$

where T is temperature in kelvin, D_i is the diameter of the ith shell, $a = 3.87 \times 10^{-4}\ nm^{-1}\ K^{-1}$, $b = 0.2$, and $d_T = 1300$ nm K. The MFP and temperature dependent resistance of a CNT bundle can be given as

$$R_b(T) = \frac{R_{\mathrm{SWCNT}}}{n_{\mathrm{CNT}}} = \frac{R_c + R_Q}{n_{\mathrm{CNT}}} \quad \text{for } l < \lambda_{\mathrm{eff}} \tag{9a}$$

$$R_b(T) = \frac{R_{\mathrm{SWCNT}}}{n_{\mathrm{CNT}}} = \frac{R_c + R_S}{n_{\mathrm{CNT}}} \quad \text{for } l > \lambda_{\mathrm{eff}} \tag{9b}$$

$$R_Q = \frac{h}{4e^2}; \quad R_S = \frac{h}{2N_i e^2}\left[\frac{l}{\lambda_{\mathrm{eff}}(T)}\right] \tag{10}$$

where n_{CNT} is the total number of CNTs in a bundle. The temperature dependent expressions of the ESC inductance of a CNT bundle can be given as

$$L^b_{\mathrm{ESC}}(T) = \frac{L_{\mathrm{m}} + (L_{\mathrm{k}}/N)}{n_B} \tag{11}$$

where L_{m} and L_{k} are the magnetic and kinetic inductances of an isolated CNT. They can be given by the expressions,

$$L_{\mathrm{m}} = \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right); \quad L_{\mathrm{k}} = \frac{h}{2e^2 v_{\mathrm{f}}} \tag{12}$$

Similarly, the effective capacitance of a CNT bundle placed on a ground plane is the series combination of the electrostatic and quantum capacitances of the CNT bundle. The relevant expressions are:

$$C^b_{\mathrm{ESC}}(T) = \left(\frac{C^b_E \cdot C^b_Q}{C^b_E + C^b_Q}\right) \tag{13}$$

$$C^b_E = n_W \times \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{y}{d}\right)}; \quad C^b_Q = n_B \times \frac{2Ne^2}{hv_{\mathrm{f}}} \tag{14}$$

where n_{W} is the number of CNTs along the width of the bundle given in Eq. 2, h is Plank's constant, v_{f} is the Fermi velocity, e is charge of electron, y is the separation between CNT and ground plane and d is the diameter of the CNT. The electrostatic capacitance of the bundle is calculated by considering only the outer CNTs in the bundle as the inner CNTs are not capacitively coupled to the substrate due to the shielding effect of the outer CNTs. The schematic of the ESC model circuit is shown in Fig. 5.

The ESC parameters are computed for T-CNT bundles as well as for AR = 1, 1.5 and 2 bundles at room temperature and listed in Table II. The contact resistance is considered as 10 kΩ for all the cases.[27] The quantum resistance is distributed equally between the end contacts. It can be seen that the wire resistance is least for AR = 2 bundle and largest for triangular CNT bundles. This is because, the total number of CNTs in AR = 2 bundle is more than all other bundles while triangular CNT bundle has least number of CNTs in it. For the same reason, the quantum capacitance is the least for the triangular bundle while it is highest for CNT bundle with AR = 2.

In the case of inductance, triangular CNT bundles possess the highest values while CNT bundles of AR = 2 have least values. As expected, all the quantities increase with increase in length. Owing to the small magnitudes of the subthreshold current, the current dependent magnetic inductance of

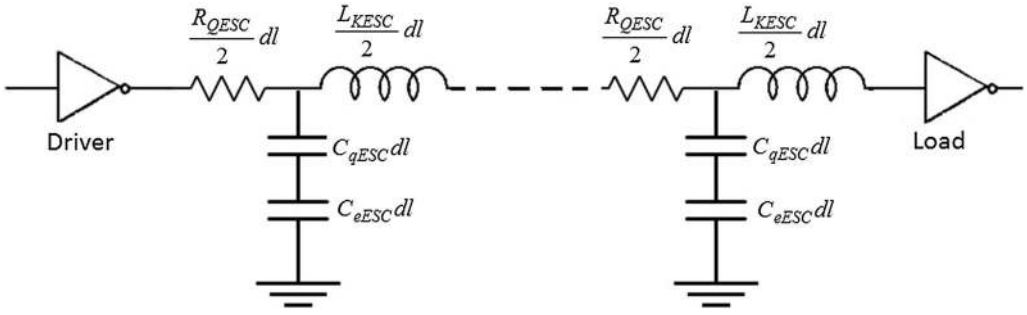

Fig. 5. ESC model of the proposed interconnects.

the bundles would be negligible. Further, it must be noted that the kinetic inductance was neglected citing lower operating frequencies and higher driver resistance.[6–8] However, we envisage that our model of triangular CNT bundles can operate at higher frequencies than expected earlier for subthreshold region.

MODEL VALIDATION AND ANALYSIS OF THE PROPOSED CNT BUNDLES

As a first step, we perform electrostatic field simulations of both Square (AR = 1) and triangular SWCNT bundles when they are excited by a subthreshold voltage of 0.3 V, as shown in Fig. 6. The per unit length conductance of CNTs is $1.55 \times 10^{-4}\ \Omega^{-1}$. The dielectric medium surrounding the wires is considered to have a dielectric constant of 2.4. The electric field surrounding the square bundle in Fig. 6a is more interactive with its neighbor than that of T-CNT bundles. Also, the electric field strength between square CNT bundles is found to be 0.5 times higher than between triangular CNT bundles, which is shown in Fig. 6b. As the aspect ratio of the interconnect structure is increased from 1 to 1.5 and 2, we have found that the coupling gets stronger.

Now, we perform a SPICE based transient analysis of the ESC circuit model shown in Fig. 4 for our proposed T-CNT bundles to compare its propagation delay and power dissipation with conventional bundles of AR = 1, 1.5 and 2. We use the PTM-HP library based 20 nm technology node inverter as driver and load.[35] Propagation delay of a CNT bundle is dependent mainly on the CNT bundle resistance and capacitance. For T-CNT bundles, the resistance is highest as can be seen from Fig. 5a and its intrinsic capacitance is least as per Fig. 5b. This shows that its propagation delay is the least among the CNT bundles considered as shown in Fig. 7. It is 42.31% lesser than for square CNT bundle of AR = 1. Quite obviously, since the T-CNT bundles' capacitance is 48.64% less than its closest competitor of AR = 1, its power dissipation is also less by 34.80% compared to the AR = 1 square bundle. Further, the swing of the output waveforms is better for T-CNT bundles than for other bundles. Hence, we show that T-CNT bundles are better candidates than conventionally used square/rectangular CNT bundles for subthreshold circuit design.

Table II. ESC parameters for CNT bundle interconnects at 20 nm node

Parameter	AR = 1	AR = 1.5	AR = 2	T-CNT
R_b (kΩ/mm)	14.54	7.4	5.49	21.5
L^b_{ESC} (nH/mm)	7.1	4.6	3.4	13.33
C^b_Q (pF/mm)	225.6	348	470	120
C^b_E (fF/mm)	720	720	720	720
C_{C} (nF/mm)	316.32	487.66	659	292.2

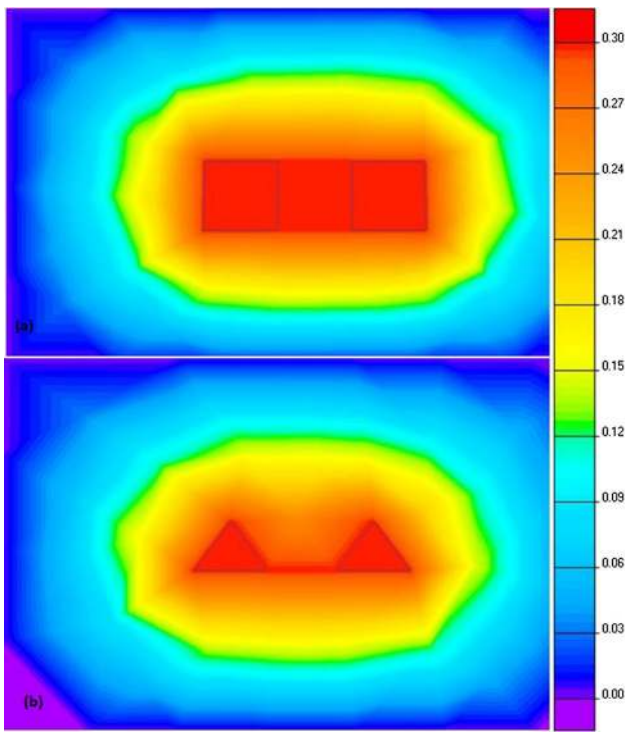

Fig. 6. Electrostatic simulations of (a) square CNT bundles, (b) triangular CNT bundles. Scale = 10 nm.

CROSSTALK AND NOISE ANALYSIS OF PROPOSED INTERCONNECTS

Now, we perform crosstalk analysis of the proposed bundle interconnects for two different cases of switching activity. Case I: aggressor is switching from low to high and victim is tied to low; Case II: aggressor is switching from high to low and victim is tied to low. In both the cases, we analyze the effect

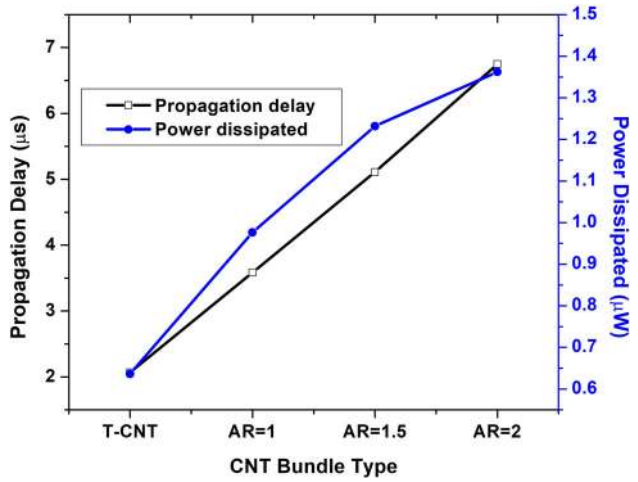

Fig. 7. Propagation delay and power dissipated by various CNT bundles under consideration.

of the coupling capacitance of the interconnects, which determines the crosstalk between the aggressor and the victim. More the capacitance, more the crosstalk and hence more the delay induced. So, for reliable interconnect operation, crosstalk must be minimal and the delay should be least. This is possible by using triangular cross sectioned CNT bundles only. So, for two capacitively coupled T-CNT bundles with n number of CNTs along their side, the coupling capacitance of the nth corresponding CNT pair can be given as

$$C_{\text{C.CNT}} = \frac{2\pi\varepsilon}{\cosh^{-1} y_n/d} \tag{15}$$

where $y_n = y_{n-1} + S_p$ is the inter-CNT distance of the nth pair of coupled CNTs, $n = 1, 2, 3, 4, \ldots$ and $y_0 = 34$ nm. So, the total coupling capacitance CC, of the bundles can be given as

$$C_{\text{C}} = \sum_{m=1}^{n} C_{\text{C.CNT}^m} \tag{16}$$

Comparison of the coupling capacitances computed using (16) for T-CNT bundles with other CNT bundles of AR = 1, 1.5 and 2 is shown in Fig. 8. It can be seen that the C_{C} of T-CNT bundles is 7.3% less than its closest competitor, AR = 1 CNT bundle. Transient SPICE analysis of the proposed coupled interconnects is carried out next for various cases of switching activity.

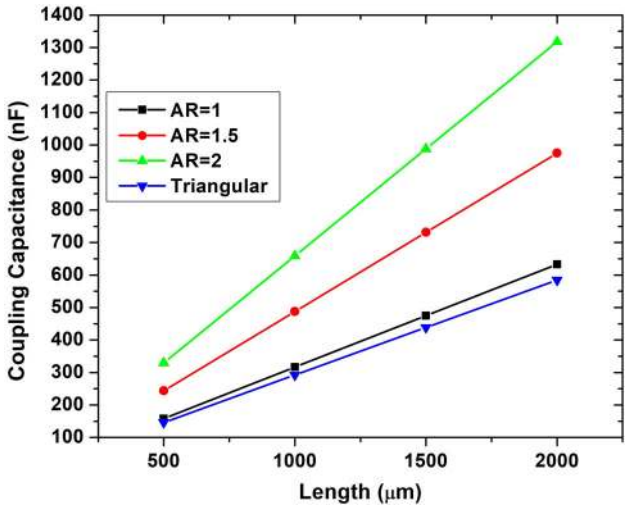

Fig. 8. Coupling capacitance of various CNT bundles versus length.

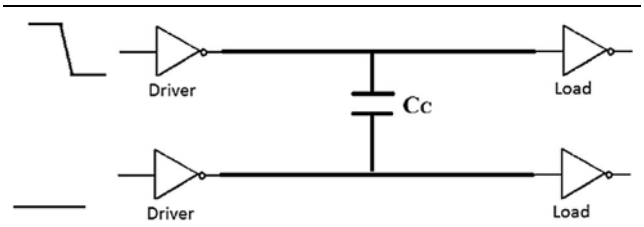

Fig. 9. Capacitively coupled interconnects for Case I.

Case 1: Aggressor Switching from High to Low and Victim Is Tied to Low

The subthreshold output voltage of an inverter is dependent on the width of the nFET transistor when the input waveform transits from low to high. We consider capacitively coupled interconnects as shown in Fig. 9 and apply a pulsed input to the aggressor. The victim line is tied to V_{DD}.

We choose the nFET width as 9 nm and pFET width as 13 nm to get a full swing of the output waveform. We use minimum sized inverters at the load terminals of the wires. Because of the coupling capacitance between the lines, crosstalk occurs and hence delay is induced in the signals. As shown in

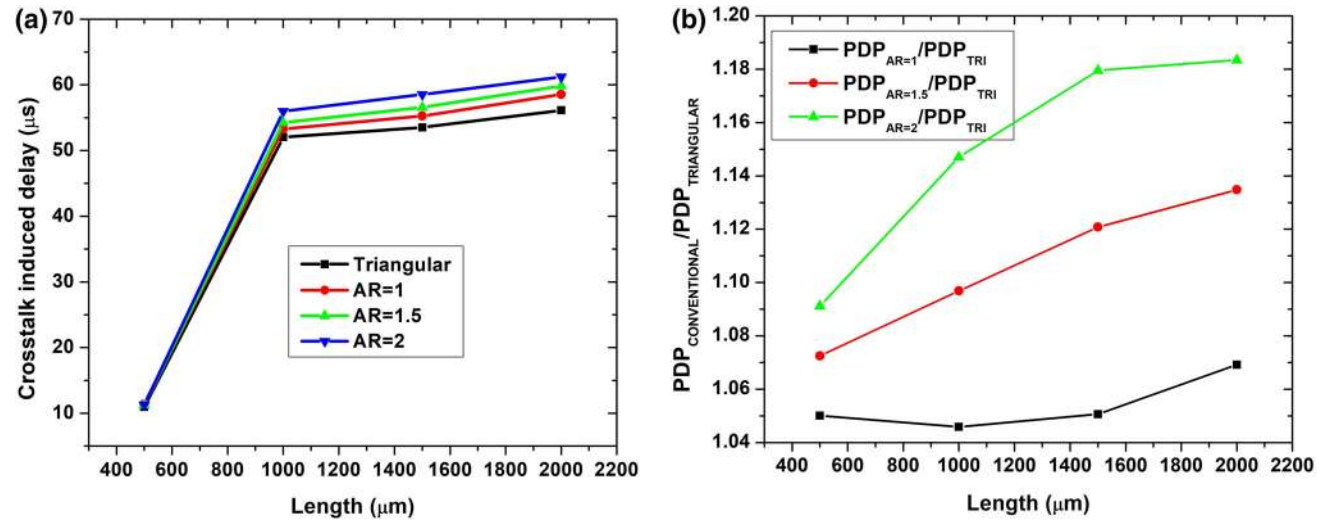

Fig. 10. (a) Crosstalk induced delay and (b) normalized PDP of triangular bundles by conventional bundles for Case I.

Fig. 10a, the delay is least for T-CNT bundles. Further, delay dramatically increases when the length is 1000 μm and above which is evident of the shift from intermediate length to global lengths.

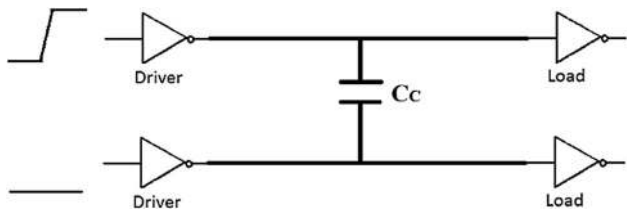

Fig. 11. Capacitively coupled interconnects for Case II.

The power dissipated by T-CNT bundles is found to be lesser by 4.7668% at 500 μm and increases to 6.4704% at 1000 μm when compared to AR = 1 bundles. Also, it was found that the power dissipated is 8.36% and 15.49% lesser compared to AR = 2 bundles, at 500 μm and 1000 μm, respectively. Figure 10b shows the normalized power delay product (PDP) at various wire lengths.

Case 2: Aggressor Switching from Low to High and Victim Is Tied to Low

When the input voltage is switching from high to low, the output of the inverter is dependent on the width of the pFET transistor. Figure 11 shows the schematic of capacitively coupled wires that have minimum sized inverters as load. Here, the pFET

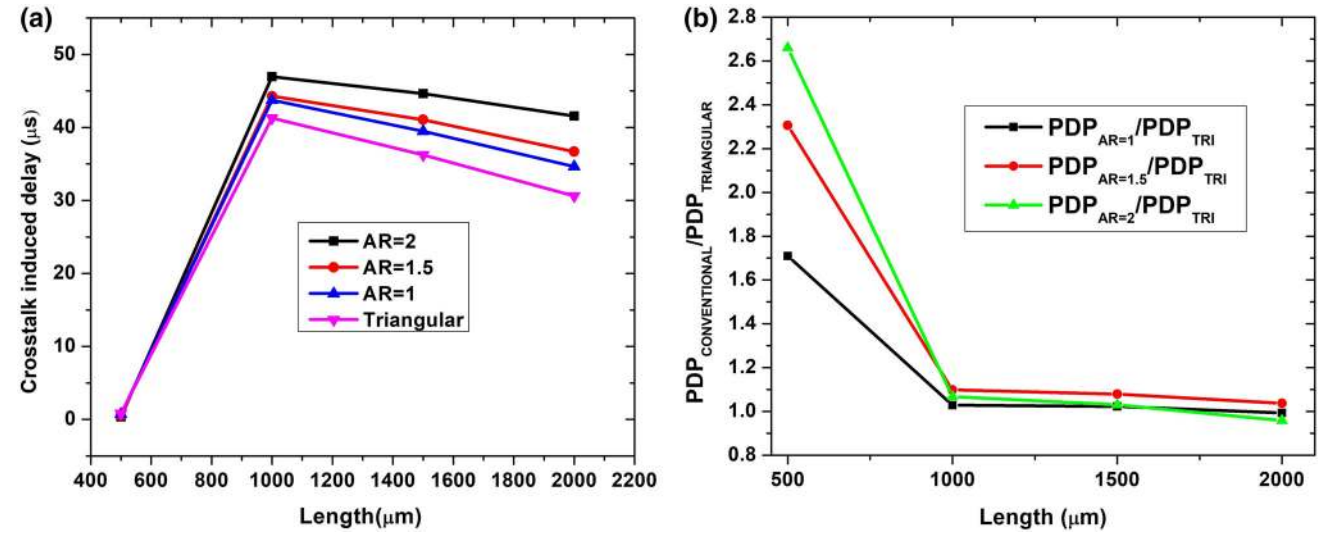

Fig. 12. (a) Crosstalk-induced delay and (b) normalized PDP of triangular bundles by conventional bundles for Case II.

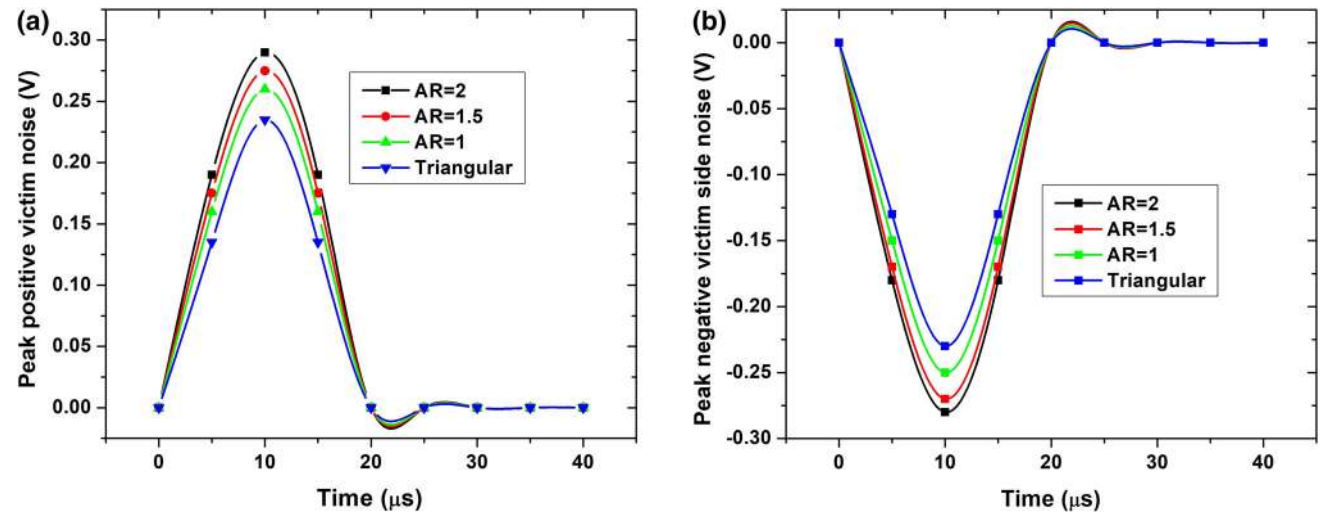

Fig. 13. (a) Peak positive noise and (b) peak negative noise at victim lines due to crosstalk.

width is chosen as 9 nm and nFET width as 13 nm to get full swing waveform at the output.

The crosstalk-induced delay in this case is also lesser for T-CNT bundles than other bundles as in Fig. 12a. It is 36.47% less than AR = 1 bundle at 500 μm and 11.72% less at 2000 μm. Further, the normalized power dissipation with respect to AR = 1, 1.5, 2 bundles is plotted in Fig. 12b.

Crosstalk Noise Analysis

Noise is the ratio of the differential capacitance to the total capacitance and the output crosstalk noise voltage at the victim side is noise times the input voltage. The noise at the victim line due to the switching activity of the aggressor is shown in Fig. 13.

The peak positive noise at the victim side is for Case I and the peak negative noise is for Case II. It can be seen that the crosstalk induced noise is worst for AR = 2 bundles while T-CNT bundles induce least noise on the victim line. Overall, the performance of T-CNT bundles outshines those of AR = 1, 1.5 and 2 bundles as its RC charge up time is less compared to others. Further, at subthreshold voltages, since the current is low, the RC charging time is higher than at nominal voltages. The resistance of T-CNT bundles is sufficiently within the tolerable range of $R_w << R_{driv}$. For global interconnects, there exists a critical length where the $R_w = R_{driv}$, after which the performance of the interconnects degrades. In our case, the proposed T-CNT bundle resistance is far lesser than that of a single CNT, which was the contender as the subthreshold interconnects at global level.

CONCLUSIONS

Subthreshold operation of CNT interconnects is analyzed here. Triangular CNT bundles are found to outperform traditionally used square/rectangular CNT bundle interconnects. The width of the transistors in the driver circuits is also found to influence the subthreshold current and an optimum width is found where the current is at maximum, using the current over capacitance method. Performance factors such as propagation delay, crosstalk-induced delay, power dissipation and power delay product of CNT bundle interconnects of lengths ranging from 500 μm to 2000 μm, are found and compared. It is found that T-CNT bundles have least possible delay, power dissipation and crosstalk induced delay. For the two cases of switching considered: high-to-low and low-to-high, T-CNT bundles showed lesser crosstalk induced peak noise. Thus, T-CNT bundles must be the preferred choice as subthreshold global interconnects.

REFERENCES

1. B. Singh, D. Gola, E. Goel, S. Kumar, K. Singh, and S. Jit, *J. Comput. Electron.* 15, 502 (2016).
2. M.Z. Li, C.I. Ieong, M.K. Law, P.I. Mak, M.I. Vai, S.H. Pun, and R.P. Martins, *IEEE Trans. Very Large Scale Integr. Syst.* 23, 3119 (2015).
3. O. Jamal and A. Naeemi, *IEEE Trans. Nanotechnol.* 10, 99 (2011).
4. Q. Chen, B. Agrawal, and J.D. Meindl, *IEEE Trans. Electron Devices* 49, 1086 (2002).
5. K.J. Lee, H. Park, J. Kong, and A.P. Chandrakasan, *IEEE Trans. Electron Devices* 60, 383 (2013).
6. P.U. Sathyakam and P.S. Mallick, *Int. J. Electron.* 99, 1439 (2012).
7. R. Dhiman and R. Chandel, *J. Comput. Electron.* 13, 360 (2014).
8. M.R. Khezeli, M.H. Moaiyeri, and A. Jalali, *IEEE Trans. Electromagn. Compat.* 61, 100 (2018).
9. M.G. Kumar, R. Chandel, and Y. Agrawal, *IEEE Trans. Electromagn. Compat.* 60, 487 (2018).
10. P.U. Sathyakam, A. Karthikeyan, and P.S. Mallick, *IEEE Trans. Nanotechnol.* 12, 662 (2013).
11. X. Wang and M. Yu, *AEU Int. J. Electron. Commun.* 68, 773 (2014).
12. S.D. Pable and M. Hasan, *Integr. VLSI J.* 45, 186 (2012).
13. S.D. Pable and M. Hasan, *IEEE Trans. Nanotechnol.* 11, 633 (2012).
14. N. Wary and P. Mandal, *AEU Int. J. Electron. Commun.* 68, 969 (2014).
15. M. Mehri and N. Masoumi, *AEU Int. J. Electron. Commun.* 69, 1199 (2015).
16. P.U. Sathyakam and P.S. Mallick, *J. Nano Res.* 52, 21 (2018).
17. P.U. Sathyakam and P.S. Mallick, *J. Nano Res.* 48, 29 (2017).
18. P.U. Sathyakam, A. Bisht, Y. Tandon, and P.S. Mallick, in *Proceedings on 2016 3rd International Conference on Emerging Electronics (ICEE 2016)* (2017). https://doi.org/10.1109/icemelec.2016.8074592.
19. X. Wang, A. Wang, and N.K. Ingle, *V trench dry etch*. US Patent: United States Applied Materials, Inc. (Santa Clara, CA, US), US Grant No. US9355856B2.
20. R. Krupke, F. Hennrich, H.V. Lohneysen, and M.M. Kappes, *Science* 301, 344 (2003).
21. M. Dimaki and P. Boggild, *Nanotechnology* 15, 1095 (2004).
22. P.F. Wu and G.B. Lee, *Adv. Optoelectron.*, Article ID 482741 (2011).
23. G.F. Close and H.S.P. Wong, in *Proceedings of 2007 IEEE International Electron Devices Meeting*. https://doi.org/10.1109/iedm.2007.4418902.
24. I. Ciofi, A. Contino, P.J. Roussel, R. Baert, V.H. Vega-Gonzalez, K. Croes, M. Badaroglu, C.J. Wilson, P. Raghavan, A. Mercha, and D. Verkest, *IEEE Trans. Electron Devices* 63, 2488 (2016).
25. International Technology Roadmap for Semiconductors (ITRS), http://www.itrs.net/reports.html (2013). Accessed on 12 November 2018.
26. K.M. Mohsin and A. Srivastava, in *Proceedings of the 25th edition on Great Lakes Symposium on VLSI - GLSVLSI'15*, 1, C (2015), pp. 265–270.
27. M.K. Majumder, B.K. Kaushik, and S.K. Manhas, *IEEE Trans. Electromagn. Compat.* 56, 1666 (2014).
28. L.A. Akers, *IEEE Electron. Dev. Lett.* 7, 419 (1986).
29. B.H. Calhoun, A. Wang, and A. Chandrakasan, *IEEE J. Solid-State Circuits* 40, 1778 (2005).
30. M. Muker and M. Shams, *Electron. Lett.* 47, 372 (2011).
31. M. Nabavi and M. Shams, *IEICE Electron. Express* 9, 1550 (2012).
32. M.O. Nabavi, *Designing faster CMOS subthreshold circuits using transistor sizing and parallel transistor stacks* (Ph.D. Dissertation, Carleton University, Ottawa 2012). https://curve.carleton.ca/…/nabavi-designingfastercmossubthresholdcircuitsusing.pdf. Accessed 25 March 2019.
33. G.F. Close, S. Yasuda, B. Paul, S. Fujita, and H.S.P. Wong, *Nano Lett.* 8, 706 (2008).

34. A. Alizadeh and R. Sarvari, *IEEE Trans. Very Large Scale Integr. Syst.* 24, 803 (2016).
35. Predictive Technology Models, http://ptm.asu.edu/. Accessed 10 November 2018.