Research Article

S. Madichetty*, A. Dasgupta and S. Jinka

A New Harmonic Mitigation Scheme for MMC – An Experimental Approach

Abstract: A multilevel converter has been brought into limelight in this article, however, particular attention has been provided to the form and function of modular multilevel converter (MMC) with new design, control and harmonic mitigation schemes. A new controller scheme has been proposed to mitigate the lower and higher order harmonics. The proposed scheme shows its effectiveness by theoretical calculations, verified by simulation and experimental results. Till date, research in this field is very limited with circulating currents and harmonics as the major problem. This article effectively addresses the problem with prototype 1 kVA implementation and attempts to make a detailed analysis with their functions in comprehensive manner with high-voltage DC application under different conditions. Also, the applicability of zero voltage switching at turn ON and zero current transition at turn OFF has been verified experimentally. The strategic conclusions on MMC have been made in order to make the system more robust in operation, less complexity in design and control.

Keywords: modular multilevel converter, review on MMC, MMC topologies, MMC modeling

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1 Introduction

Many investigations in the field of modular multilevel converters have led to successful operation in high-voltage DC (HVDC) systems. In recent times, in the power transmission era, very long distances HVDC transmission lines based current-source converters and voltage-source converters (VSI) offered more economic and cost-effective power transmission. But, recently HVDC transmission systems based on VSI have received increasing attention owing to many opportunities like the grid access of weak AC networks, independent control of active and reactive power, supply of passive networks and black start capability, high dynamic performance and small space requirements. In particular, the novel power converter topology for modular multilevel converter (MMC) has been intensively researched and developed, evaluated by many features like high modularity, simple scalability, low expense of filters, robust control, simple in design and redundancy. This converter is composed of identical power cells connected in series, each one build up with standard components, enabling the connection to high-voltage poles. Although the MMC and derived topologies offer several advantages, they also introduce a more complex design of the power circuit and control goals, which have been the main reasons for the recent and ongoing research. Furthermore, medium-voltage converters are an interesting area for the application of MMCs.

The important features of the multilevel converters are as follows:

- Voltage sharing of the devices is handled automatically by the topology.
- The waveform shape will lead to sinusoidal waveform due to which the THD is reduced and the harmonics as well.
- The operating voltage of the converters can be increased, instead of connecting the devices in series or in parallel, which makes the system more complex.

A new transformer less four-leg topology is suggested for shunt compensation [1]. In "Accelerated Model of Modular Multilevel Converters in PSCAD/EMTDC" [2] and in "High-Power Modular Multilevel Converters With SiC JFETs" [3], the possibility of building a MMC using silicon carbide (SiC) switches has been studied. In the IEEE paper "Active Redundant Sub-module Configuration in Modular Multilevel Converters" [4], the MMC is based on the cascaded connection of identical sub-modules (SMs) enabling additional redundancies. In the papers

"Active Redundant Sub-module Configuration in Modular Multilevel Converters" and "The Multilevel Modular DC Converter" [5], the configuration of the MMC topology with redundant SMs is proposed, and the effects of active redundancies are demonstrated. In the IEEE Transaction paper on Industrial Electronics "Hybrid Electric Vehicle Power Management Solutions Based on Isolated and Non-isolated Configurations of Multilevel Modular Capacitor-Clamped Converter" [6], it is mentioned that the MMC has become an increasingly important topology in medium- and high-voltage applications. In Ref. [7], the various configurations of a multilevel modular capacitor-clamped converter (MMCCC) are presented, and it also reveals many useful and new formations of the original MMCCC for transferring power in either an isolated or non-isolated manner. In Ref. [8], it proposes a novel topology of a multilevel modular capacitor-clamped dc–dc converter. Barrena et al. [9] provide the idea of voltage balancing of the capacitors of different SMs comprising the converter. In Ref. [10], it proposes a modulation strategy for the MMC which provides the voltage balancing of the capacitors of different SMs comprising the converter. In Ref. [11] it states that HVDC transmission systems are becoming increasingly popular when compared to conventional AC transmission. HVDC VSCs can offer advantages over traditional HVDC current-source converter topologies, and as such, it is expected that HVDC VSCs will be further exploited with the growth of HVDC transmission. In Ref. [12], the modular multilevel cascade converter (MMCC) family based on cascade connection of multiple bidirectional chopper cells or single-phase full-bridge cells are discussed. In Ref. [13], a discussion on new ac/ac modular multilevel topology for connecting two three-phase systems is provided. The operating principle is explained, and characteristic waveforms are given. In Ref. [14], it is clearly mentioned that an onshore horizontal axis wind turbine, generator and converter are usually in the nacelle on the top of the tower, while the grid step-up transformer is placed at the bottom. Also, a new ac/ac modular multilevel converter [15] (M^2LC) family is expected to be introduced. The new concept stands out due to its modularity and superior control characteristics. Multilevel voltage-source converter topologies are widely used today in high-power applications such as medium-voltage drives [16]. On the other hand, studies on matrix converters have been mainly limited to the low power range. A modular multilevel cascade converter based on double-star bridge cells is expected to be one of the next-generation medium-voltage PWM converters intended for grid connections [17, 18].

This paper is organized in six sections. Section 1 introduces the MMC and its literature survey. The proposed circuit and its operation are discussed in Section 2, followed by Section 3 that discusses the controller design and its stability analysis. Section 4 discusses the switching schemes and its implementation. In Section 5, the application of proposed technique to HVDC is discussed, and Section 6 provides conclusion with recommendations.

2 Proposed circuit and its operation

The basic circuit topology is shown in Figure 1(a). It is a three-phase five-level MMC having four SMs in upper limb and four SMs in lower limb. Each SM basic circuit is shown in Figure 1(b). This circuit mainly consists of an inductor having self-inductance L_1 and L_2. Each module consists of main switch S_1 and auxiliary switch S_2 also termed as I_1 and I_9 with their anti-parallel diodes D_1 and D_2, respectively. Main switch and auxiliary switch consist of a capacitor connected in parallel as C_{s1} also termed as C_1.

It has been considered the five-level MMC for validation. The switching operations have been shown in Table 1. The top four switches in "R" phase limb are considered as I_1, I_2, I_3 and I_4, and the bottom four switches are considered as I_5, I_6, I_7 and I_8 of a single leg, whereas the auxiliary switches are in anti-operation of main switches provided with delay, which will be explained in subsequent sections. In Table 1, it shows the switching states of a MMC. Here, it has been considered that "1" indicates the switch is in ON condition and "0" indicates the switch is in OFF condition. It mainly consists of: "1" state of "$v/2$" output voltage, "16" states of "$v/4$" output voltage and "16" states of "0" voltage conditions. Table 2 shows the basic operation of some redundancy switching state conditions of upper limb of a phase. Table 3 shows the capacitor charging status of an upper limb of a phase. The basic circuit topology is represented in Figure 1(a) and 1(b). The modified module has been presented in Figure 4. It is one of three-phase five-level MMCs having four SMs in upper limb and four sub-modules in lower limb. This circuit mainly consists of a transformer having self-inductance L_1 and L_2 with an assumption of the coefficient of coupling $M = 1$. It has main switch S_1 and auxiliary switch S_2 with their anti-parallel diodes D_1 and D_2, respectively. Main switch and

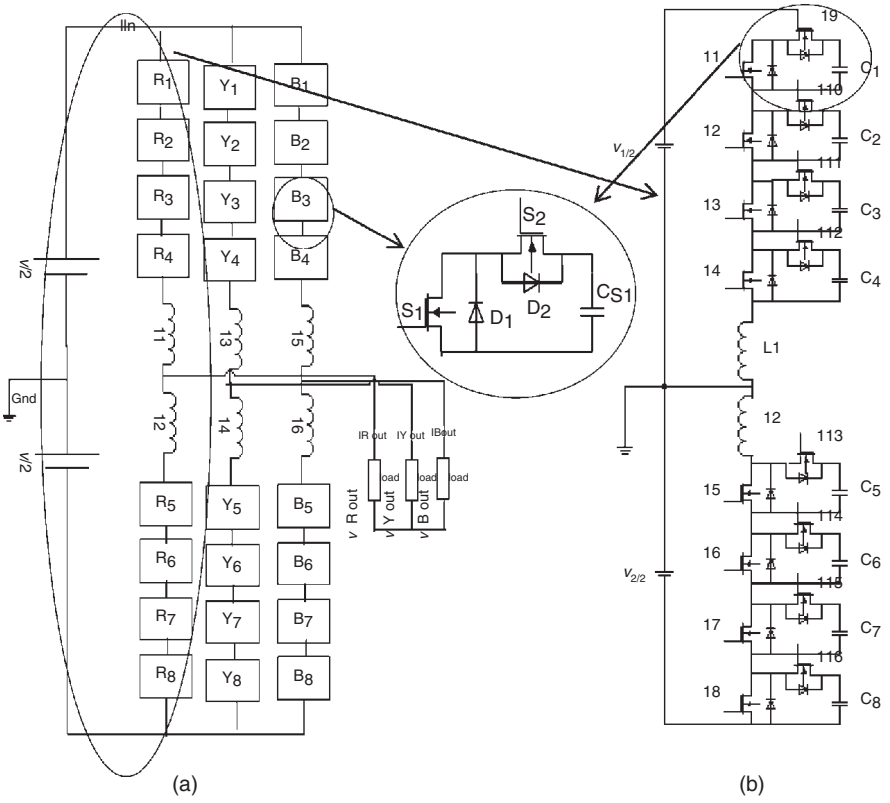

Figure 1 (a) Three-phase five-level MMC. (b) Expanded MMC for a "R" phase limb

Table 1 Basic switching operation of a five-level MMC

State	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	State
$+V/2$	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	$-V/2$
$+V/4$	1	1	1	0	1	0	0	0	0	0	0	1	0	1	1	1	$-V/4$
	1	1	1	0	0	1	0	0	0	0	0	1	1	1	0	1	
	1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	0	
	0	1	1	1	1	0	0	0	1	0	0	0	0	1	1	1	
0	1	1	0	0	1	1	0	0	1	0	1	0	1	1	0	0	0
	1	1	0	0	0	1	1	0	1	0	1	0	0	1	1	0	
	1	1	0	0	0	0	1	1	1	0	1	0	0	0	1	1	
	1	1	0	0	1	0	0	1	1	0	1	0	1	0	0	1	

Table 2 Basic switching operation of a redundancy switching state in MMC

State	Current	Switching	Capacitor	Capacitor
1010	$i_a > 0$	S_1 D_2 S_4 D_3	$C_{s2} \uparrow$	$C_{s4} \downarrow$
1010	$i_a < 0$	S_2 D_1 S_3 D_4	$C_{s4} \uparrow$	$C_{s2} \downarrow$
0110	$i_a > 0$	S_2 D_1 S_4 D_3	$C_{s1} \uparrow$	$C_{s4} \downarrow$
0110	$i_a < 0$	S_2 D_1 S_4 D_3	$C_{s4} \uparrow$	$C_{s1} \downarrow$
0101	$i_a > 0$	S_2 D_1 S_3 D_4	$C_{s1} \uparrow$	$C_{s3} \downarrow$
0101	$i_a < 0$	S_1 D_2 S_4 D_3	$C_{s3} \uparrow$	$C_{s1} \downarrow$
1001	$i_a > 0$	S_1 D_2 S_3 D_4	$C_{s1} \uparrow$	$C_{s3} \downarrow$
1001	$i_a < 0$	S_2 D_1 S_4 D_3	$C_{s3} \uparrow$	$C_{s2} \downarrow$

auxiliary switch consist of capacitors connected in parallel as C_{s1} and C_{s2} with an additional capacitor C_{aux} to provide soft switching operations, whereas the auxiliary switches are in anti-operation of main switches provided with delay, which will be explained in subsequent sections.

Due to the uneven voltage distribution in the legs of a phase, circulating currents will flow through the system. It consists of current harmonics that deteriorate the system performance. Here, an attempt is made to derive the current harmonics present in circulating currents and it is necessary to make controller to suppress the same. The instantaneous voltages across the capacitors are denoted as $V_{c1}, V_{c2}, V_{c3}, V_{c4} \ldots V_{cN}$, and also the voltage distribution across the capacitors is considered as unequal. The

Table 3 Basic capacitor switching operation of a redundancy switching state in MMC

S_1	S_2	V_{out}	Current	Power	Capacitor
ON	OFF	0	$i_{out} > 0$	S_1	Undefined
ON	OFF	0	$i_{out} < 0$	D_1	Undefined
OFF	ON	V_{dc}	$i_{out} > 0$	D_2	Charge
OFF	ON	V_{dc}	$i_{out} < 0$	S_2	Discharge

current flowing through the R phase top limb, bottom limb, circulating current and R phase currents are represented by "i_{tr}", "i_{lr}", "i_{cir}" and "i_r", respectively. In order to find out voltage for the "R" phase, KVL is applied to Figure 1. Then the voltage across the R phase top limb, "V_{tr}", and resistance, R_{top}, for bottom limb, "V_{lr}" and resistance, R_{low}, circulating currents, "i_{cir}", with supply voltage, "V_{dc}", "V_{ntr}" represents the voltage of limb "n", and "N" represents the number of modules.

$$V_{c1} = V_{c2} = V_{c3} = V_{c4} \ldots V_{cN}. \tag{1}$$

Under any switching conditions, the average voltage across the upper arm switches is shown in eq. (2).

$$\frac{V_{cu}}{N} = \frac{V_{dc} + \Delta V_{cu}}{N} \tag{2}$$

The total capacitor voltage of the capacitor is shown in eq. (3) and the differential capacitor voltage is shown in eq. (4).

$$V_{cu} = V_{c1} + V_{c2} + V_{c3} \ldots V_{cN}. \tag{3}$$

$$\Delta V_{cu} = \Delta V_{c1} + \Delta V_{c2} + \Delta V_{c3} \ldots \Delta V_{cN}. \tag{4}$$

$$\frac{V_{cl}}{N} = \frac{V_{dc} + \Delta V_{cl}}{N} \tag{5}$$

$$V_{cl} = V_{c(N+1)} + V_{c(N+2)} + \ldots V_{c2N} \tag{6}$$

$$\Delta V_{cl} = \Delta V_{c(N+1)} + \Delta V_{c(N+2)} + \ldots V_{c2N} \tag{7}$$

The circulating currents in the arm inductors consist of both DC and AC components. These AC components are called as the harmonics, since those are rotating with the higher frequencies in the system.

$$i_{cir} = \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} (i_{acn}) \tag{8}$$

$$i_{cir} = \frac{i_{dc}}{3} + i_{ac1} + i_{ac2} + i_{ac3} + \ldots i_{acn} \tag{9}$$

In order to derive the circulating voltage and current, we need the output voltage of a single-phase from the three-phase:

$$V_R = \frac{V_{dc} \cdot m \cdot \sin(\omega_o t)}{2} \tag{10}$$

$$I_R = I_o \cdot \sin(\omega_o t - \varphi) \tag{11}$$

"m" is the modulation index of a signal. Yet again, the actual voltages are shown as follows:

$$V_{acu} = N \cdot \frac{V_{dc}}{2} (1 - m \cdot \sin(\omega_o t))(V_{ac} + \Delta V_{cu}) \tag{12}$$

$$V_{acl} = N \cdot \frac{V_{dc}}{2} (1 + m \cdot \sin(\omega_o t))(V_{ac} + \Delta V_{cl}) \tag{13}$$

Therefore, the total voltage is

$$V_{ac} = V_{au} + V_{al} \tag{14}$$

$$= \frac{V_{dc}}{2} (1 - m \cdot \sin(\omega_o t))(\Delta V_{cu} + V_{ac}) + \frac{V_{dc}}{2} \; 1 + (m \cdot \sin(\omega_o t)(V_{ac} + \Delta V_{cl})) \tag{15}$$

$$V_{au} + V_{al} = V_{dc} + \frac{\Delta V_{cu} + \Delta V_{cl}}{2} + \frac{m \cdot \sin \omega_o t \cdot (\Delta V_{au} - \Delta V_{cl})}{2} \tag{16}$$

In order to derive the disturbance voltage for the upper and lower cell capacitors of a leg i.e. ΔV_{cu} and ΔV_{cl}:

$$V_{cl} = \frac{1}{C_l} \int i_l(t) \cdot dt \tag{17}$$

$$V_{cu} = \frac{1}{C_u} \int i_u(t) \cdot N_u \cdot dt \tag{18}$$

At this instance,

$$i_u = \sum_{n=0}^{\infty} i_{un} \tag{19}$$

$$i_l = \sum_{n=0}^{\infty} i_{ln} \tag{20}$$

$$N_u = \frac{1 - m \cdot \cos \omega t}{2} \tag{21}$$

$$N_l = \frac{1 + m \cdot \cos \omega t}{2} \tag{22}$$

$$V_{cu} = \frac{1}{C_u} \int \sum_{n=0}^{\infty} i_{un} \cdot \frac{1 - m \cdot \cos \omega t}{2} \tag{23}$$

$$V_{cl} = \frac{1}{C_l}\int \sum_{n=0}^{\infty} i_{ln} \cdot \frac{1 - m \cdot \cos \omega t}{2} \tag{24}$$

$$C_u = C_1 + C_2 \ldots C_n \tag{25}$$

$$C_l = C_{n+1} + C_{n+2} \ldots C_{2n} \tag{26}$$

Now, let us consider about the current

$$i_{au} = i_{dc} + i_{al} + \sum_{n=2}^{\infty} i_{ac}n \tag{27}$$

$i_{au} \rightarrow$ The current present in the phase "a" upper arm, $i_{dc} \rightarrow$ DC component of the current, $i_{ac} \rightarrow$ Fundamental component of the current, $i_{ac} \cdot n \rightarrow$ Harmonic component of current.

$$i_{al} = i_{dc} - i_{al} + \sum_{n=2}^{\infty} i_{ac} \cdot n \tag{28}$$

$$i_{ac} = i_{ac} m \cdot \cos(n\omega t + \varphi_n) \tag{29}$$

$\therefore$ The total current

$$i_a = i_{au} + i_{al} \tag{30}$$

$$i_a = \left(i_{dc} + i_{al} + \sum_{n=2}^{\infty} i_{ac} \cdot n\right) + \left(i_{dc} - i_{al} + \sum_{n=2}^{\infty} i_{ac} \cdot n\right) \tag{31}$$

By considering voltage for "*N*th" module in terms of capacitance

$$i_a = I_o \cdot \sin(\omega t - \varphi) \tag{32}$$

$$= \left(i_{dc} + i_{al} + \sum_{n=2}^{\infty} i_{ac} \cdot n\right) + \left(i_{dc} - i_{al} + \sum_{n=2}^{\infty} i_{ac} \cdot n\right) \tag{33}$$

$$\Delta V_{cu} = \frac{1}{2C} \cdot N \cdot \int (1 - m \cdot \sin(\omega_o t)) \cdot \left(\frac{i_a}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}\right) \cdot dt \tag{34}$$

$$\Delta V_{cl} = \frac{1}{2C} \cdot N \cdot \int (1 + m \cdot \sin(\omega_o t)) . \left(-\frac{i_a}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}\right) \cdot dt \tag{35}$$

$\therefore$ The total "R" phase voltage is shown in eq. (36)

$$V_a = V_{au} + V_{al} \tag{36}$$

$$V_a = V_{dc} + V_{au} + V_{al} \tag{37}$$

By substituting eqs (34) and (35) in eq. (37), we have

$$= V_{dc} + \left(\frac{\Delta V_{cu} + \Delta V_{cl}}{2}\right) + \left(\frac{m \sin(\omega_o t) \cdot \Delta V_{cu} - m \sin(\omega_o t) \cdot \Delta V_{cl}}{2}\right) \tag{38}$$

$$= V_{dc} + \frac{1}{2C} \cdot N \cdot \int (1 - m \cdot \sin(\omega_o t)) \cdot \left(\frac{i_{au}}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}\right) \cdot dt + \frac{1}{2C} \cdot N \cdot \int (1 + m \cdot \sin(\omega_o t)) \cdot \left(-\frac{i_{al}}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}\right) \cdot dt \tag{39}$$

$$= \frac{m \sin(\omega_o t) \cdot \frac{1}{2C} \cdot N \cdot \int (1 - m \cdot \sin(\omega_o t)) \cdot \left(\frac{i_{au}}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}\right) \cdot dt}{2} - \frac{m \sin(\omega_o t) \cdot \frac{1}{2C} \cdot N \cdot \int (1 + m \cdot \sin(\omega_o t)) \cdot \left(-\frac{i_{al}}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}\right) \cdot dt}{2} \tag{40}$$

From above, it can be concluded that, the system consists of both dc and ac components. The most important issue here is the steady state of a system with controller, if applied. To maintain its fundamental Harmonic component and eliminate the dc and ac components, a controller is needed to be implemented in the system. The controller should be designed so as to fully suffice eqs (41) and (42).

$$\Rightarrow \left[\int (1 - m \sin \omega_o t) \frac{i_{dc}}{3} + (1 - m \sin \omega_o t) \sum_{n=1}^{\infty} i_{acn}\right] = 0 \tag{41}$$

$$\Rightarrow \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn} = 0 \tag{42}$$

From eqs (41) and (42), it is found that, load voltage depends upon the current i_V, difference between upper and lower capacitors; i_{cir} depends only on the DC link voltage, the sum of the arm voltages.

3 Optimal controller used to compensate the circulating currents

Taking into account eqs (39)–(41), the controller should eliminate both the lower order even harmonics and higher order harmonics. Even though the higher order harmonics are less in number, as the order of converter increases, the effect on system can be noticed. To proficiently eliminate the harmonics from the system, a repetitive controller is then added to the system. The optimum values of proportional and integral controller are obtained with the use of the minority charge carrier inspired algorithm [19, 20] as shown in Figure 2.

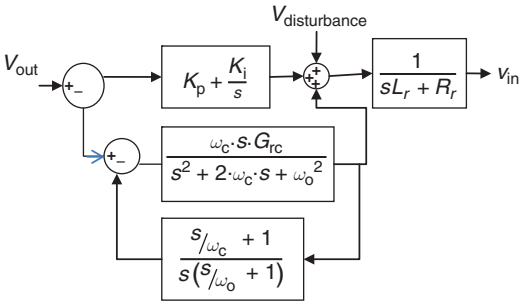

Figure 2 Repetitive controller used for MMC

Balancing a system needed to have the net energy transfer to be zero. Hence,

$\omega_c \rightarrow$ Bandwidth of the controller,

$G_{rc} \rightarrow$ Gain of the resonant controller,

$\omega_o \rightarrow$ Resonant frequency of the controller

As per Figure 3(a), the controller suppresses the even harmonics completely. The controller is designed with keeping the stability view in mind. Controller and its various responses as shown in Figure 3(a)–3(d). It shows that the controller will retain stability under any disturbances. All the harmonics can be controlled by the optimal switching pattern of MMC as per Table 1. All the voltages can be sensed by the sensors, and respective switches can be triggered, in order to maintain the voltage in balance condition.

4 ZVCTS based switching scheme in MMC using proposed scheme

A new switching loss-mitigated sub-module scheme proposed for modular multilevel converter is shown in Figure 4.

The active snubber circuit, proposed, is discussed in the aspects of design and validation for a five-level modular multilevel converter. Furthermore, it provides a zero voltage transition (ZVT) at turn ON and zero current

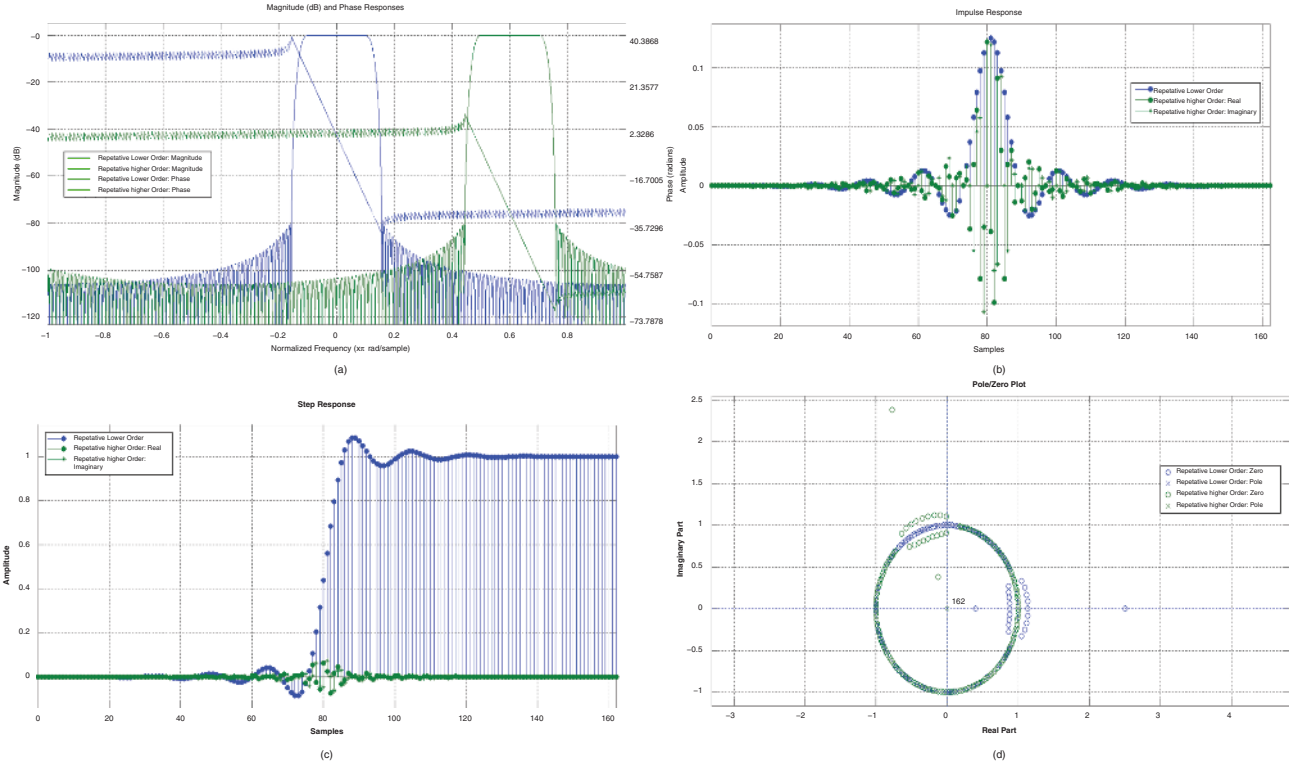

Figure 3 (a) Repetitive controller used for MMC showing magnitude and phase responses (*X*-axis – normalized frequency in rad/sample and *Y*-axis – magnitude in db). (b) Repetitive controller used for MMC showing impulse responses (*X*-axis – samples and *Y*-axis – amplitude). (c) Repetitive controller used for MMC showing step responses (*X*-axis – samples and *Y*-axis – amplitude). (d) Repetitive controller used for MMC showing pole/zero responses (*X*-axis – real part and *Y*-axis – imaginary part)

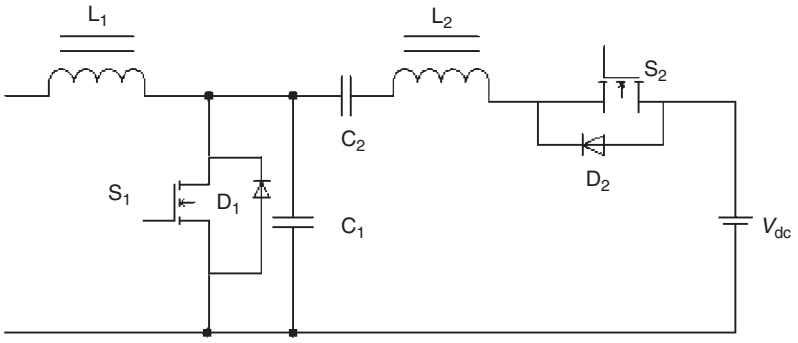

Figure 4 Modified sub-module used in MMC under Zero Voltage current transition switching (ZVCTS) conditions

transition (ZCT) at turn OFF for switch "S_1". Again zero current switching at turn ON for an auxiliary switch "S_2" and ZCT at turn OFF will be achieved.

4.1 Assumptions

If I_{S2}(current passing through the switch S_2) increases, resonance will occur in between $L_1 - C_1 - L_2$. If S_2 conducts, then resonance will occur in between $L_2 - C_2 - L_1$ and will achieve Zero Current Switching (ZCS).

(i) A resonance will occur in between C_1–L_1–L_2–C_2, then the condition of Zero Voltage Switching (ZVS) will be achieved.

(ii) If S_2 is in conducting state, it leads to a conduction of a resonant current between L_1–L_2–C_1, where Zero Voltage Transition (ZVT) kept turned on for S_1.

4.2 ZVT turn ON and ZCT turn OFF for S_1

1. First, turn ON the switch "S_2", then the capacitor C_1 discharges its energy due to which the capacitor "C_2" and "L_2" will get charged. Due to coupling effect, the primary winding will also get transferred, and instantly energy will concentrate on L_1–C_1–L_2 which leads to response. This is the ideal time to switch on "S_1". This signal can be applied as long as the C_1 completely discharges; thus emerges the ZVT.
2. While the switch "S_1" conducts the current, the signal is applied to the switch "S_2" for creating a resonance current higher than that of an input current. At this time, the current is always zero. Therefore, "S_1" can be cancelled, and ZCT can be possible for the same time, as shown in Figure 5.

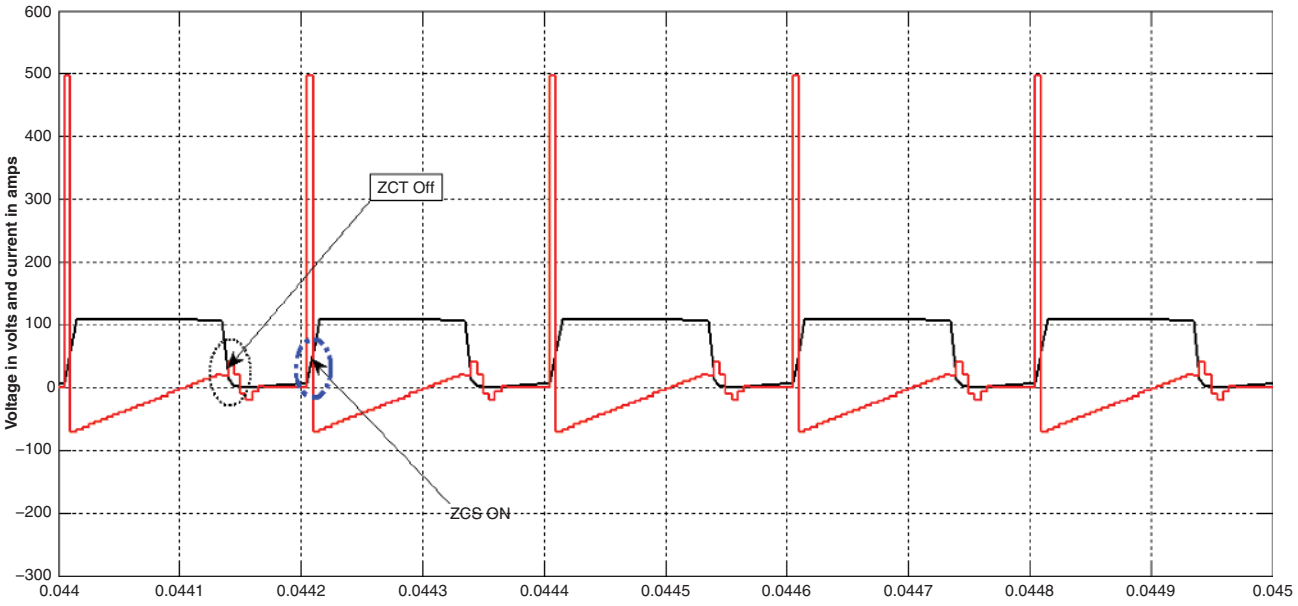

Figure 5 ZVT turn ON and ZCT turn OFF condition for switch S_1

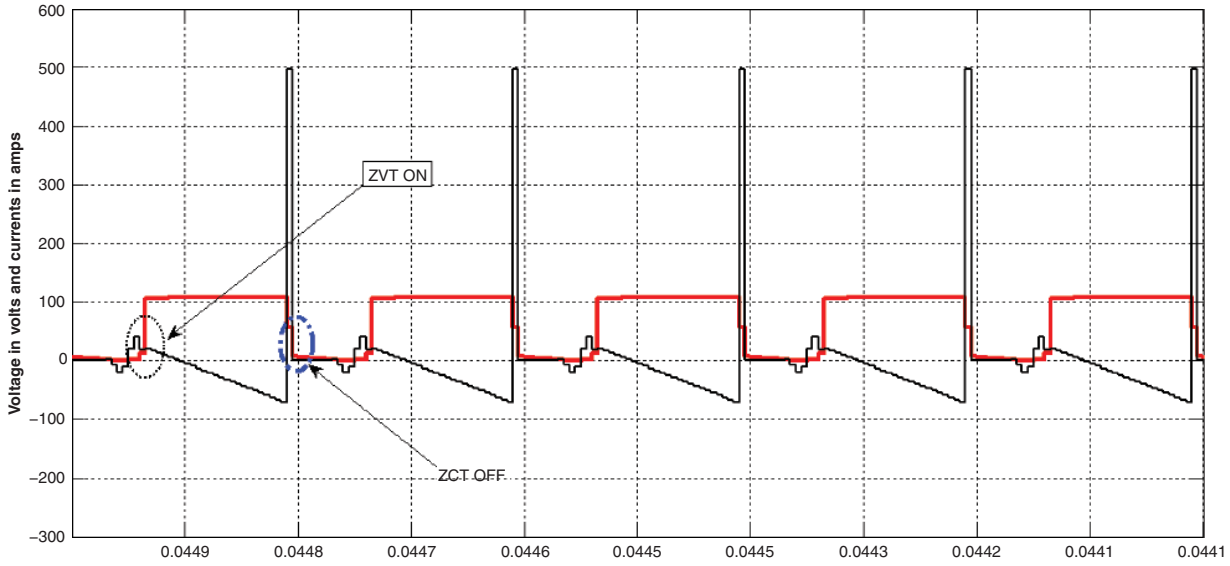

Figure 6 ZCS turn ON and ZCT turn OFF condition for S_2

4.3 ZCS turn ON and ZCT turn OFF for S_2

1. When the switch "S_1" gets suddenly switched OFF, the resonance conduction will take place, resulting in the application of ZCS.
2. While turning OFF, "S_2" current should reach to zero with a resonance. So, ZCT can be provided here and is shown in Figure 6.

The values of capacitor and inductor have been selected as per Table 4.

Table 4 Design of inductor and capacitor under ZVCTS condition

Design of capacitor	Design of inductor
C_{S1} and C_{S2} should be selected based on the values of L_{S1} and L_{S2} taking into account the resonance condition.	The value of L_{S2} can be selected in such a way that $\frac{V_{out}}{L_{S2}} \cdot t_{r_{S2}} \leq I_{maxin}$ The value of L_{S1} can be selected in such a way that $L_{S1} = 2 * L_{S2}$

5 Application of proposed scheme

The proposed scheme is developed and applied to HVDC transmission system with consideration of fault conditions. For this case, a HVDC line having parameters as 100 km length, HVDC line with the power capacity of 2,000 MVA, 530 kV, 50 Hz is considered as shown in Figure 7(a). The system is investigated for different conditions as explained below: The HVDC system is connected to grid with experimental verification of MMC. A virtual fault condition is created at three different conditions as LLL, LLG and LG faults and investigation results are as follows.

The AC voltage step 10% is applied at $t = 0.2$ s during 0.14 s. The above results clarify that the active and reactive power deviation from the pre-disturbance is less than 0.09 pu and 0.2 pu, respectively. The recovery time is less than 0.3 s, and the steady state is reached before next perturbation initiation. The LLL fault is applied at $t = 1.5$ s during 0.9 s. Consequently, results in the active and reactive power deviation from the reference. During the three-phase fault, the transmitted DC power is almost halted, and the DC voltage tends to increase (1.2 pu), since the DC side capacitance is being excessively charged. The proposed controller in the active power control at AC attempts to limit the DC voltage within a fixed range. The system recovers well after the fault, within 0.5 s, and damped oscillations are negligible in the reactive power. The systems with different conditions are shown in Figure 7(b) and 7(c) which are self-explanatory. At different loading conditions, the output, capacitor voltages and inductor currents are shown in Figure 8(a) and 8(b), respectively, and it is evident that, system is running ideally without any significant losses.

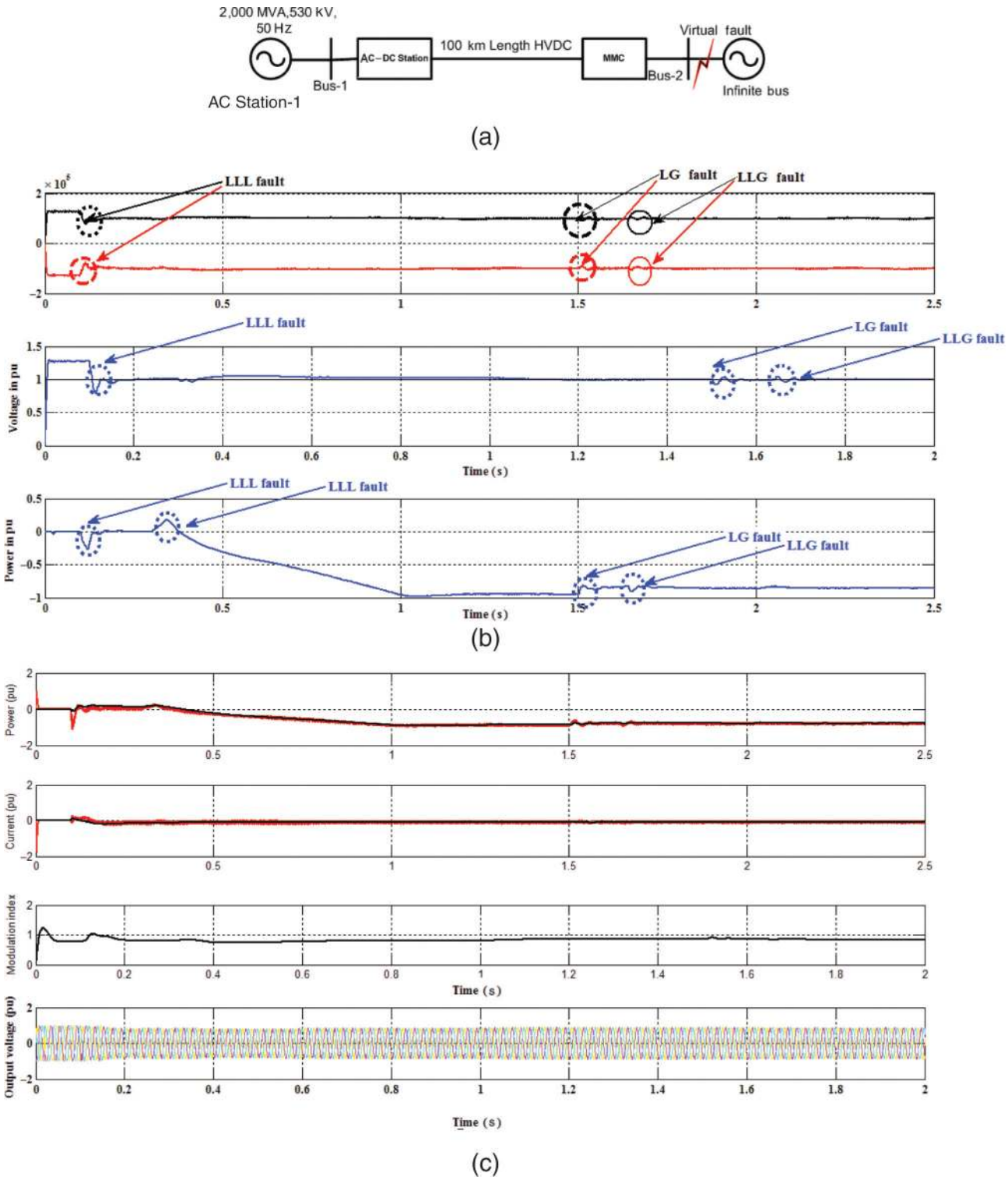

Figure 7 (a) HVDC block diagram. (b) System verification by applying different faults at different time. (c) System verification by different faults for change in modulation index

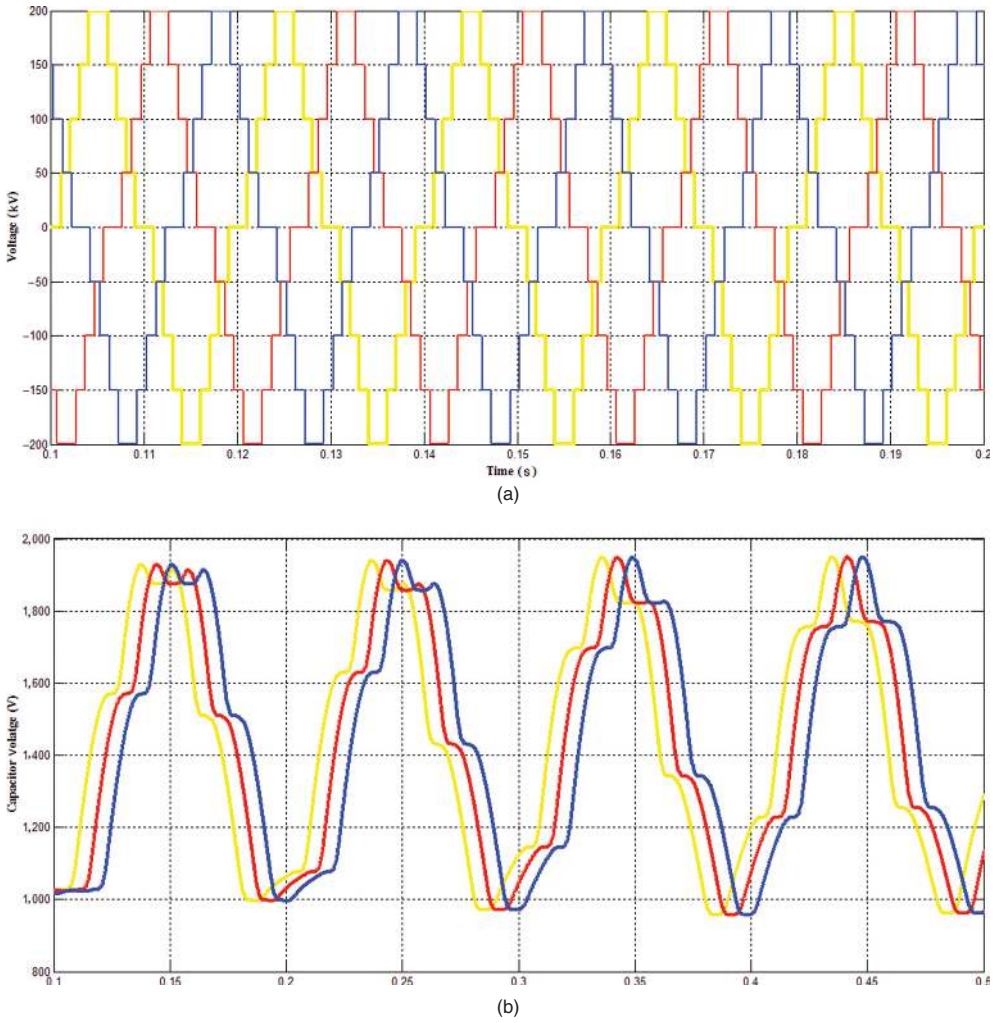

Figure 8 (a) Output voltage of five-level MMC. (b) Capacitor voltage of five-level MMC under different conditions. *X*-axis – time (s) and *Y*-axis – capacitor voltage in pu

6 Simulation and experimental results

In order to test the proposed method for mitigating the circulating currents of the MMC, computer simulation is carried out first and then verified experimentally as well.

The system has been tested with the parameters listed in Tables 5 and 6. The experimental setup has been shown in Figure 9(a).

It has been developed a model, with proposed controller that is suitable for wide range of loads with different modulation indexes.

Firstly, system has been investigated for its output voltage. Since, it is one of the important factors to access the controller performance. System without controller is distorted with its actual values and produced unwanted components called as harmonics in the system. As shown in Figure 9(b), it is clear that output voltage is distorted without controller. The RMS values of phase to neutral current are 31.4 A with controller and 29.2 A without controller. From those values, it is clear that output current is also distorted due to circulating currents. Please note that, each division is taken as 5 ms. From Figure 9(c) and 9(d), it is clear that ZVCTS operation is

Table 5 Optimum gain for proportional and integral controller

Five-level MMC	Optimum integral controller gain of KI*	Optimum proportional controller gain Kp*
1% step load for $m = 1$	1.4	3.6
10% step load	2.4	1.8

Table 6 Parameters used for five-level MMC simulation and experiment

MMC level	Five	
DC voltage	$V_{dc} = 200$ V DC	Specifications of MOSFET used for prototype.
Circulating current reference	$I_{cref} = 0$	
Arm inductors	$L_1 = L_2 = L = 3$ mH	VDS (V) = 200 (source voltage)
Switching frequency	$S_f = 100$ Hz	RDS(on) = 0.18 Ω (Resistance of MOSFET at ON condition)
Capacitor value	$C = 16$ μF/400 V	VGS = 10 V (Gate to source voltage applied)
Bandwidth of the controller	$\omega_c = 2,000$	
Load parameters	$L_r = 10$ mH/$R_r = 30$ Ω	Here, it has been considered MOSFET instead of IGBT for
Gain of resonant controller	$G_{rc} = 1{,}250$	purpose of preparing the prototype only, in actual it should
Resonant frequency of controller	$\omega_0 = 2{,}000$	use IGBT.

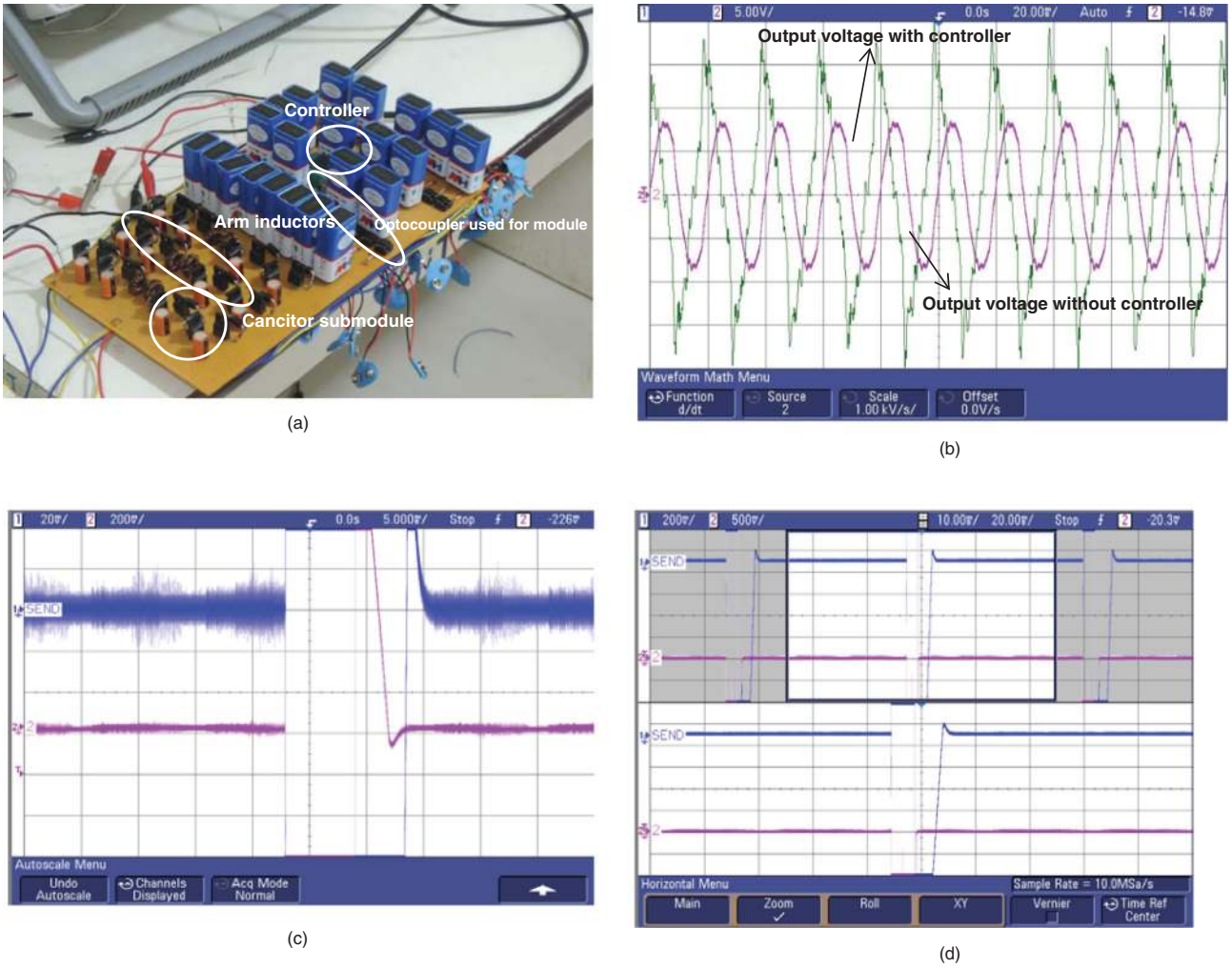

Figure 9 (a) Experimental setup for five-level MMC. (b) "R" phase to neutral voltage with and without controller. (c) ZCS turn ON and ZCT turn OFF condition for S_2. (d) ZVT turn on and ZCT turn off condition for switch S_1

verified. Due to this, the losses in the system will drastically decrease and efficiency has been increased 14% compared with system without controller. The system is exposed to sudden change in the load of 10% from its actual value at $t = 0.032$ s, due to which a sudden dip in the capacitor voltage happens at $t = 0.033$ s. Suddenly, controller senses the module voltage, sends its signal to the distorted module and makes it uniform within

0.02 s. Then, the controller reaches its steady state in 0.007 s.

At time $t = 20$ ns, the load on the system is suddenly increased by 1%, Then controller receives the signal and reciprocates appropriate signal to module, finally settled at $t = 2$ ns. Then at time $t = 60$ ns, the load on the system is suddenly increased by 10%, then the controller responded quickly and settled in time $t = 10$ ns. After this, the load on the system is then increased suddenly by 30% and it is settled in $t = 12$ ns. From this, it is concluded that, as the load increases, the controller takes a little time to settle down. All the cases, along with their zoomed views, have been shown in Figure 9(a). As modulation index changes, accordingly controller response has been observed. From the above analysis, it concludes that controller can be used for various loads and various modulation indexes. At the outset, the optimum obtained values by ISE techniques have been implemented and observed the results as shown in Figure 9(c) and 9(d). From this, it is clear that upper and lower limb currents are equal and opposite to each other. The circulating currents are completely eliminated, thereby the losses in the system have been decreased drastically and efficiency has been increased. The above-obtained results are compared with Xu et al. [2] and shown to be better than the technique proposed by them.

7 Conclusions

This paper proposed a closed-loop control method for mitigating circulating currents with ZVT and ZCT obtained by a new snubber circuit applied to the MMC. Efficiency of system substantially increased by 14% compared with conventional MMC. This method is simple in design and can substantially eliminate the RMS value of the circulating current compared with the existing method [4], while the voltages of the SM capacitors are kept well balanced. This method is very helpful for reducing power losses of the MMC in real HVDC applications and also verified by experimental results. The proposed system can be applied to wide range of loads with various modulation indexes. The steady-state analysis and harmonics can substantially be reduced by the proposed method. Both simulation and experimental results have shown the validity and effectiveness of the proposed method.

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