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Aging Degradation Impact on the Stability of 6T-SRAM Bit-cell

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Abstract

Background: In all electronic based applications, memory design is crucial which decides the performance of the system. In present technology nodes reliability is a growing concern where the static SRAM memories are not able to store the contents for a longer period of time. Reliability is mainly due to aging degradation which characterises BTI (Bias Temperature Instability) and HCI (Hot Carrier Injection) resulting in permanent damage to MOS parameters and as a result MOS deviates slightly from its normal behaviour. **Method:** In order to maintain the performance of SRAM within considerable PVT (Process Voltage Temperature) boundaries over a period of time, all the six MOSFETs strength should be dynamically adjusted. So that the ground bounce can be minimised at critical nodes of the bit-cell and stability can be maintained. **Findings:** In this paper, statistical analysis is performed on 14nm designed 6T-SRAMs and various Shmoo -plots have been developed for different PVTs considering aging impact for a span of 10 years. Analysis was performed for both SRAM read and write operation. All simulations were carried out using HSPICE-2013 version and aging models of MOSRA level-3 version 103.1. **Conclusion:** From the analysis it clearly evident that read is slightly degraded by 15%-25% were the operating voltage ranges has been degraded. In this design core voltage has been increased from 0.96v to 1.08v and periphery voltage from 0.5v to 0.62v. Thus to ensure the same performance after 10 years the operational voltage has to be increased by 20%.

Keywords: Aging and FINFET, 6T-SRAM

1. Introduction

Recent advancements in digital technologies have provided lot of space for the embedded applications to upgrade. Based on the requirements in any sort of application, complexity in designs has also increased proportionally. Thus the amount of storage memory has also increased for processing all the real-time data and preserving those data efficiently in storage areas is very crucial. In order to have a memory working close to processor frequency, high speed SRAM memories have been the best candidate. Along with the logic transistors, the SRAM bit cell has also been successfully scaled across several technologies. The problem started when the scaled devices started approaching the dimension of atomic level, where we observe lot of variations in the normal behaviour of devices due to various second order effects and process variations.

These second order effects were a result of various short channel effects like DIBL (Drain-Induced-Barrier-Lowering), GIDL (Gate-Induced-Drain-Leakage) etc. These caused a large increase in leakage currents[1] which made the planar MOSFETs deviate drastically from its normal behaviour. In order to overcome all these drawbacks much advancement were made to the physical design of planar-MOS like straining engineering, High-K Metal gates, SOI (Silicon-On-Insulator) transistor, etc. Non-planar FINFET transistors are the latest addition to the MOS device structures, having better control of gate on the channel because of its surrounded gate like structure named fin. Even the short channel effects impact on FINFET is relatively much less than the planar MOSFETs in sub-28nm technology nodes.

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Reflecting from its name 'SRAM' signifying its behaviour as 'static', the data should remain unchanged for infinite period of time unless and until there are some supply voltage variations. As SRAM is the fastest memory and the requirements of periodic refreshing are not necessary as in the case of DRAMs, SRAMs are normally preferred for cache implementation in processors and SoCs. As present technology nodes have already reached to dimensions of atomic sizes approximately to 10nm mark, the behaviour of the semiconductor devices have changed drastically due to many second order effects like Short Channel Effects (SCE) and huge device variations introduced from the fabrication process.

FINFET based SRAMs were designed in order to overcome a part of short channel effects[2] and get better control over the bitcell parameters. One more important variation introduced inherently into the design is the process variations due to inaccuracies of manufacturability of similar nanometre sized devices. These intra/inter die variations may lead to line edge roughness or random do pant fluctuations resulting in deviation in device characteristics. These variations can be characterised with the help of Monte-Carlo simulations which takes into account all the randomness included in the spice models. Due to scaling of devices, the supply voltages and threshold voltage have also scaled down. So utmost care should be taken so that data will not be corrupted in these low-V_{th} based SRAMs, because even small glitch or some noise potential added at critical nodes of bit-cell may result in data getting corrupted or bit-cell may flip its contents stored to different logic level . We will address two types of stability margins in order to analyse the performance of any memory compiler designed, one is ADM (Access Disturb Margin) during the read phase and other is WRM (Write Margin) during the write phase.

Section 2 describes the concepts of ADM and WRM along with the methodology involved in estimating the sigma. Section 3 details about aging degradation phenomena and their impact on various device parameters. In section 4 a comprehensive analysis are done over the bit-cell margins before and after degradation which are analysed for various PVTs.

2. 6T SRAM Bit-cell

Two inverters cross coupled with each other along with two pass gates connected to critical nodes of the inverters forms the general structure of an SRAM bit-cell as shown in Figure 1. The bit-lines and word-lines are connected to the pass gates which are used for reading the contents from bit-cell and writing the data into the bit-cell.

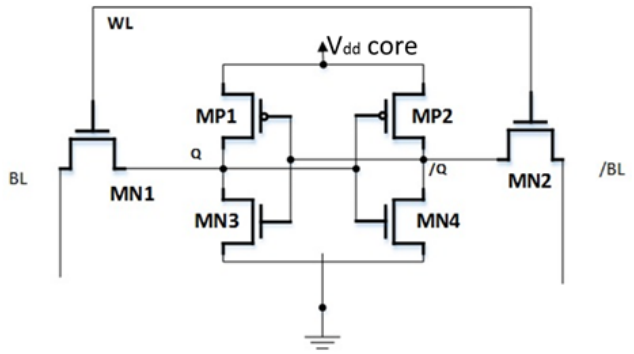

Figure 1. SRAM Bit-cell.

2.1 ADM

Access disturb margin is a measurement of read disturb. As the name itself signifies that we are accessing the contents of the bit-cell and at the same instance tending to disturb the contents of bit-cell stored[3]. This stability issue arises due to a ground bounce at the critical nodes of the cross coupled inverters. For example considering a logic '0' stored on 'Q' node in the cell. During read mode the bit-lines are pre-charged to supply voltage, and when the word line is enabled, transistors MN1, MN3 and MP2 are ON. BL will discharge through the path MN1-MN3 and this develops a potential difference between the bit-lines which is sensed by the sense amplifier.

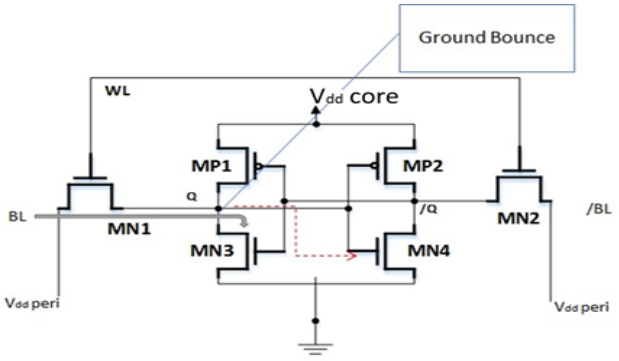

Figure 2. Ground bounce occurrence during a Read operation.

As the transistors have a finite resistance, the discharge path MN1-MN3 forms a simple potential divider and a small rise in the potential at 'Q' node is observed, i.e. previously where zero voltage was present, it may be around 100-200mV, depending on the drive strengths of

pull down and pass gates. This rise in potential is termed as "ground bounce" as shown in Figure 2. If this ground bounce approaches very close to threshold voltage of MN4, then MN4 starts to conduct slowly, resulting in drop in potential at '/Q' node thus making MN3 weaker and MP1 slightly conductive, by pulling MP1 also into the ohmic region. Subsequently the voltage at 'Q' node is further pulled up as MP1 started conducting. Hence this positive feedback process keeps on continuing until the bit-cell has flipped, MN4 and MP1 are settled into the saturation regions.

2.2 WRM

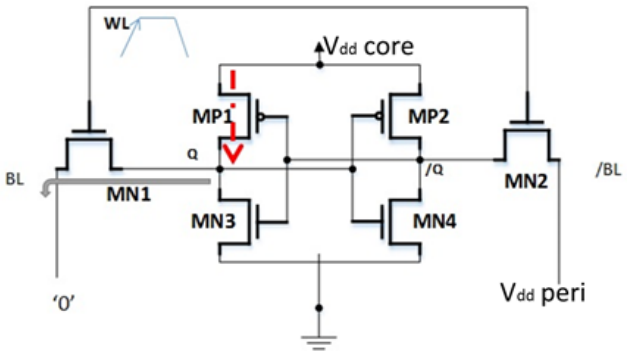

Figure 3. Write operation of bit-cell.

Write stability margin is during the write phase of the memory which provides an approximate value of the writ ability of the cell. It accounts for the ability of overwriting the previous data stored in the bit-cell. Considering logic '1' is stored in the cell, in order to overwrite with logic '0' now BL is held at '0' and /BL at '1', thus the 'Q' node will be discharged through MN1 pass gate when WL is turned ON, as shown in Figure 3.

The amount of voltage to be pulled down depends on the V_{th} of the devices, so that in this case MN4 turns OFF and also dependent on the drive strength of Pull-up transistors in order to flip the contents of the cell. When the voltage is pulled down at 'Q' node, MP1 tries to charge up the node, retaining its potential, thus PG and PU will be competing against each other. Thus the write drivers will be designed to have very high drive capabilities and strength of PU will be limited enough so that it is just capable of holding the potential in steady (ideal) state. In case the 'Q' node is not pulled below the threshold of the inverter formed by MP2 and MN4, in order to flip the contents of the cell before the WL gets disabled, it results in write failure.

2.3 Algorithm for Estimating Sigma

The procedure for estimating the bitcell's stability margin, which decides the operational voltage of the memory, is given below. All the simulations are performed using hspice[4-6]

- Find the V_{th} of all the devices: PD, PU and PG using 100nA constant current method[7]. To account for the process variations, 1K Monte-Carlo simulations are run; hence final 1-sigma V_{th} offset values are used for further calculations.
- Next find I_{crit} or delay for individual devices as described in[6].
- Based on the direction of I_{crit}, signs are assigned to the devices, i.e. if it is increasing, then '+', otherwise '-'.
- By the method of Bisection, find out the PVTA variable[6].
- Find individual hybrid offset by assigning pvta parameter to individual transistors as PVTA*Sign*1-sigma.
- Find the fail sigma or pass sigma by applying the hybrid offsets calculated previously by sweeping pvta parameter.

3. Aging Degradation

Device reliability has a severe impact on the present designs which causes performance margin issues and design failures resulting in yield loss. HCI (Hot Carrier Injection) and BTI (Bias Temperature Instability)[8-10] are the two degradation phenomena observed which affect the performance over time that needs to be clearly validated in the design phase with simulations done prior to high volume manufacturing so that there is no significant yield loss.

3.1 BTI

Normally two phenomena observed in BTI are NBTI (Negative-BTI) in PMOS, as shown in Figure 4.a, and PBTI (Positive-BTI) in NMOS, as shown in Figure 4.b[11-13]. These phenomena are a result of charges getting trapped in the dielectric (SiO_2) present above the channel when the transistor is in the inversion mode and in the absence of V_{ds} i.e. horizontal electric field.

Due to aging lot of device parameters will be degraded, all this degraded parameters can be modelled by only taking the core parameters i.e. V_{th} and I_{ds}. The shift in V_{th} and percentage change in I_{ds} is modelled as given below;

$$V_{th}\ shift = A_p\ e^{G.type.V_{gs}}\ e^{-Ea/KT}\ t_{stress}\ e^{-D.abs(V_{ds})}\ e^{mL}$$

$$\Delta I_{ds} = A_p\ e^{G.type.V_{gs}}\ e^{-Ea/KT}\ t_{stress}\ e^{D.abs(V_{ds})}\ e^{-mL}$$

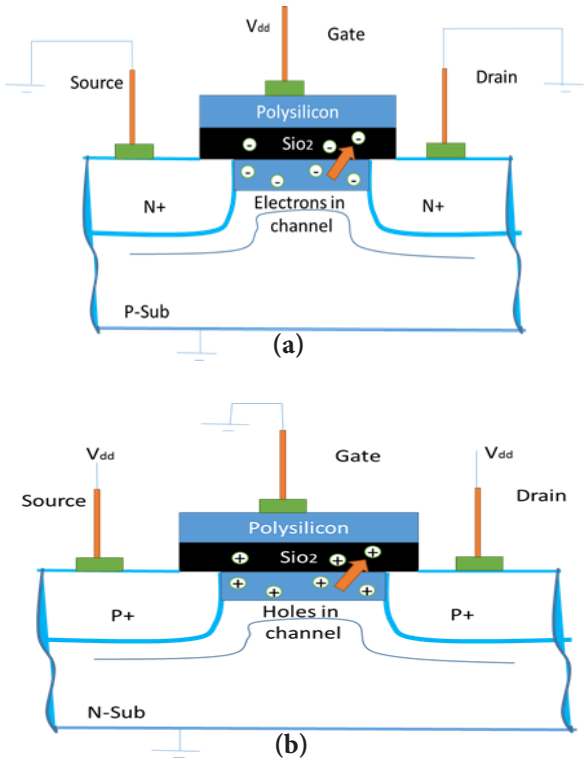

Figure 4. (a) NBTI in PMOS (b). PBTI in NMOS.

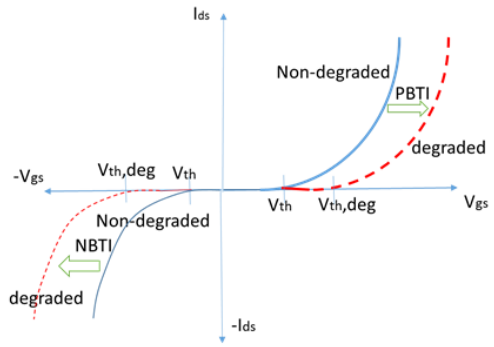

Figure 5. BTI Impact on V_{th} shift.

The BTI impact on V_{th} as modelled by the above equations can be graphically shown in Figure 5.

3.2 HCI

Hot carrier Injection is a resultant of 'HOT' carriers. When the carriers travel through the channel and pass through regions of high electric fields due to large V_{ds} they gain tremendous kinetic energy. If this mean energy is larger than that associated with the lattice in thermal equilibrium, they are called 'hot' because the carriers were historically assumed to be thermally disturbed over an effective temperaturehigher than that oflattice. These high-energy carriers 'hot carriers' can be injected into dielectric or tunnel into the dielectric layer causing interfacial damage and permanent damage of the insulation region. This results in shift in the transistor parameters, which is modelled as change in on-current.

4. Results

Based on the algorithm explained in section 2.3, SRAMs read and write stability is analysed considering 256 RPBL (Rows per bit-line). Various Shmoo-plots are derived for various voltages considering worst ever possible constraints.

4.1 ADM and WRM without Aging

Vdd Perl \ Vdd core	0.66	0.68	0.7	0.72	0.74	0.8	0.84	0.96	1.08	1.2
1.2	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS
1.08	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS
0.96	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS
0.84	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.8	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.74	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.72	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.7	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS	FAIL
0.68	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS	FAIL
0.66	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS	FAIL
0.64	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL
0.62	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL
0.6	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL
0.58	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL
0.56	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL
0.54	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL
0.52	FAIL	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL	FAIL
0.5	FAIL	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL	FAIL	FAIL

Figure 6. Shmoo-Plot of ADM.

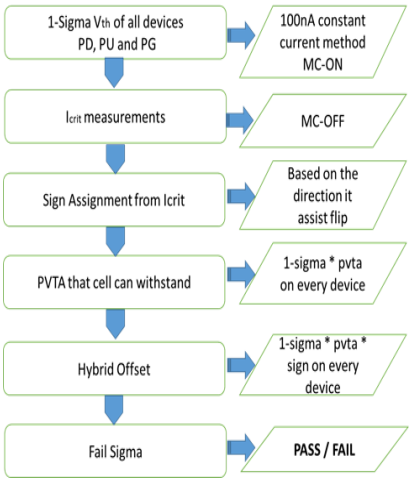

Figure 7. Step-by-step procedure for ADM analysis.

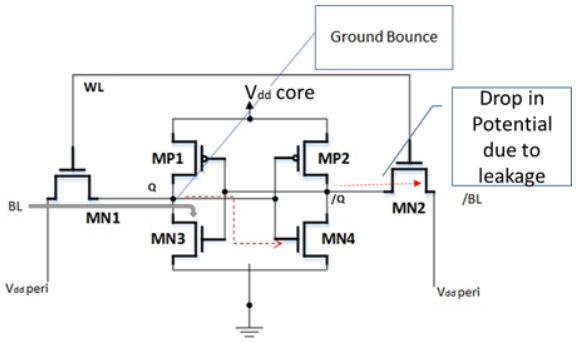

Figure 8. Bitcell flipping action due to ground bounce and leakage due to low peripheral voltage.

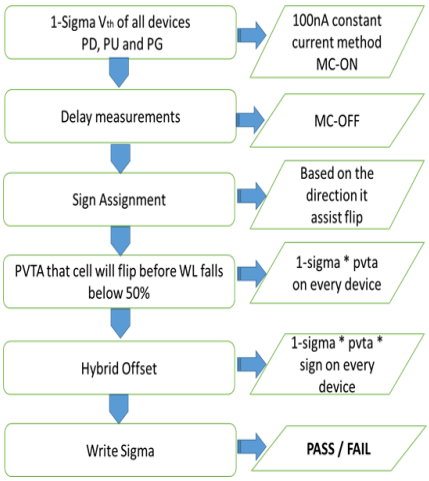

Figure 9. Step-by-step procedure for WRM analysis.

Considering the worst PVTs for ADM estimation (FSA process corner, Core and Periphery voltages varying from 0.5V to 1.2V and Temperature 125C), fail sigma for each PVT arc is found. Considering a 5-sigma as the criteria for pass or fail, Shmoo-plot is drawn as shown in Figure 6 using the step by step procedure as in Figure 7. From the Shmoo it's clearly evident that there should be sufficient amount of core voltage provided so that bit-cell is stable during the read phase, and even for very low periphery voltages the bit-cell is vulnerable to stability due to leakage taking place on the other half, as evident in Figure 8, which facilitates the flipping of stored contents as MP1 and MN4 are slowly entering into ohmic region during a read action. The cumulative feedback continues by dropping the potential at '/Q' node and raising the potential at 'Q' node. The cell ultimately flips its content due to the combined effort of ground bounce facilitated with additional leakage.

Vdd peri \ Vdd core	0.66	0.68	0.7	0.72	0.74	0.8	0.84	0.96	1.08	1.2
1.2	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
1.08	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.96	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.84	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.8	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.74	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.72	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.7	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.68	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.66	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.64	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.62	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.6	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.54	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.52	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.5	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.48	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.46	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.44	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS

Figure 10. Shmoo-Plot of WRM.

For estimating the write failures, word-line pulse of 1ns is considered and PVT (Process SFA, voltage variation from 0.44V to 1.2V and Temperature -40C) is assumed. The resultant Shmoo-plot for WRM is shown in Figure 10 following the procedure as shown in Figure 9.

4.2 ADM and WRM with Aging

As aging degradation impact on bit-cell is a dynamic behaviour, it also depends on the input stimulus and duration. Considering a total time period of 12ns and different duty cycles of the input, degradation of V_{th} is observed in Table 2 from BOL (Beginning Of Life) to EOL (End Of Life) of SRAM FETs and these degraded values are used for estimating the ADM and WRM to observe the aging impact on stability of bit-cells margins.

Table 1. BTI Parameters

Parameter	Significance	Default Value
A_p	Pre-factor	0.0
M	Length Dependency	3.0
E_a	Temperature Acceleration	0.143
D	Vds voltage dependency	0.0
G	Vgs voltage dependency	5.0
T	Time dependence	10

Table 2. BTI Impact on Threshold Voltage for various input duty cycles

Pull down NMOS		Pull up PMOS	
Duty Cycle (percentage)	ΔV_{th} (mV)	Duty Cycle (percentage)	ΔV_{th} (mV)
50:50	33.75	50:50	68.57
60:40	36.19	60:40	73.53
70:30	38.61	70:30	78.45
80:20	41.05	80:20	83.39
90:10	43.52	90:10	88.41
100:0	62.99	100:0	93.53

Vdd peri \ Vdd core	0.66	0.68	0.7	0.72	0.74	0.8	0.84	0.96	1.08	1.2
1.2	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS
1.08	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS
0.96	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS
0.84	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS
0.8	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS
0.74	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	FAIL
0.72	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	FAIL
0.7	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	FAIL	FAIL
0.68	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	FAIL	FAIL
0.66	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	FAIL	FAIL
0.64	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	FAIL	FAIL	FAIL
0.62	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	FAIL	FAIL	FAIL
0.6	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
0.58	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
0.56	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	<1.73
0.54	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	<1.2
0.52	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	<1.7	<1.7
0.5	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	<1.2	<1.2

Figure 11. Shmoo-Plot of ADM after Aging Degradation.

Taking the degraded V_{th} values considering 50:50% duty cycle, and adding it to the original threshold voltages and following the same procedure again, the degraded Shmoo-plot is obtained in Figure 11. Clearly from the Shmoo it is evident that the range of operating voltages where the SRAM can operate without any failures has been shrunk due to BTI impact on the devices. Thus over a span of 10 years the performance of the memory will be exponentially degraded as almost 50% drop in read stability is evident from the Shmoo plots.

Vdd peri \ Vdd core	0.66	0.68	0.7	0.72	0.74	0.8	0.84	0.96	1.08	1.2
1.2	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
1.08	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.96	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.84	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.8	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.74	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.72	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.7	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.68	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.66	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.64	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.62	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.6	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.54	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.52	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.5	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.48	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.46	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS
0.44	FAIL	FAIL	FAIL	FAIL	FAIL	PASS	PASS	PASS	PASS	PASS

Figure 12. Shmoo-Plot of WRM after Aging Degradation.

In a similar way, the write margins are also obtained as shown in Figure 12, which shows that write stability has improved at the cost of increased write time. Because of increased threshold voltages, if the bit-lines are capable of pulling the critical nodes below this threshold voltage then easy flipping of the contents occurs. For example, consider before aging if the threshold voltage of PMOS was around 250mV, the BL had to drop the potential of 'Q' node from V_{dd}-core by more than 250mV in order to overwrite the stored '1' to '0'. After aging, if the V_{th} has increased to 400mV, then the BL should pull the 'Q' node more than 400mV below V_{dd}-core. With increased threshold voltage, the pull-up PMOS holding the node at '1' is weakened and it allows for easy flipping of the cell.

But it is also observed that if V_{th} of the device is increased the switch ON and OFF times are increased thus making the device operations slow, and time to overwrite the previous data with new content will be increased. We can observe that although the passing voltage range remains same even after degradation, the overall write sigma is improved much more than the qualifying sigma.

5. Conclusion

Overall from the results presented, a significant drop in read stability of SRAMs can be stated due to the impact of aging phenomena. This drop in stability of bit-cell over time is almost exponential in nature. With the continued scaling of devices in the lower technology nodes, the aging impact might become more severe where stability degradation can be observed very soon from the BOL to EOL of SRAM bitcell.

6. Acknowledgment

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