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Research Article

An FPGA Chaos-Based PWM Technique Combined with Simple Passive Filter for Effective EMI Spectral Peak Reduction in DC-DC Converter

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A new and simple but effective electromagnetic interference suppression technique based on field programmable logic array (FPGA) technology to provide a significant EMI noise attenuation in DC-DC converters is discussed. The voltage controlled boost converter for EMI reduction is analyzed using FFT under traditional PWM technique and chaotic mode operation. This technique aids the DC-DC converters to comply in specified EMI limits and replace conventional bulky passive filter with a simple passive filter. A prototype model has been tested and hardware results show significant reduction of EMI in chaotic mode operation of the boost converter.

1. Introduction

Electromagnetic iterference is a man-made or natural electromagnetic disturbance signal which results in unacceptable response and sometimes in malfunctioning of an electrical or electronic device. So it is essential to suppress the EMI at switching. Though there are organizations such as IEC, IEEE, and FCC that are consistently insisting on EMC standards for different environments, the increasing essentiality of DC-DC converter in different applications [1] also increases the conducted EMI problems. Wide deployment of DC-DC power converters in emerging engineering applications such as hybrid vehicles, SMPS, satellite power supply units, and bio medical instrumentation [2] also increases the risk of EMI. Generally DC-DC converters release electromagnetic emissions because of very high switching frequency and therefore are the main sources of EMI [3, 4]. So suppressing EMI in a DC-DC converter is of great significance to clean the environment.

The EMI filters are traditionally used in power converters to attenuate switching noise and to meet the EMI standards for many years now. However, the bulkiness, design limitation for a band of frequency, parasitic reactive elements, and chance of attenuating the useful signal lead to some other effective alternatives like soft switching and random modulation techniques. However, soft switching has some limitations because of its auxiliary circuits. But incorporation of chaotic modulation, a type of random modulation method, is effective in suppression of EMI for a wider range of frequency.

Over the years, EMI filters are widely used in power electronics systems for EMI noise suppression [5, 6]. However, the parasitic effect of filter plays vital role in Common Mode and in Differential Mode EMI filters. In order to compensate the degradation caused by the parasitic elements in the common mode (CM) filter [4], another element is connected on the LISN side. Thus the pi-shaped filter is very simple, economic, and less prone to parasitic effect.

Though there are lots of techniques, such as EMI filter and shielding, for mitigation of EMI, they work as a remedy after EMI is generated [7, 8]. However, in comparison, chaotic PWM method suppresses the EMI at switching itself. Chaotic switching reduces the chance of accumulation of noise power at the multiples of central frequency greatly. Hence, the noise power spreads over a wide range of frequency resulting in reduced spectral peaks.

FPGAs—field programmable gate arrays [9] are future-oriented building bricks which allow perfect customization

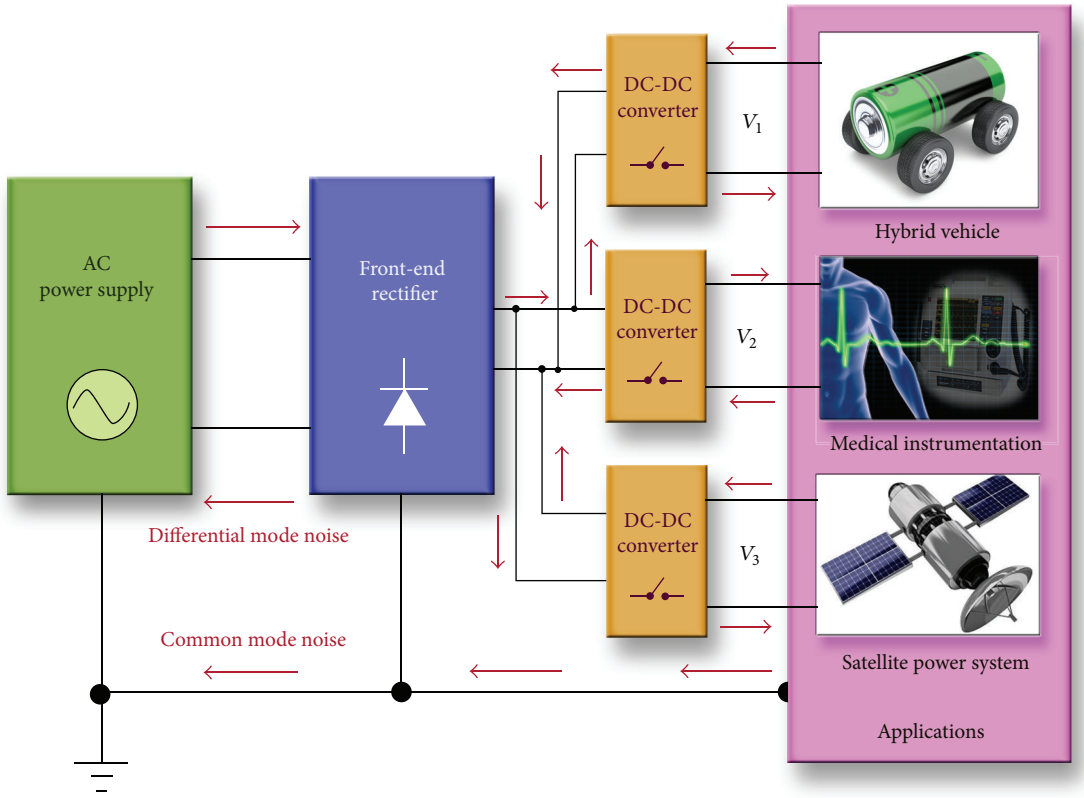


Figure 1: EMI Coupling path in ideal AC-DC power supply.

of hardware with a lesser price even for lesser units. FPGA components are easily available in different sizes and also at a cheaper price. A possibility in near future of synthesizing an application-specific integrated IP cores FPGA may avoid the time-consuming and expensive redesign of the board, especially for very specialized applications with small or medium volumes. With help of FPGA-based random pulse generation, spread spectrum scheme can be accomplished [10].

By combining the advantages of EMI filtering with chaotic PWM switching, it is possible to achieve effective spectral peak reduction in the network. Hence, in this paper, the objective of effective EMI suppression is realized by incorporating the technique by this novel combination. First, the simulations of conventional PWM technique and chaotic switching are done. Then the hardware prototype of passive filter [7] is designed for EMI filtering and later added to the chaotically switched DC-DC converter in which the hard ware prototype is driven by pulses generated using the cost-effective FPGA.

The organization of this paper is as follows. Section 2 discusses the basic topology of boost converter and circuit diagram of the proposed method. Section 3 deals with design of passive EMI filter. Section 4 describes the chaotic PWM generation and advantages of randomization of pulse frequency in detail. Section 5 deals with the simulation results and analysis of the above-discussed technique. The practical implementation and conclusion through validation are discussed in Sections 6 and 7, respectively.

Figure 1 describes the basic functionality of a power supply unit supplying different applications and the EMI coupling path. The arrow mark indicates the path of the conducted EMI through the equipment. The common mode noise enters into the medical equipment through lines and returns back via the chassis ground, wherein, the differential mode noise couples between the lines. V_1, V_2, and V_3 are different voltage levels.

2. DC-DC Power Converter

Power electronic circuits are typical examples of variable structure systems where the topology is changed due to the operation of the switching element. As a result, systems become nonlinear and time varying. Although DC-DC converters are well known for their significant advancement in power density and their low thermal dissipation, threat of generating EMI by di/dt and dv/dt at high frequencies is always been a concern. As the DC-DC converter follows a new trend of power generation, their switching frequencies have increased dramatically to reduce their dimensions.

DC-DC converter sheds electromagnetic emissions and thus forms the main source of EMI. Therefore, controlling EMI in a DC-DC converter is of great importance for cleaning

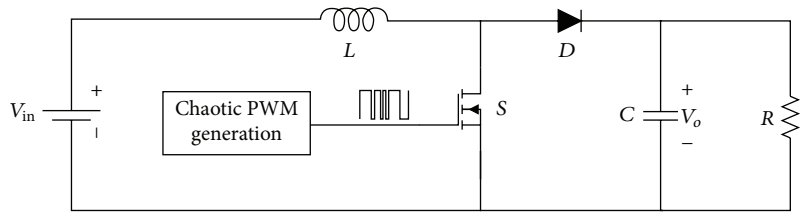


Figure 2: Basic topology of boost converter with chaotic PWM.

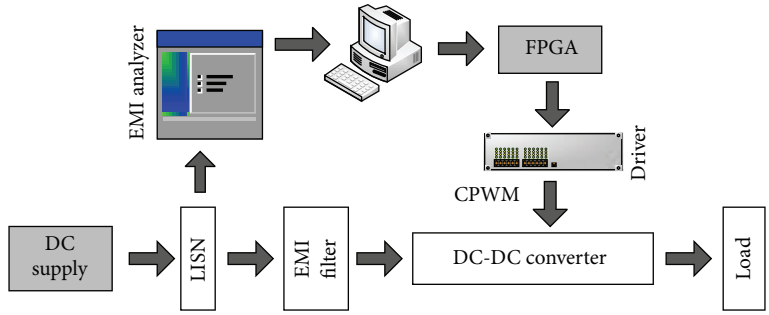


Figure 3: Block diagram for the proposed method.

the entire EMI environment. Of all types of DC-DC converters, boost converters are widely adopted and its general circuit diagram is shown in Figure 2. And the functional block diagram for the proposed combined technique is shown in Figure 3.

The elaborated circuit diagram of the proposed methodology is shown in Figure 4 which is comprised of both EMI filter [11–15] and chaotic switching method, where Inductor L, Capacitor C, Diode D, and Switch S belong to the power circuit and L_F and C_F are the filter parameters.

The LISN is stabilizing the impedance of the source and the circuit for the accurate measurement of conducted EMI generated in the boost converter. The techniques are combined for the effective reduction of the EMI as discussed earlier.

3. EMI Filter Design

EMI Filters are widely used in power electronic systems for EMI noise suppression. Conventional passive EMI filters are either one-or two-stage LC filters. EMI filters are usually composed of common mode (CM) and differential mode (DM) filters. CM filters are used to suppress CM noise, which flows through the parasitic capacitance between the power electronics systems, ground, line impedance stabilization network (LISN), and the power lines. The capacitance of common mode (CM) filter is usually limited by the safety standard-IEC60950-1. As a result, the total CM capacitance cannot be too large. Hence, to achieve the low cutoff frequency to achieve high attenuation on CM noise, the CM inductance in CM filters is usually very large. The inductors and capacitors in EMI filters are not ideal components. Firstly, they are self-parasitic [16]. For capacitors, the equivalent series inductance (ESL) is very important for its performance. Likewise in inductors, the equivalent parallel capacitance (EPC) is very important for its performance. Secondly, there are parasitic couplings between these two components. The coupling between the input and output loops of the filters is also important. For CM filters, the EPC of the CM inductors is usually the most important parasitic parameter since it may resonate with the CM inductance at very low frequencies. The magnetic flux of CM current is constrained in magnetic cores of the CM inductors and the size of CM capacitors is small, so the coupling is not as significant as that of DM filters. Here a simplified common mode passive filter is designed to aid the random modulation switching for 100 kHz central frequency for EMI suppression. The equivalent circuit for CM noise with filter is shown in the Figure 5(a).

The common mode noise is considered with high source but low load impedances and, according to the impedance mismatch criteria for EMI filter design, a Γ-shaped filter (CL topology) should be incorporated for CM noise suppression, where the capacitor is faced with an inverter and the CM choke is faced with a line impedance stabilization network (LISN). However, due to the effect of stray winding capacitance, the CM choke is no longer with an inductance property after its self-resonant frequency. In order to pay off the filtration performance degradation caused by the parasitic winding capacitance of the CM choke, another capacitor is connected on the LISN side; thus, a π-shaped filter is created. Figure 5(b) demonstrates the topology of a CM filter and CM noise source power converter, where EPC signifies the parasitic winding capacitance of the CM choke [17]. The main origin of CM noise in a pulse width modulation (PWM) converter is the mandatory parasitic capacitance distributed from converter inductor and inductive loads to ground. The capacitor C_{Y1} shown in Figure 5(b) provides

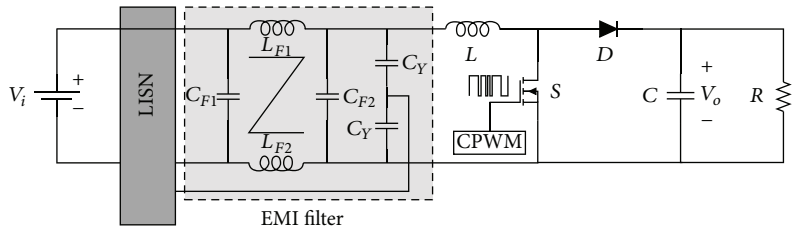


Figure 4: Circuit diagram for the proposed method.

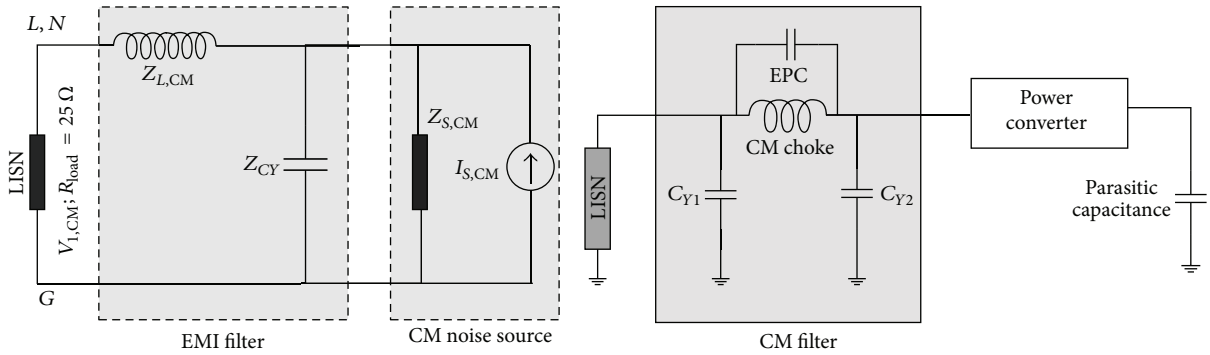


Figure 5: (a) General equivalent circuit of CM noise with filter. (b) Schematic of CM filter and CM noise source.

the return path for the current charging and discharging. The parasitic capacitance of the CM choke prevents the charging current from running through the supply lines to the LISN resistor, and the capacitor C_{Y2} is used because of the nonideal property of the CM choke [18, 19]. Therefore, it is recommended that π-shaped topology should be used for single-stage high-performance CM filter design in high-frequency applications.

The common mode filter is designed as follows. The attenuation amplitude is shown in (1) which is the ratio of common-mode voltage without filter over its counterpart with common-mode filter:

$$\left|A_{TT}\right| = \left|\frac{V_{\text{noise without filter}}}{V_{\text{noise with filter}}}\right| = \left|\frac{V_{2,\text{CM}}}{V_{1,\text{CM}}}\right|, \tag{1}$$

where $V_{\text{noise with filter}}$ is the common-mode voltage by measuring LISN with common-mode filter, in dBμV; $V_{\text{noise without filter}}$ is the common-mode voltage by measuring LISN without common-mode filter, in dBμV; R_{load} indicates the impedance of LISN and $Z_{S,\text{CM}}$ means the impedance of common-mode noise source. The common-mode voltage measured across the LISN without the common-mode filter can be derived as

$$V_{\text{noise without filter}} = V_{2,\text{CM}} = I_{S,\text{CM}} \cdot \frac{Z_{S,\text{CM}}}{R_{\text{load}} + Z_{S,\text{CM}}} \cdot R_{\text{load}}\,. \tag{2}$$

Further the reduction of (2) can be derived as shown in (3) provided that $Z_{S,\text{CM}} \gg R_{\text{load}}$:

$$V_{2,\text{CM}} = I_{S,\text{CM}} \cdot R_{\text{load}}. \tag{3}$$

$Z_{L,\text{CM}}$ means the impedance of common-mode inductance and Z_{CY} means the impedance of common-mode capacitance:

$$Z_{CY} = \frac{1}{2\pi f 2C_Y}. \tag{4}$$

The common-mode voltage measured across the LISN with the common-mode filter can be therefore derived as

$$\begin{aligned} V_{\text{noise with filter}} &= V_{1,\text{CM}} \\ &= I_{S,\text{CM}} \cdot \frac{Z_{S,\text{CM}}}{Z_{S,\text{CM}} + Z_1} \\ &\quad \cdot \frac{Z_{CY}}{Z_{CY} + Z_{L,\text{CM}} + R_{\text{load}}} \cdot R_{\text{load}}, \end{aligned} \tag{5}$$

where

$$Z_1 = \left(Z_{L,\text{CM}} + R_{\text{load}}\right) \parallel \left(Z_{CY}\right). \tag{6}$$

Further reduction of (5) can be derived as shown in (7) provided that $Z_{S,\text{CM}} \gg Z_1$:

$$V_{1,\text{CM}} = I_{S,\text{CM}} \cdot \frac{Z_{CY}}{Z_{CY} + Z_{L,\text{CM}} + R_{\text{load}}} \cdot R_{\text{load}}. \tag{7}$$

Substituting (3) and (7) into (1) yields

$$\begin{aligned} \left|A_{TT}\right| &= \frac{I_{S,\text{CM}} \cdot R_{\text{load}}}{I_{S,\text{CM}} \cdot \left(Z_{CY} / \left(Z_{CY} + Z_{L,\text{CM}} + R_{\text{load}}\right)\right) \cdot R_{\text{load}}} \\ &= \frac{Z_{CY} + Z_{L,\text{CM}} + R_{\text{load}}}{Z_{CY}}. \end{aligned} \tag{8}$$

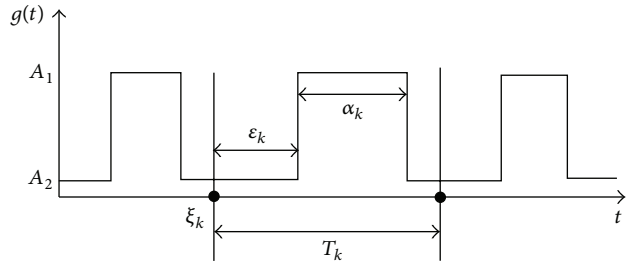


Figure 6: Randomization parameters in switching signal.

And, by (8), the impedance of common-mode inductance can be derived as follows:

$$Z_{L,\mathrm{CM}} = (A_{TT} - 1) \cdot (Z_{CY}) - R_{\mathrm{load}}. \tag{9}$$

For the output voltage 24 V and the load current of 0.2423 A, the output impedance calculated is 99.05 ohms. The filter capacitor and inductor that could be calculated from the formula (10) are 0.01606 μF and 0.158 mH. The inductor value is split with half in the hot side and half in the return side of 0.079 mH each:

$$X_L = L\omega; \qquad X_C = \frac{1}{C\omega}; \qquad f_C = \frac{1}{2\pi\sqrt{LC}}. \tag{10}$$

4. Chaotic Pulse Width Modulation (CPWM)

Pulse width modulation technique is generally used for generating the pulses required for switching operation in the DC-DC converter. In PWM, the carrier wave will be a chaotic carrier wave and the modulating signal remains the same, that is, DC signal. The frequency of the carrier wave determines the frequency of the PWM pulses; since the carrier wave is chaotic in nature [10], the PWM pulse also being chaotic; that is, the frequency will spread over a range. Therefore the main part of chaotic PWM generator is the generation of a chaotic carrier wave.

4.1. Randomization of PWM Pulse Parameters. PWM technique is generally used for generating the pulses required for the switches of the DC-DC converter. Here, for the PWM, the carrier wave is chaotic in nature and the modulating signal remains the same, that is, DC signal [10]. The theoretical setup needed to analyse randomized switching schemes is quite different from the deterministic PWM analysis approach. For a general representative scheme, the power spectrum formula can be computed. As shown in Figure 6, if the kth switching cycle begins at a time ξ_k, where

$$\xi_k = \sum_{i=0}^{k-1} T_i \quad k = 1, 2, \ldots, T_0 = 0, \tag{11}$$

then, with $u_k(t - \xi_k)$ denoting the defined single-pulse waveform, the switching function can be written as

$$g(t) = \sum_{k=-\infty}^{\infty} u_k (t - \xi_k), \tag{12}$$

where

$$u_k(t) = \begin{cases} 1, & \text{for } \varepsilon_k \le t \le \varepsilon_k + \alpha_k \\ 0, & \text{otherwise,} \end{cases} \tag{13}$$

T_k is the duration of the kth cycle, α_k is the duration of the ON state within this cycle or the ON Time, and ε_k is the delay from the beginning of the switching cycle to the turn-on within the cycle. d_k is the duty ratio (α_k/T_k), F_k is the switching frequency $(1/T_k)$.

In Figure 6, T_k is the duration of the kth cycle, α_k is the duration of the ON state within this cycle, and ε_k is the delay from the beginning of the switching cycle to the turn-on within the cycle. Note that the duty ratio is $d_k = \alpha_k/T_k$ and the switching frequency is $F_k = 1/T_k$. The switching function $g(t)$ consists of a series of such switching cycles. To spread the frequency spectrum of the switching noise, $\{F_k, d_k, \text{and/or } \varepsilon_k\}$ can be randomized. Among all the possibilities of randomization, one of the new schemes RCFMFD is designed, implemented, and addressed in this paper with the flexibility and programmability of FPGA technology.

4.2. Randomized Carrier Frequency Modulation with Fixed Duty Ratio (RCFMFD). Among the different randomized carrier frequency techniques, the RCFMFD is chosen because of its simplicity and characteristics of giving a constant output voltage for the DC-DC converter. In this scheme, the carrier frequency is randomized maintaining the duty ratio constant. This switching frequency of the random switching techniques has its own limitation such as increasing randomization range of the switching frequency increases the noise reduction until a certain ratio, after which the noise reduction again starts to decrease. The later may be due to the increased low-frequency noise and the overlaps between the successive frequency spectrum ranges. To avoid such overlapping, a superior limit of the randomization range of the switching frequency should not be taken more than ± one-third of the central switching frequency. The improved performance and cost reduction of FPGA technology have made it applicable for power supply application in DC- DC Converters.

In order to investigate the effectiveness of the stochastic variable randomness level on spreading harmonic power, a randomness level $\mathfrak{R}$ for RCFMFD is defined as follows:

$$\mathfrak{R}_{\mathrm{RCFMFD}} = \frac{T_2 - T_1}{T_S}. \tag{14}$$

In this modulation scheme, T_k varies between a minimum possible value T_1 and maximum possible value T_2. The PSD

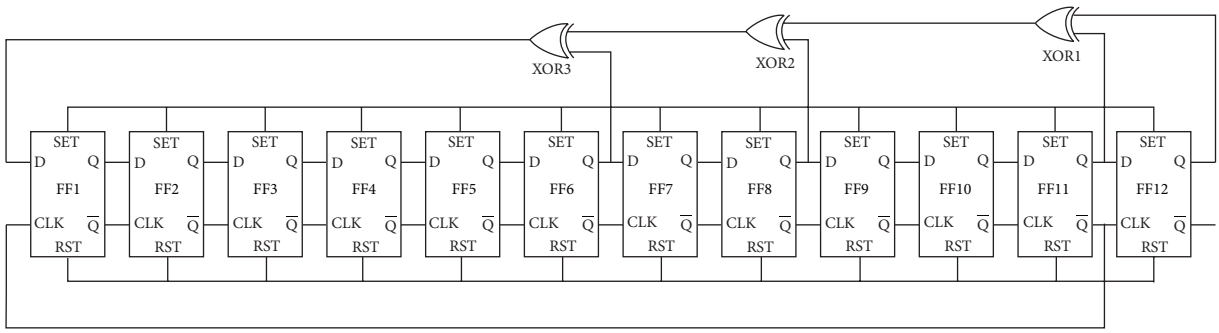


Figure 7: 12-bit linear feedback shift register.

Table 1: Spectral peak magnitude for different methods.

Method	Multiplier	Instants			
		13 ns	16.5 ns	20 ns	27.5 ns
Periodic without filter	7.3/3.2	2.7	1.82	0.69	−0.912
Chaotic without filter	5.3/3.1	0.85	0.25	−1.02	−2.04
Periodic with filter	5.8/3.1	1.31	1.12	−0.19	−1.87
Chaotic with filter	3.3/3.1	0.11	−0.21	−1.06	−1.59

$S_P(f, \mathfrak{R})$ of the waveform shown in Figure 6 with RCFMFD scheme is equal to

$$S_P\left(f, \mathfrak{R}_{\mathrm{RCFMFD}}\right) = \frac{1}{E\left[T_S\right]}\left\{E\left[\left|G\left(f\right)\right|\right]^2 + 2\,\mathrm{Re}\left\{\frac{E\left[G\left(f\right)e^{j2\pi fT_S}\right]E\left[G^*\left(f\right)\right]}{1-E\left[e^{j2\pi fT_S}\right]}\right\}\right\}, \tag{15}$$

where $G^*(f)$ is the complex conjugate of $G(f)$, and the expected terms are expressed as follows:

$$\begin{aligned}
&E\left[\left|G\left(f\right)\right|\right]^2 \\
&= \frac{2}{\left(2\pi f\right)^3 \mathfrak{R}_{\mathrm{RCFMFD}} T_S} \\
&\quad\times\left\{\left(A_2 - A_1\right)\left\{\frac{A_1}{D}\left[\sin\left(2\pi fDT_2\right) - \sin\left(2\pi fDT_1\right)\right]\right.\right. \\
&\qquad\qquad - \frac{A_2}{1-D}\left\{\sin\left[2\pi f\left(1-D\right)T_2\right]\right\} \\
&\qquad\qquad \left.\left. - \sin\left[2\pi fDT_1\right]\right\}\right. \\
&\qquad - A_1A_2\left[\sin\left(2\pi fT_2\right) - \sin\left(2\pi fT_1\right)\right] \\
&\qquad + 2\pi f\mathfrak{R}_{\mathrm{RCFMFD}}T_S\left(A_1^2 + A_2^2 - A_1A_2\right)\Big\},
\end{aligned}$$

$$\begin{aligned}
&E\left[G\left(f\right)e^{j2\pi fT_S}\right] \\
&= \frac{1}{\left(2\pi f\right)^2 \mathfrak{R}_{\mathrm{RCFMFD}} T_S} \\
&\quad\times\left\{\frac{A_1 - A_2}{1-D}\left[e^{j2\pi f(1-D)T_2} - e^{j2\pi f(1-D)T_1}\right]\right. \\
&\qquad \left. - A_1\left[e^{j2\pi fT_2} - e^{j2\pi fT_1}\right] + jA_2 2\pi f\mathfrak{R}_{\mathrm{RCFMFD}}T_S\right\} \\
&E\left[G^*\left(f\right)\right] = \frac{1}{\left(2\pi f\right)^2 \mathfrak{R}_{\mathrm{RCFMFD}} T_S} \\
&\qquad\times\left\{\frac{A_1 - A_2}{D}\left[e^{j2\pi fDT_1} - e^{j2\pi fDT_2}\right]\right. \\
&\qquad\quad - A_2\left[e^{j2\pi fT_2} - e^{j2\pi fT_1}\right] \\
&\qquad\quad \left. + jA_1 2\pi f\mathfrak{R}_{\mathrm{RCFMFD}}T_S\right\} \\
&E\left[e^{j2\pi fT_S}\right] = \frac{j}{2\pi f\mathfrak{R}_{\mathrm{RCFMFD}}T_S}\left[e^{j2\pi fT_1} - e^{j2\pi fT_2}\right].
\end{aligned} \tag{16}$$

Thus, the PSD of RCFMFD with randomness level $\mathfrak{R}_{\mathrm{RCFMFD}}$ can be obtained by substituting (4.2) into (15). The observation from the PSD shows the continuous spectrum.

4.3. Pseudorandom Number Generation. Pseudorandom number is assimilated to make the PWM period random, which can be generated using a linear feedback shift register (LFSR). A LFSR is a shift register; when clocked, it advances the signal through the register from one bit to the next Most Significant Bit. Some of the outputs are combined in

XOR configuration to form a feedback mechanism. A linear feedback shift register can be formed by performing XOR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip-flops as shown in Figure 7.

When the outputs of the flip-flops are loaded with a seed value (anything except all 0's, which would cause the LFSR to produce all 0 patterns) and the LFSR is clocked, a pseudorandom pattern of 1's and 0's is generated. Note that the only signal necessary to generate the test patterns is the clock. LFSR produces the maximum number of $(2^n - 1)$ random numbers, where n is the number of register elements in the LFSR.

The boost converter tested for conducted noise has a single switch and therefore requires a single PWM signal of central frequency of 100 kHz. Pulse width modulation signals are generated using a Xilinx Spartan-3E LX45 FPGA board, which has a clock frequency of 50 MHz; the logic used here for pulse generation is counting the clock frequency:

$$F_{\text{sw}} = F_L + (K * \text{RFS}), \tag{17}$$

where F_{sw} is the switching frequency, F_L is the Lower frequency limit (68 kHz taken), RFS is the value generated using LFSR, and K is the Constant (chosen as 2).

4.4. Algorithm and Flowchart. The randomization technique used for generation of chaotic PWM pulse is RCFMFD. The algorithm can be written as follows.

(i) Initialize the PWM period value and count value and instantiate the LFSR module.

(ii) Always when a positive edge of clock occurs, do the following steps.

(iii) Calculate the ON time for the PWM signal based on required duty cycle and PWM period value.

(iv) Initially begin with ON pulse increment count with 1 on each positive edge of clock till count reaches ONtime. Now make PWM pulse OFF, increment count with 1 on each positive edge of clock till count value reaches the PWM period value.

(v) When the count value exceeds the PWM period value, reinitialize count with 1 and calculate the next PWM period value by adding LFSR output value with a fixed value corresponding to the maximum frequency.

And also it can be represented through flowchart shown in Figure 8.

5. Simulation Study

The various cases like PWM without and with filter and chaotic switching without and with filter are simulated in MATLAB/SIMULINK. The FFT of the common-mode output voltages is obtained. Figures 9(a) and 9(b) depict the conventional PWM technique and chaotic modulation without filter. Figures 10(a) and 10(b) depict the conventional PWM technique and chaotic modulation with the simple passive π filter. From the FFT it can be observed that the spectral peaks are reduced drastically in chaotic modulation using filter.

6. Hardware Results and Discussion

In order to verify the effectiveness of the proposed algorithm a hardware prototype with the specification mentioned in Table 1 is developed and tested. To implement the RCFMFD, the power switch is operated at a randomized frequency with the central frequency of 100 kHz, and the output voltage is varied by varying the duty cycle. The design values of boost converter is given as $L = 0.29$ mH, $C = 0.5\ \mu$F, $V_i = 12$ V, and $V_o = 24$ V with a duty cycle of 0.5 at a switching frequency of 100 kHz.

The programming and interfacing are done by Xilinx Spartan-3E XC3S500E FPGA board associated with Xilinx ISE Design Suite 13.1_2. The chaotic PWM pulses that are generated using Xilinx Spartan-3E XC3S500E FPGA are fed to the designed prototype boost converter to analyze and investigate the effect of randomization of carrier wave in reducing the conducted noise. The Xilinx Spartan-3E XC3S500E FPGA board has an oscillator frequency of 50 MHz and gives an output voltage of 3.3 V. This voltage is not sufficient enough to drive the switching device MOSFET IRF 540; therefore an amplifier and Opto-coupler circuit are being employed for making the gate pulses to 10 V.

The generated periodic and RCFMFD PWM pulses are shown in Figures 12(a) and 12(b). It is observed that, when DC-DC converter is switched periodically, it results in higher amplitude of peaks at the multiples of central frequency because of the accumulation of noise power as shown in the Figure 11(a). In which, the peaks 7.3 dB, 3.54 dB, 2.85 dB, and 1.71 dB could be observed at the multiples of central frequency, whereas from the Figure 13(b) and Figure 14(b) it can be concluded that the chaotic switching with and without filter makes the spectral power to be distributed over the wide range of the frequency. However the noise generated by the periodic switching is also reduced considerably by using the filter alone as shown Figure 14(a). The simulation results also support the hardware result. The comparisons of FFT obtained with different methods are graphically shown in the Figure 15 and the results are tabulated in Table 1.

7. Conclusion

The effect of FPGA-based chaotic PWM technique using RCFMFD spread spectrum scheme along with EMI filter on the conducted noise characteristics of a DC-DC converter (boost converter) has been experimentally investigated. The FFT analysis shows that the spectral peaks are reduced drastically in chaotic modulation using filter. The chaotic modulation is also more effective compared to PWM with and without filter. From Table 1 it can be observed that, at instant of 13 ns and 16.5 ns, the chaotic switching with filter is more effective than the other techniques. The max dBV is 3.3 dBV in chaotic switching with filter whereas, it is 7.3 dBV in conventional PWM technique without filter. The

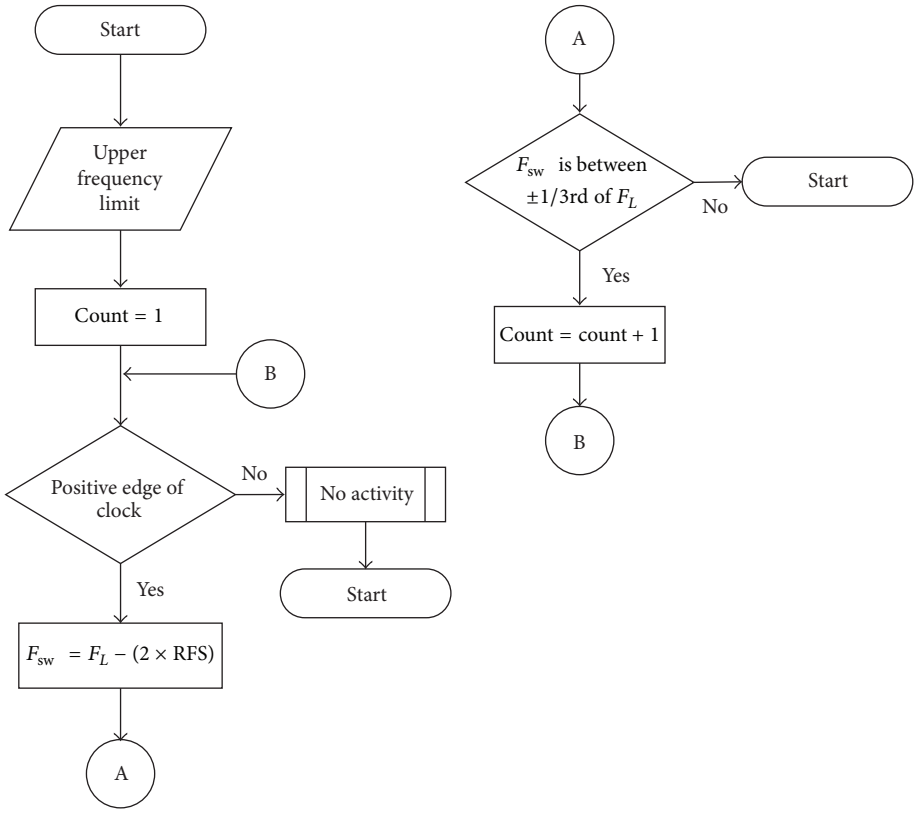


Figure 8: Flowchart for RCFMFD-based chaotic PWM generation.

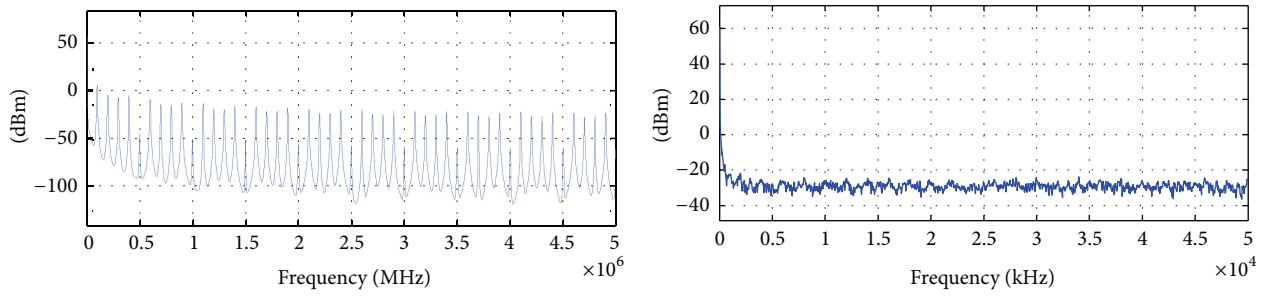


Figure 9: (a) FFT of output voltage without EMI filter for periodic pulses. (b) FFT of output voltage without EMI filter for chaotic pulses.

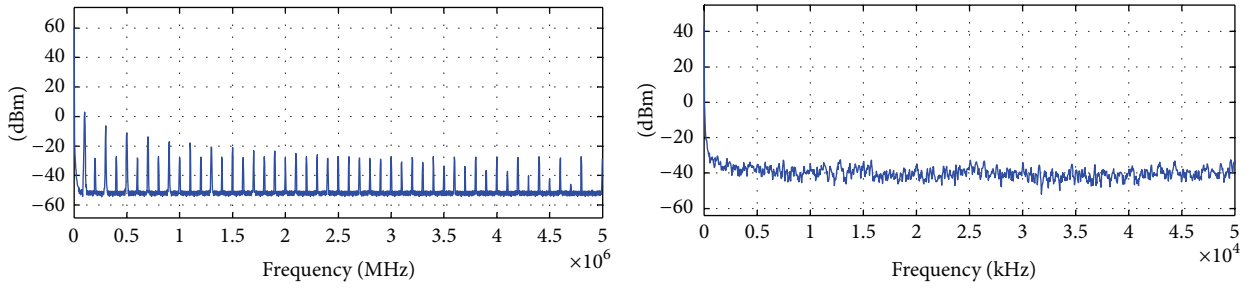


Figure 10: (a) FFT of output voltage with EMI filter for periodic pulses. (b) FFT of output voltage with EMI filter for chaotic pulses.

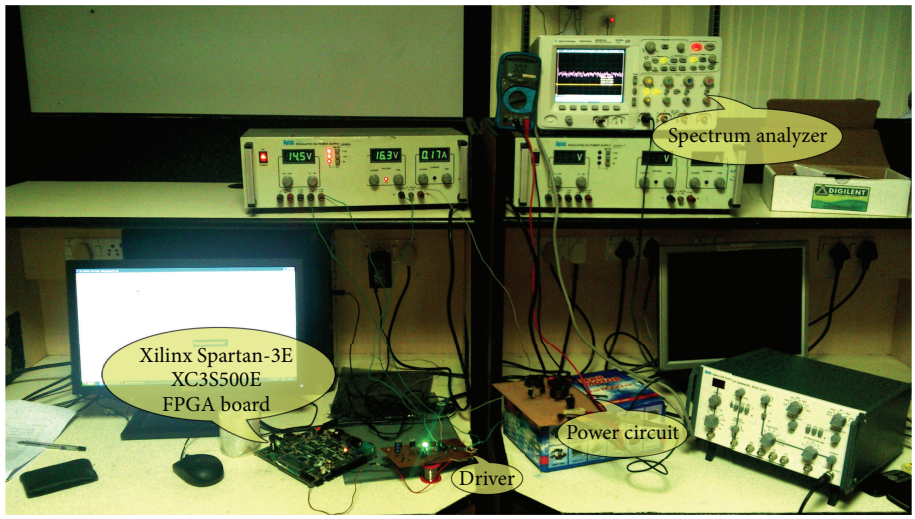
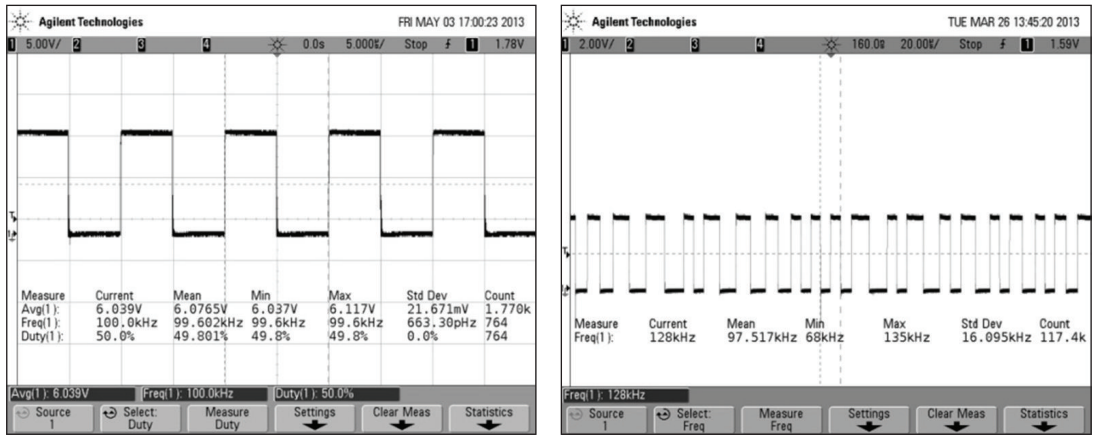
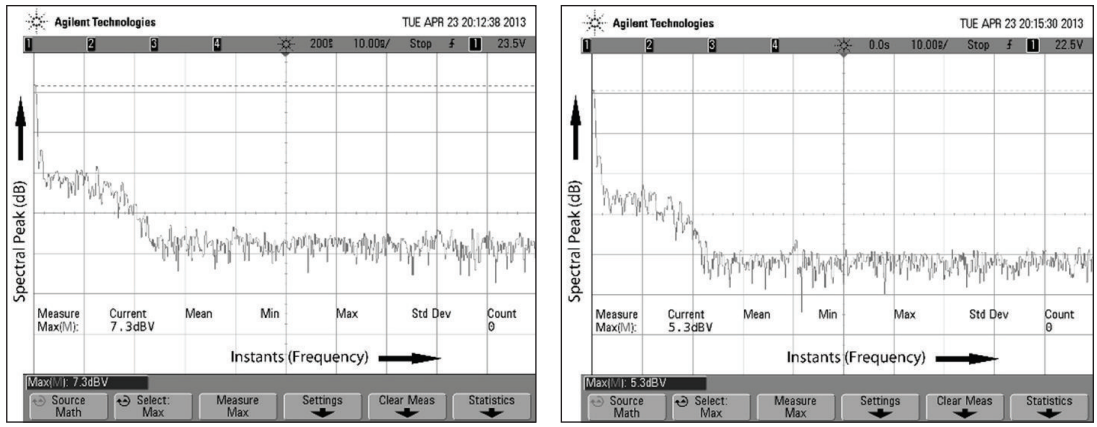


Figure 11: Hardware setup.



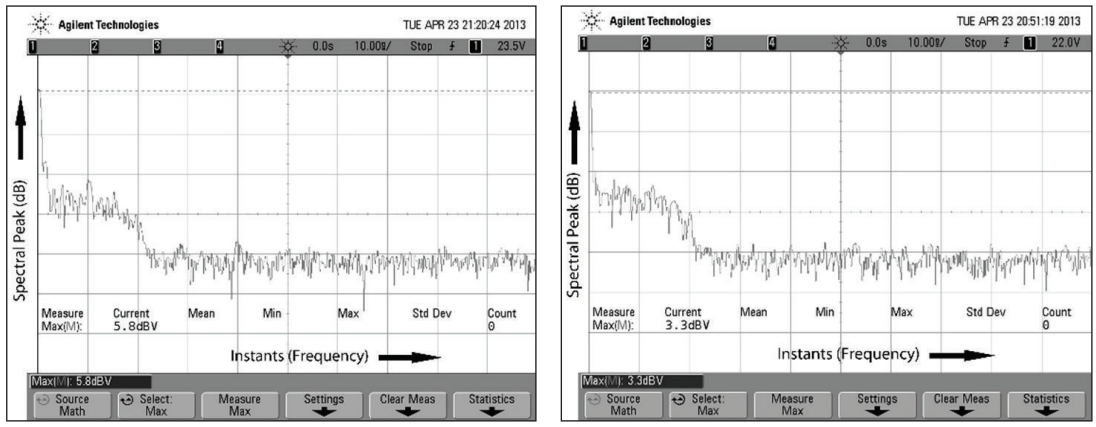
(a) (b)

Figure 12: (a) Periodic PWM pulse of 100 kHz. (b) CPWM pulses in the range ±1/3 rd of 100 kHz.



(a) (b)

Figure 13: FFT of output voltage without EMI filter for (a) periodic pulses and (b) chaotic pulses.



(a) (b)

Figure 14: FFT of output voltage with EMI filter for (a) periodic pulses and (b) chaotic pulses.

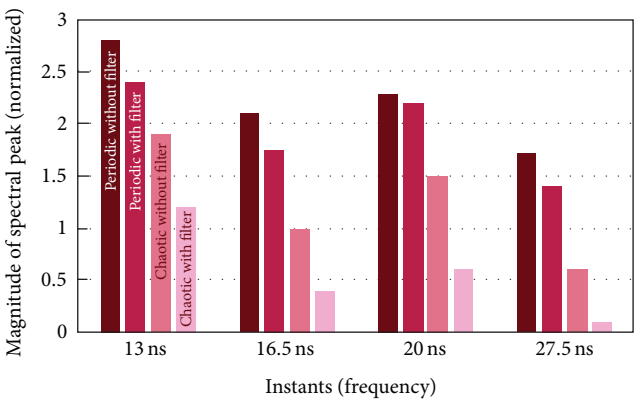


Figure 15: Comparison of spectral peak magnitude.

mitigation of spectral peaks after 20 ns is very promising. The scheme also illustrates the spreading of energy over the specified range of frequency. The chances of equipment malfunction, misdiagnose in medical instrumentation, performance degradation, and source of radiated emission are greatly reduced. The proposed scheme also improves the electromagnetic compatibility of the power supply unit very effectively.

Nomenclature

L: Inductor
C: Capacitor
R: Load resistor
S: Power switch
D: Power diode
V_{in}: Input voltage
V_o: Output voltage
T_S: Switching time period
T_k: Duration of the kth cycle
α_k: Duration of the ON state within this cycle
ε_k: Delay form the beginning of the switching cycle to the turn-on within the cycle
$q(t)$: The switching function
ξ_k: Time at which kth switching cycle begins
F_k: Switching Frequency.

Abbreviations

EMI: Electromagnetic Interference
EMC: Electromagnetic Compatibility
FPGA: Fieldprogrammable gate array
PWM: Pulse width modulation
CPWM: Chaotic pulse width modulation
PCB: Printed circuit board
LFSR: Linear feedback shift register
PSD: Power spectral density
RCFMFD: Randomized carrier frequency modulation with fixed duty ratio
LISN: Line impedance stabilization network
ESL: Equivalent series inductance
EPC: Equivalent parallel capacitance.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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