Braun's Multiplier Implementation using FPGA with Bypassing Techniques.

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Abstract:

The developing an Application Specific Integrated Circuits (ASICs) will cost very high, the circuits should be proved and then it would be optimized before implementation. Multiplication which is the basic building block for several DSP processors, Image processing and many other. The Braun multipliers can easily be implemented using Field Programmable Gate Array (FPGA) devices. This research presented the comparative study of Spartan-3E, Virtex-4, Virtex-5 and Virtex-6 Low Power FPGA devices. The implementation of Braun multipliers and its bypassing techniques is done using Verilog HDL. We are proposing that adder block which we implemented our design (fast addition) and we compared the results of that so that our proposed method is effective when compare to the conventional design. There is the reduction in the resources like delay LUTs, number of slices used. Results are showed and it is verified using the Spartan-3E, Virtex-4 and Virtex-5 devices. The Virtex-5 FPGA has shown the good performance as compared to Spartan-3E and Virtex-4 FPGA devices.

Key words:

Digital Signal Processing (DSP), Field Programmable Gate Array (FPGA), fast addition, Spartan-3E, truncated multiplier, Verilog HDL, Virtex-4, Virtex-5, Virtex – 6 Low power.

1. INTRODUCTION

Multiplication – an important fundamental function in arithmetic operation. Currently implemented in many DSP applications such as FFT, Filtering etc., and usually contribute significantly to time delay and take up a great deal of silicon area in DSP system. Now – a – days time is still an important issue for the determination of the instruction cycle time of the DSP chip. Both the multiplication and the DSP play a vital role in the implementation of VLSI system.

Multiplication – Repeated addition of n – bits will give the solution for the multiplication. ie. Multi-operand addition process. The multi – operand addition process needs two n – bit operands. It can be realized in n- cycles of shifting and adding. This can be performed by using parallel or serial methods. This will be simple to implement in two's complement representation, since they are independent of the signs. It is advantageous to exploit other number systems to improve speed and reduce the chip area and power consumption.

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Generally multiplications can be carried out in all the types of number system. The one which carried out for the Binary number system is the Digital Multiplier.

A **Field-programmable Gate Array** (**FPGA**) is an integrated circuit designed to be configured by the customer or designer after manufacturing. Field Programmable means that the FPGA's function is defined by a user's program rather than by the manufacturer of the device. A typical integrated circuit performs a particular function defined at the time of manufacture. In contrast, the FPGA's function is defined by a program written by someone other than the device manufacturer. Depending on the particular device, the program is either 'burned' in permanently or semi-permanently as part of a board assembly process, or is loaded from an external memory each time the device is powered up. This user programmability gives the user access to complex integrated designs without the high engineering costs associated with application specific integrated circuits (ASIC).

2. BRAUN MULTIPLIERS:

It is a simple parallel multiplier generally called as carry save array multiplier. It has been restricted to perform signed bits. The structure consists of array of AND gates and adders arranged in the iterative manner and no need of logic registers. This can be called as non – addictive multipliers. **Architecture:**

An n*n bit Braun multiplier [9] & [10] is constructed with n (n-1) adders and n^2 AND gates as shown in the fig.1, where,

X: 4-bit multiplicand

Y: 4-bit multiplier

P: 8-bit product of X and Y

$P_n = X_i Y_j$ is a product bit

The internal structure of the full adder can be realized using FPGA. Each products can be generated in parallel with the AND gates. Each partial product can be added with the sum of partial product which has previously produced by using the row of adders. The carry out will be shifted one bit to the left or right and then it will be added to the sum which is generated by the first adder and the newly generated partial product.

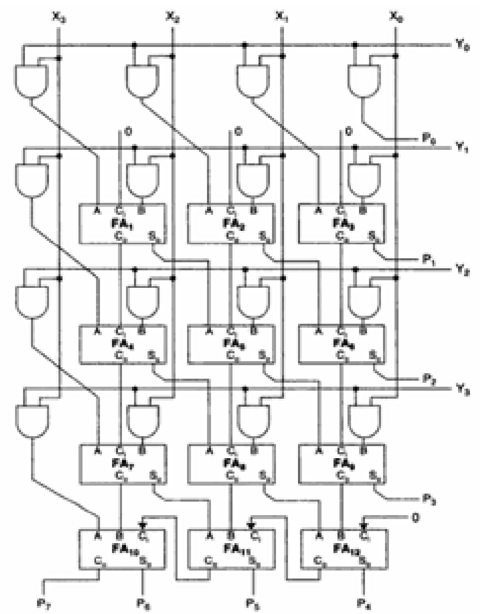

fig.1 Braun Muliplier

The shifting would carry out with the help of Carry Save Adder (CSA) and the Ripple carry adder should be used for the final stage of the output. Braun multiplier performs well for the unsigned operands that are less than 16 bits in terms of speed, power and area. But it is simple structure when compared to the other multipliers. The main drawback of this multiplier is that the potential susceptibility of Glitching problem due to the Ripple Carry Adder in the last stage. The delay depends on the delay of the Full Adder and also a final adder in the last. The power and area can also be reduced by using two bypassing techniques called **Row bypassing technique (fig. 2) [4 & 3]** and **Column bypassing technique (fig. 3) [4]**.

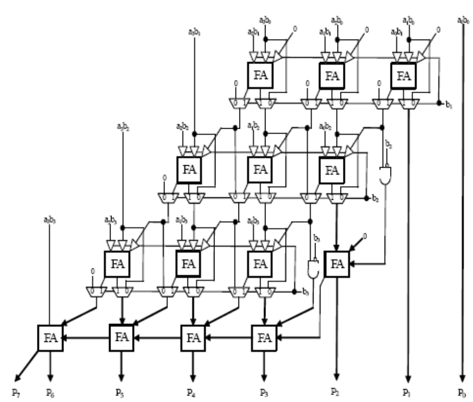

Fig. 2 4*4 row bypassing

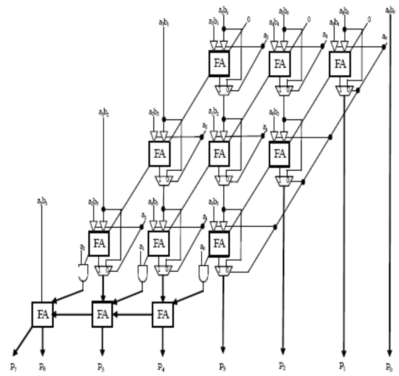

Fig. 3 4*4 column bypassing

In this paper we have simulated and synthesized the Braun's multiplier and the bypassing multipliers (row bypassing and column bypassing) and then we compare the results of the multipliers. The objective of this study is to present a comparative study of Braun's multiplier and bypassing technique using Spartan-3E, Virtex-4, Virtex-5 and Virtex 6 low power FPGA devices.

3. PROPOSED METHOD:

The Braun's Multiplier (fig. 1) which uses the full adder block adding the PP. in the proposed method we have used the fast addition [9] method so that we are reducing the number of slices, LUTs, and the delay is getting reduced. The fig. 4 which shows the proposed method of the Braun's multiplier.

In the proposed method the number of LUTs, slices are reduced and mainly the delay has been very less when compare to the conventional method. The table.1 will give the comparison result of the all the methods which is simulated and synthesized and tested in the FPGA boards.

The Row bypassing and the Column bypassing method also simulated and synthesized by using the proposed method. Table 1 will show the result of those multipliers.

3a. TWO DIMENSION BYPASSING TECHNIQUE:

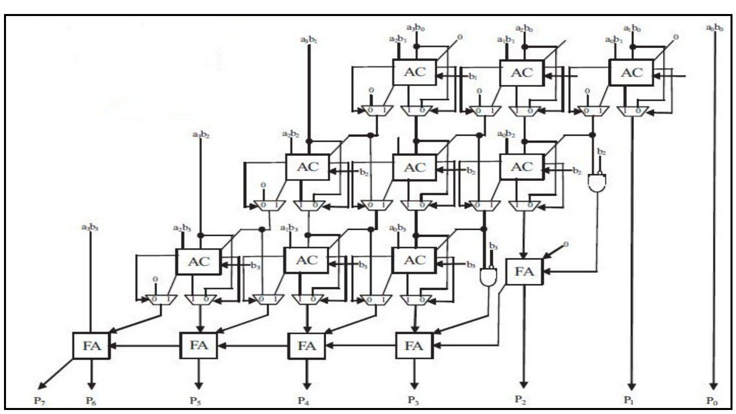

Fig 4. 4x4 2D Bypassing Multiplier ***in Braun Multiplier***

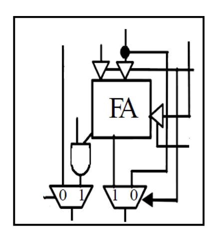

fig. 5. Adder cell

The modified Adder cell in two-dimensional bypassing Fig.4. consists of a FA, 3 tri-state buffers, two 2-to-1 mux and an extra AND gate at the carry output of the FA as shown in Fig.5. To correct the carry propagation in the multiplication result, the addition operations in the $(i+1)^{th}$ column or the j^{th} row cannot be bypassed if the bit a_i is 0, the bit b_j is 0, and the carry bit, $c_{i,j-1}$, is 1. Hence, the bypass logics are added into the necessary FA to form a correct adder cell (AC).

3b.ROW AND COLUMN BYPASSING TECHNIQUE

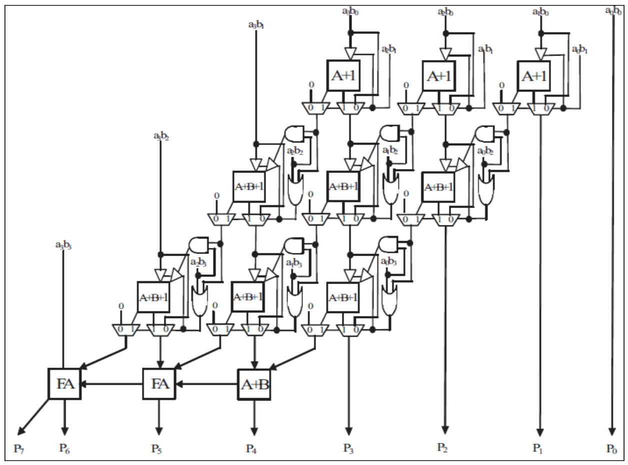

Fig. 6. Column and row bypassing multiplier

The carry bit in the $(i+1, j)^{th}$ FA can be replaced by the AND operation of the product, a_ib_j and the carry bit $c_{i,j-1}$. For the addition operation in FA, the $(i+1, j)^{th}$ FA, $1 < j < n$, can be replaced with the modified half adder, A+B+1(Fig.6(c)) and the HAs in the first row of CSAs can be replaced with the incremental adder, A+1(Fig.6(a)). Based on the operation simplification of full adders in an array multiplier, a low-power multiplier with row and column bypassing can be obtained.Besides that, each simplified adder, A+1, in the CSA array is only attached by one tri-state buffer and two 2-to-1 multiplexers and each simplified adder, A+B+1, in the CSA array is only attached by two tri-state buffers and two 2-to-1 multiplexers.

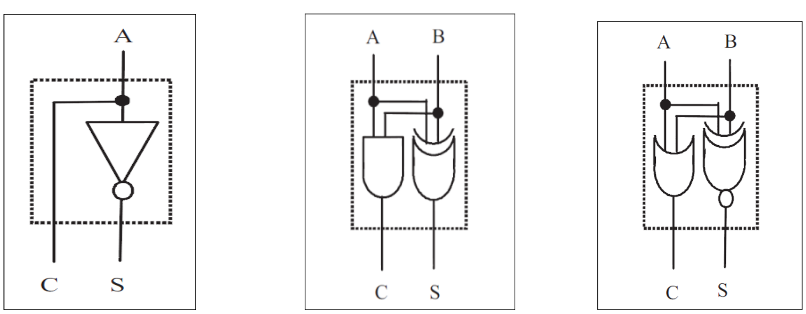

Fig.6 (a) A+1 Adder (b) A+B Adder (c) A+B+1 Adder

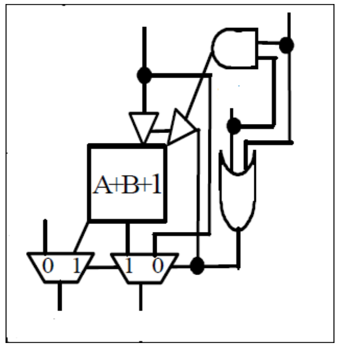

Fig.7 Row & Column Bypassing Adder Cell.

4. IMPLEMENTATION USING SPARTAN 3E, VIRTEX 4, VIRTEX 5 AND VIRTEX 6 Low Power FPGA DEVICES [11]:

4.1 FPGA design and implementation results: The design of standard, row bypassing, column bypassing and the proposed 4×4 multipliers are simulated and synthesis using Verilog HDL and implemented in the Xilinx Spartan – 3E (xc3s500e-4ft256), Virtex – 4 (xc4vlx15-10-sf363), Virtex – 5 (xc5vlx30-1-ff324), and Virtex – 6 ((xc6vlx75tl-1L-ff484) FPGAs using the Xilinx ISE 12.4 design tool and as well as simulated using the Design Architect tool of Mentor Graphics.

Table 1: FPGA resource utilization for standard, row and column bypassing and proposed 4*4 multiplier for Spartan-3E (xc3s500e-4ft256)

Spartan 3E (xc3s500e 4ft256)					
multipliers	% of No. of LUTs	% of No. of slices	% of IOBs	combinational delay(ns)	average delay(ns)
Standard Bran's Multiplier	36	22	16	21.224	7.555
Row Bypassing	33	21	15	22,340	7
Column Bypassing	33	20	16	24.757	6.57
Proposed Multiplier	31	21	13	20.757	6.444
Two Dimensional Multiplier	29	18	12.601	18.629	5.452

Table 2: FPGA resource utilization for standard, row and column bypassing and proposed 4*4 multiplier for Virtex – 4(xc4vlx15-10-sf363)

Virtex – 4(xc4vlx15-10-sf363)					
multipliers	% of No. of LUTs	% of No. of slices	% of IOBs	combinational delay(ns)	average delay(ns)
Standard Bran's Multiplier	31	19	16	20.726	9.691
Row Bypassing	31	17	14	19	6
Column Bypassing	32	17	15	19.112	6.634
Proposed Multiplier	28	16	16	19.43	6.1
Two Dimensional Multiplier	26	14	14.67	17.098	7.24

Table 3: FPGA resource utilization for standard, row and column bypassing and proposed 4*4 multiplier for Virtex – 5(xc5vlx30-1-ff324)

Virtex – 5(xc5vlx30-1-ff324)					
multipliers	% of No. of LUTs	% of No. of slices	% of IOBs	combinational delay(ns)	average delay(ns)
Standard Bran's Multiplier	29	18	14	17.67	6.873
Row Bypassing	29	16	15	20	6.334
Column Bypassing	28	15	13	16.008	6.1
Proposed Multiplier	27	15	14	15.967	5.656
Two Dimensional Multiplier	26	13	13.4	13.652	6.1452

Table 4: FPGA resource utilization for standard, row and column bypassing and proposed 4*4 multiplier for Virtex – 6 Low power (xc6vlx75tl-1L-ff484)

Virtex – 6 Low power (xc6vlx75tl-1L-ff484)					
multipliers	% of No. of LUTs	% of No. of slices	% of IOBs	combinational delay(ns)	average delay(ns)
Standard Bran's Multiplier	25	16	14	16.87	6.89
Row Bypassing	24	15	12	14	6.023
Column Bypassing	21	13	12	15.76	5.784
Proposed Multiplier	19	12	13	9.214	4.032
Two Dimensional Multiplier	17	12	11	12.832	4

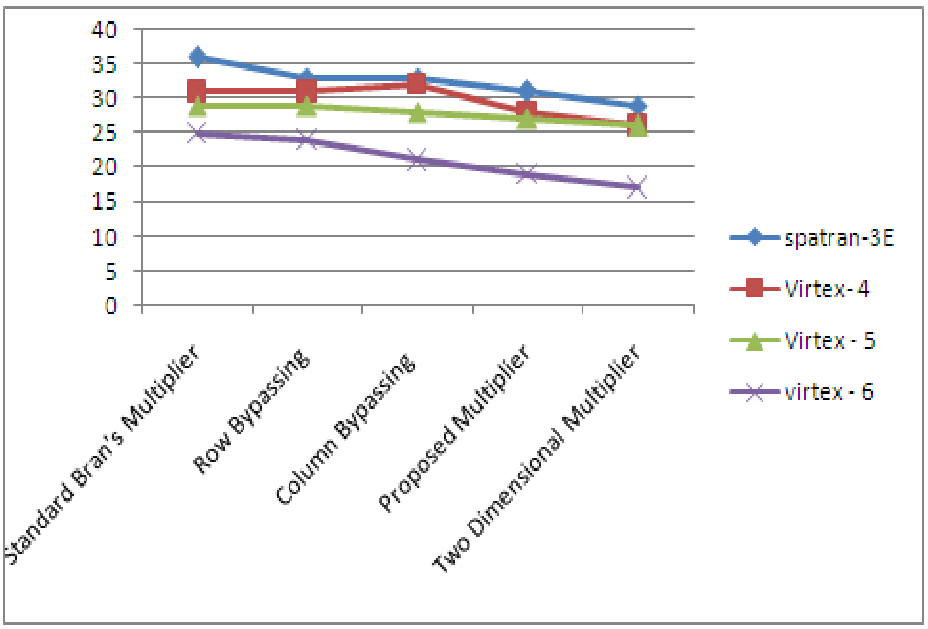

Fig. 8 The LUTs for Spartan-3AN, Virtex-4, Virtex - 5 and Virtex-6 for standard, row and column bypassing and proposed 4*4 Braun's multipliers

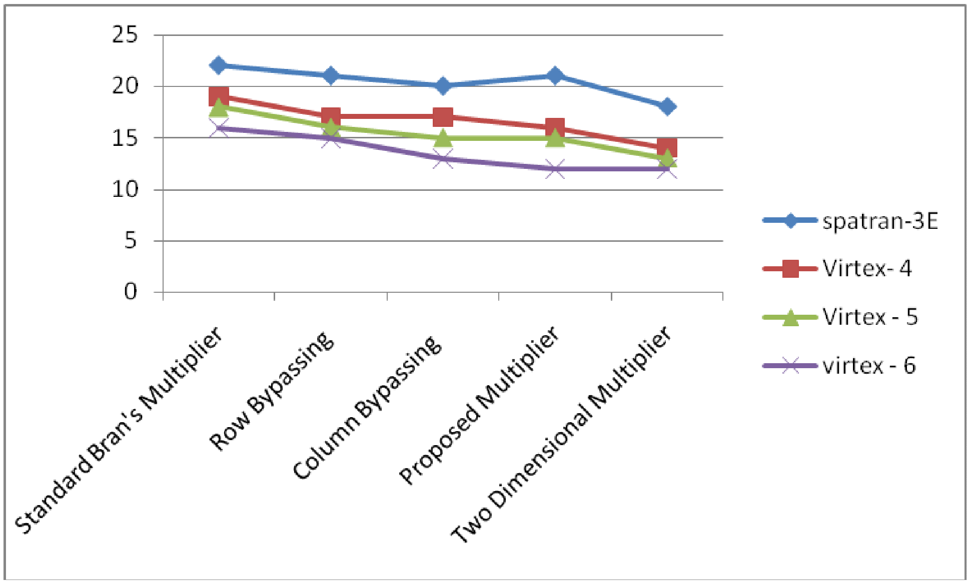

Fig. 9 The Slices for Spartan-3AN, Virtex-4, Virtex - 5 and Virtex-6 for standard, row and column bypassing and proposed 4*4 Braun's multipliers

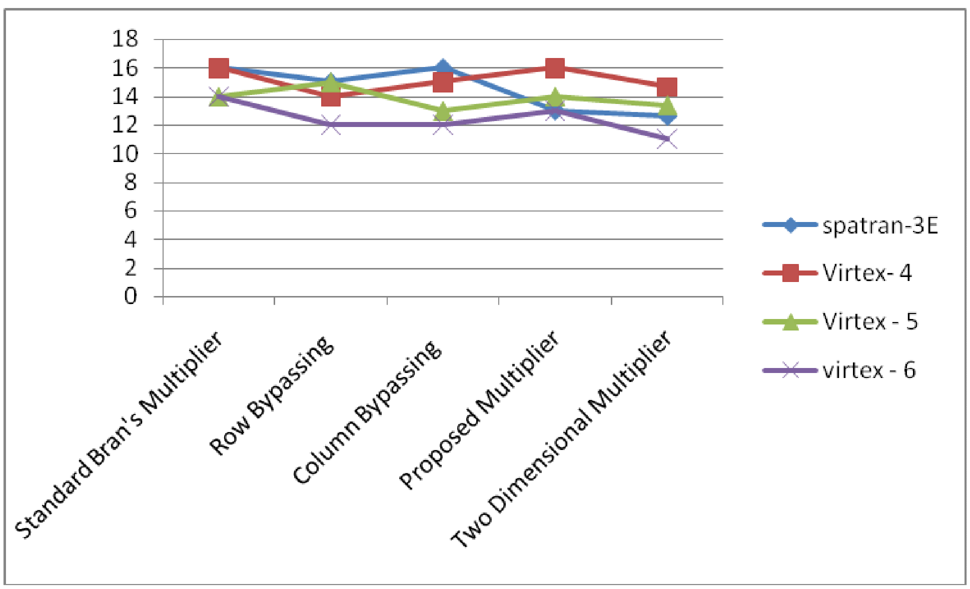

Fig. 10 The bonded IOBs for Spartan-3AN, Virtex-4, Virtex - 5 and Virtex-6 for standard, row and column bypassing and proposed 4*4 Braun's multipliers

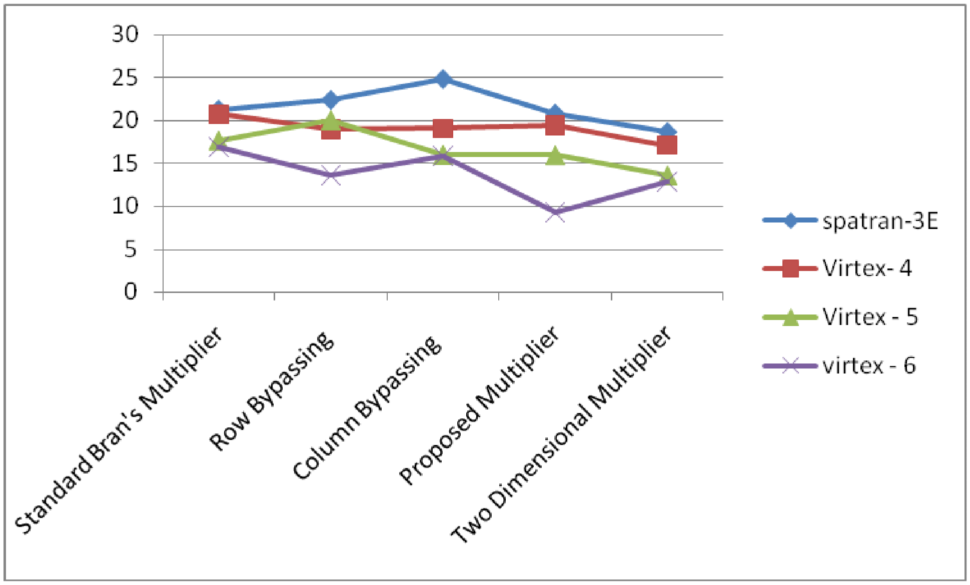

Fig. 11 The combinational path delay for Spartan-3AN, Virtex-4, Virtex - 5 and Virtex-6 for standard, row and column bypassing and proposed 4*4 Braun's multipliers

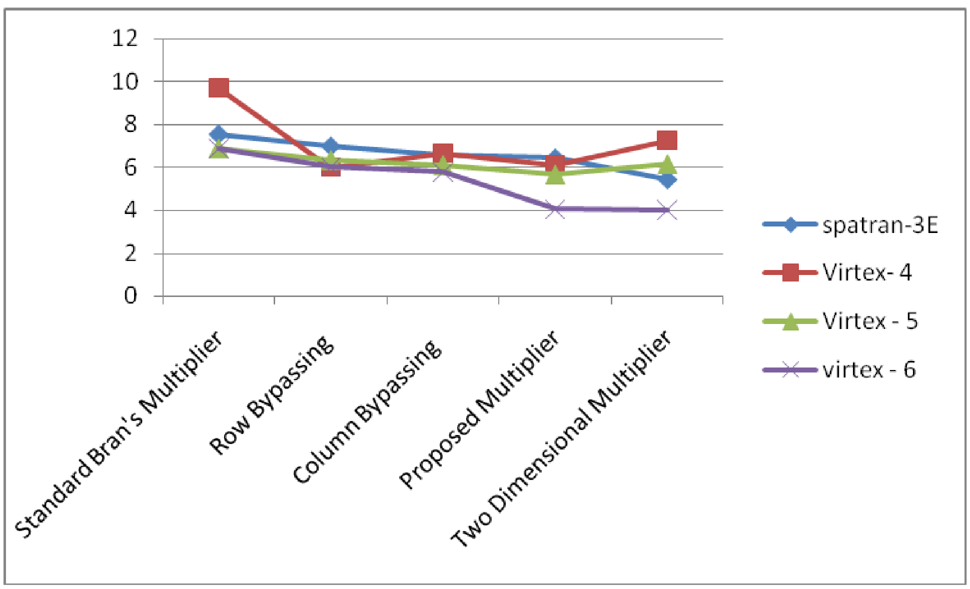

Fig. 12 The average pin delay for Spartan-3AN, Virtex-4, Virtex - 5 and Virtex-6 for standard, row and column bypassing and proposed 4*4 Braun's multipliers

Table 1-4 summarize the FPGA devices resources utilization for standard, row and column bypassing and proposed 4*4 Braun's multipliers

Figure 8 shows the comparison of number of LUTs for Spartan-3E, Virtex-4, Virtex - 5 and Virtex-6 FPGA devices for standard, row and column bypassing and proposed 4*4 Braun's multipliers, which clearly indicates that the virtex-6 FPGA device utilizes fewer resources than Spartan-3E, Virtex-4, and Virtex - 5 devices.

The number of slices and the bonded IOBs are compared in the fig. 9 and fig.10, the figure clearly shows that Virtex 6 has the less percentage of among all the FPGAs.

The table 1 -4 is showing the comparison result of the total combinational path delay of the multipliers and the graph has been plotted as shown in the fig. 11. It shows that Virtex -6 showing the less delay so that speed of the multiplier can increase. And the fig. 12 showing that the average timing delay between the pins which is used in the multipliers.

5.CONCLUSION

In this paper we have presented the hardware implementation of the Multipliers in the FPGA devices using Verilog HDL. The design was implemented on the Xilinx Spartan – 3E (xc3s500e-4ft256), Virtex – 4 (xc4vlx15-10-sf363), Virtex – 5 (xc5vlx30-1-ff324), and Virtex – 6 ((xc6vlx75tl-1L-ff484) FPGAs. The proposed Multiplier shows that reduced utilization when compare to all other multipliers. The average pin delay and combinational path delay has been reduced in the Virtex – 6 Low power FPGA device. So the Virtex – 6 Low power is obtained the best result when compare to the other FPGA devices. And it is feasible for the DSP Processor, Image processing and multimedia technology.

6.FUTURE WORK

Braun Multiplier can be modified using the adder cell, which can be replaced with the Kogge Stone adder/non linear carry select adder can be designed using the RTL complier where we can draw the layout and then validation can also be done.

REFERENCE

[1] Muhammad H. Rais, "Hardware Implementation of Truncated Multipliers Using Spartan-3AN, Virtex-4 and Virtex-5 FPGA Devices", Am. J. Engg. & Applied Sci., 3 (1): 201-206, 2010.

[2] M.A. Ashour*, H.I. Saleh, "An FPGA implementation guide for some different types of serial–parallel multiplier structures", Microelectronics Journal 31 (2000) 161–168.

[3] J. T. Yan and Z. W. Chen, "Low-power multiplier design with row and column bypassing," IEEE International SOC Conference, pp.227-230, 2009.

[4] J. T. Yan and Z. W. Chen," Low-Cost Low- Power Bypassing-Based Multiplier Design,"IEEE 2010.

[5] M. C. Wen, S. J. Wang and Y. M. Lin, "Low power parallel multiplier with column bypassing," IEEE International Symposium on Circuits and Systems, pp.1638-1641, 2005.

[6] Sanjiv Kumar Mangal, Rahul M. Badghare, Raghavendra B. Deshmukh, R. M. Patrikar,"FPGA Implementation of Low Power Parallel Multiplier", 20th International Conference on VLSI Design (VLSID'07) IEEE 2007.

[7] Yin-Tsung Hwang , Jin-Fa Lin , Ming-Hwa Sheu and Chia-Jen Sheu," Low Power Multipliers Using Enhenced Row Bypassing Schemes", IEEE 2007.

[8] Neil H.E.Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design, A circuits and system perspective", Pearson education, 2009.

[9] Kiat – Seng Yeo and Kaushik Roy," Low Voltage, Low Power VLSI Subsystems", TMC 2009 ed.

[10] Lars Wanhannar," DSP Integrated Circuits", Academic Press.

[11] www.xilinx.com

[12] Chen,Kungching, "Types of adders", M. Eng. Project_ 2005.