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Comparative analysis of modified multilevel DC link inverter with conventional cascaded multilevel inverter fed induction motor drive

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Abstract

This paper focuses a new modified multi-level DC link inverter with reduced switches. It presents a comparative analysis of the modified inverter with the existing cascaded H-bridge multilevel inverter (CHBMLI) fed with induction motor drive. The modified multilevel dc link inverter (MLDCL) which is proposed greatly minimizes the switch count as well as the number of gate drivers compare to other family of multilevel inverters. PWM technique which has been applied for proposed inverter and CHBMLI is level shifted multi carrier PWM. An exhaustive survey has taken to investigate the performance characteristics such as total harmonic distortion (THD) and efficiency of various levels of inverter. For the meticulous analysis eleven-level DC link inverter and the existing eleven-level CHBMLI are built using MATLAB/SIMULINK platform. The proposed inverter is observed to have a better performance and relatively less cost compared with the conventional scheme.

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Keywords: Multilevel Dc link inverter,Multi carrier PWM,Full bridge inverter, Induction motor.

1. Introduction

Power electronics becomes a part of our day to day life which indulging in several applications such as residential, industries, aerospace, transportation, and telecommunication also not to be missed out in area of controlling and delivering power to electric grid. In the market of global electricity consumption motor driven systems takes 43% to 46% and most of the industries prefer induction motors as it is reliable and need lesser maintenance. Once upon a time for controlling the speed of a motor mechanical clutches had been used which made the total system failure to gives out favorable efficiency. The devoted power electronics converters which made the system easier to vary the speed parameter and to get ripple free torque output [1].Multilevel inverters (MLI) are

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highly recommended for high power and medium voltage applications nowadays due to the following advantages contrast to two level inverters such as good power quality, electromagnetic compatibility, minimum switching losses, reduced dv/dt stresses, bring down the common mode voltage etc. The advancements in the area of multilevel converters and its contribution towards the diverse industrial applications especially for FACTS and HVDC systems had been reviewed broadly in [2].For grids and micro grids the interfacing of MLI with renewable energy sources is a great demand nowadays, by selecting optimum topology and control method gives improved power quality, total harmonic distortion (THD) and efficiency had been experimented and studied in [3-5].The selection of pulse width modulation(PWM) control scheme have great effect on harmonic eradication in output voltage with less switching losses had been reviewed with various MLI topologies in [6-8].

The advent of new class of multilevel dc link inverter is provided with less number of power electronic switches as well as gate drivers compared to other types of MLI such as cascaded, diode clamped and flying capacitor which are very much advantageous when the levels has been increased [9-11].In this dc sources can be separately given by any renewable energy sources to each phase leg as in cascaded type inverters. The problem with cascaded inverter is switches, which count increases with levels that can be overtaken by the use of multilevel dc link inverter [12-13]. The multilevel dc link inverter significantly increases the induction motor efficiency by eliminating the ripples in torque and also simultaneously reduces iron and copper losses along with it in motor [14-15]. In this paper level shifted multi carrier PWM has been used for the switches of proposed multilevel dc link side which is fed with single phase full bridge inverter which flips the obtained voltage from MLDCL to give desired staircase ac voltage output. The comparative analysis had been taken between the proposed multilevel dc-link inverter and the existing cascaded H-bridge inverter finally the performance of induction motor drive is validated. These configurations are built and verified using MATLAB/Simulink platform.

2. Operation of cascaded multilevel inverter and modified dc link inverter fed induction motor drive:

2.1. Three-phase eleven level cascaded inverter fed induction motor drive:

The cascaded multilevel inverters are free from clamping diodes and capacitors in topology as compared to other types. This advantage makes the structure to extend for higher levels so as to decrease the THD and to get the nearly sinusoidal wave pattern.

Fig.1 shows the three-phase eleven-level cascaded H-bridge inverter fed induction motor drive. In this topology each one of the full bridge inverter in a phase leg tends to provide three output voltages they are +Vdc, 0 and -Vdc from the fusion of four switches Sa1, Sa2, Sa3 and Sa4. Sa1 and Sa4 turns on to obtain +Vdc, in the case of -Vdc voltage, Sa2 and Sa3 should switch on. When the entire switches of a full bridge gets turned on the concerned output voltage will reaches 0. Then they obtained output phase voltage levels are calculated based on the formula m=2N+1, where “N” is the number of dc sources and “m” gives number of levels. Hence for three- phase eleven-level cascaded H-bridge inverter fed induction motor drive five dc sources had been taken to get desired eleven-level staircase output voltage waveform.

The gate signals required for the power semiconductor switches are attained by using level shifted multi carrier modulation technique. In this carrier signal is triangular wave and modulating signal is sine wave it should be 120^0 apart to give balanced three phase output voltage for driving the induction motor. Eleven-level inverter needs ten triangular carrier waves where five of them are given to the positive half cycle of modulating signal and another five are applied across negative half cycle of the modulating signal. It results to give twenty PWM signals, which applied to twenty switches of a leg. Likewise the gate pulses are provided for other two legs consequently final output voltage will be generated which is nearly sinusoidal that have a tendency to drive the dedicated three phase induction motor. Also the modulating signal frequency which decides the inverter output voltage frequency simultaneously controls the speed of the induction motor.

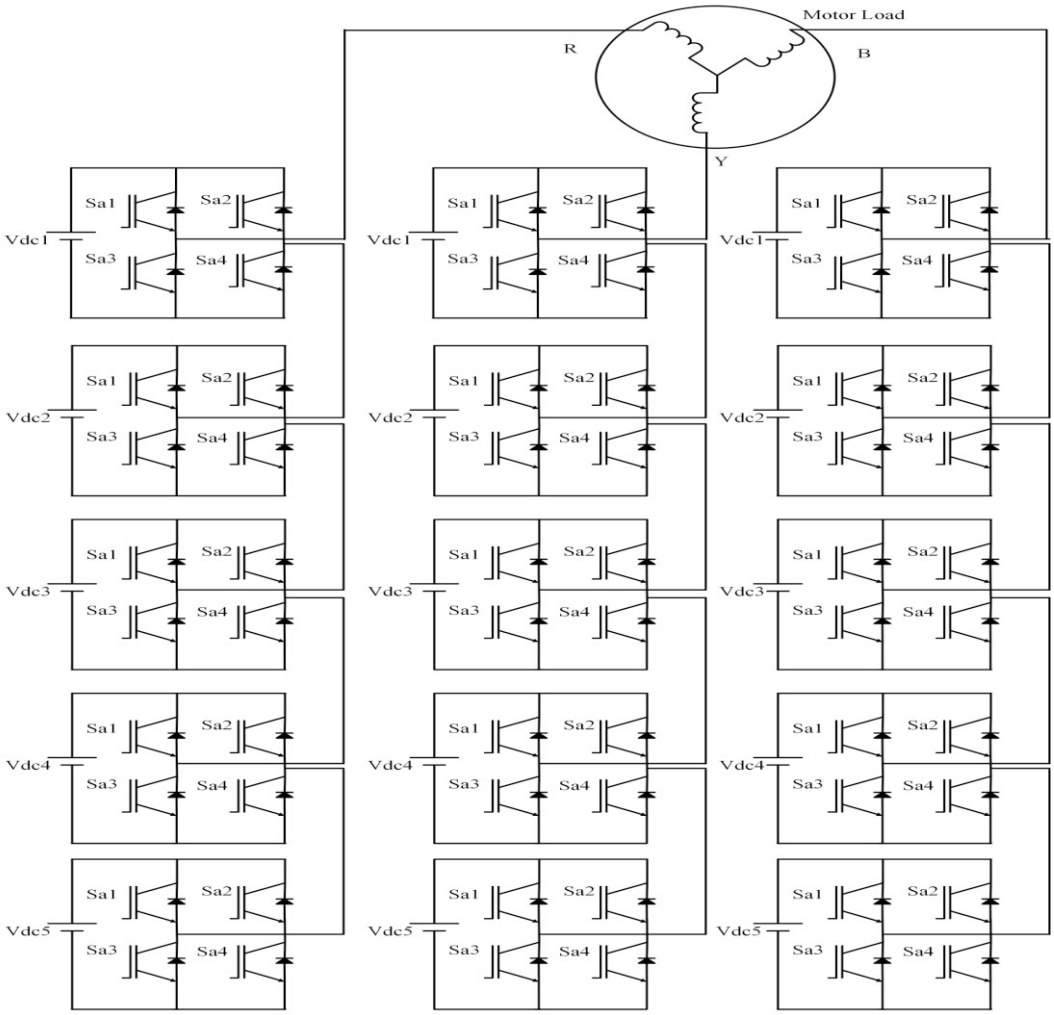


Fig.1. Three-phase eleven level cascaded inverter fed induction motor drive

2.2 Three-phase eleven level modified DC link inverter fed induction motor:

The eleven-level DC link inverter with reduced switching devices based on a capacitor-clamped phase leg is shown in Fig.2 .Each phase of a leg comprises ten switches from S1 to S10 and four clamping capacitors C1, C2, C3 and C4.A dc-bus voltage of five voltage levels, 0, 1/5 V_{dc}, 2/5 V_{dc},3/5V_{dc} ,4/5V_{dc} and V_{dc}, by turning on the switches according to the voltage level as listed in Table 1. By controlling the duration of the switching combinations, the voltage across capacitors could be maintained at the required levels. Here also the gate signals for power switches are generated by level shifted multi carrier modulation technique .The single phase full bridge inverter (SPFB) flips the dc-bus voltage polarity to give an eleven level ac voltage. Table.2 describes the switches requirement, gate drivers, clamping diodes and capacitors needed for the proposed inverter and compared with its existing counterpart for a given number of output voltage levels where ‘m’ refers to the number of levels. Now it is very clear that in this configuration when inverter voltage levels increases to higher levels almost half the number of the components can be eliminated along with it.

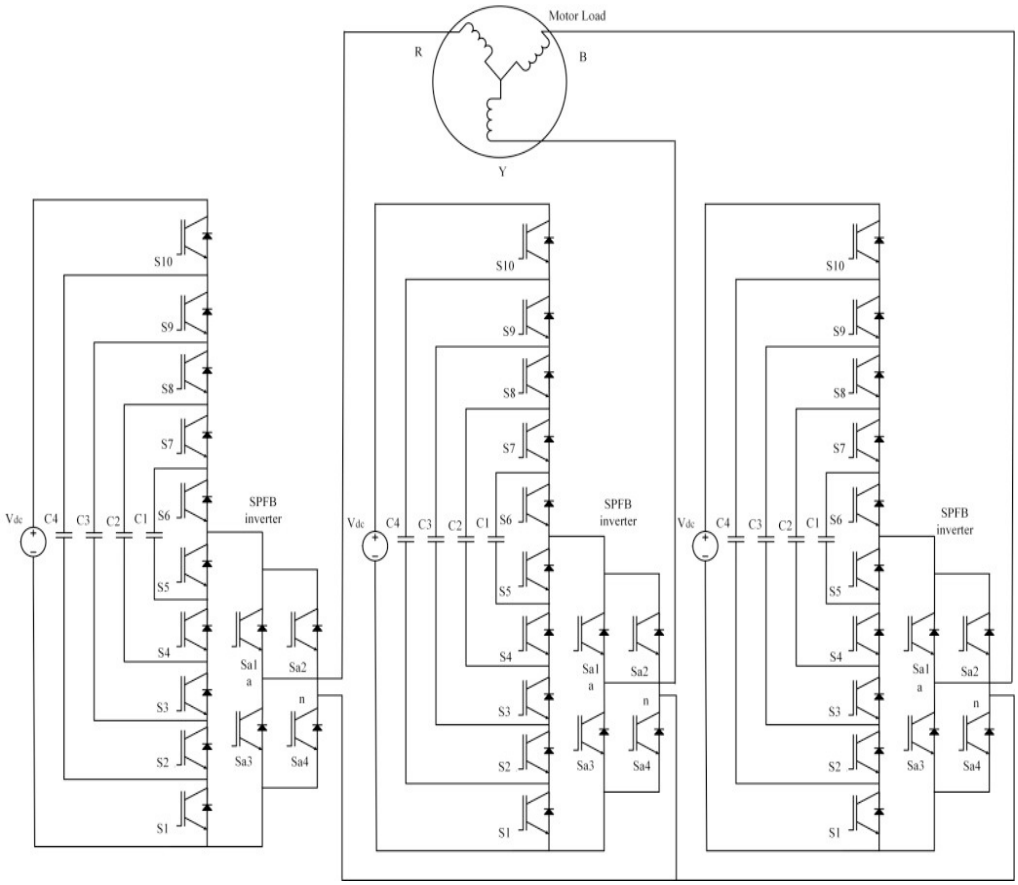


Fig.2 Eleven level DC link inverter fed induction motor drive with reduced switches

Table 1. Switching states of eleven level DC link fed induction motor

Vbus	Switches to be turned on	Charge/discharge Capacitors
0	S1,S2,S3,S4,S5	No
1/5 Vdc	S4,S3,S7	Discharge C1
	S7,S5,S3	Charge C1 and Discharge C2 Discharge C2
2/5Vdc	S7,S6,S3	Discharge C3
3/5 Vdc	S8,S7,S2 S9,S10,S3	Charge C3
4/5 Vdc	S1,S8,S9	Discharge C4
Vdc	S6,S7,S8,S9,S1,0	No

Table 2. Component count comparison

	Proposed MLDCLI	Cascaded MLI
Switches	m+3	2(m-1)
Gate Drivers	m+3	2(m-1)
Clamping Capacitors	(m-3)/2	-

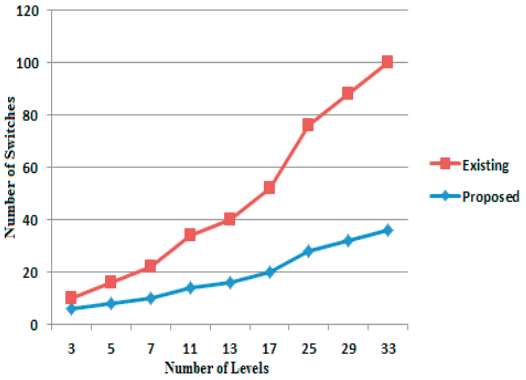


Fig.3.Comparison of switches for existing and proposed inverter

3. SIMULATION RESULTS AND DISCUSSION:

The simulation of eleven level CHBMLI and MLDCL fed induction motor drives is scrutinized and the results were presented. Level shifted multicarrier PWM is applied to both the configurations. The switching pattern for both of the topology power switches is given in Fig.4.a and b where firing pulses are generated with fundamental switching frequency. Similarly the three phase eleven level output voltage after fed to induction motor of CHBMLI is shown in Fig.5.For MLDCL initially dc link voltage 400 V is fed to single phase full bridge inverter which flips the voltage at the output is shown in Fig. 5. b.

The stator currents of induction motor for both structures are shown in Fig.6.a and b. The variation in torque of CHBMLI is shown in Fig.7a, at a time period of 1 sec it settles and the value of torque is 20 Nm.With respect to it the rotor speed increases and settles to1463 rpm at the same period, it is shown in Fig.8 a. In the same way variation in torque of three phase eleven level DC link fed induction motor is shown in Fig 7.b The rotor speed of MLDCL inverter which settles at 1482 rpm is shown in Fig.8b.The harmonic spectrum is shown in Fig. 9 a and b for both the methods. It is observed that THD result for the eleven-level CHBMLI is 13.08% and for the DC link inverter with eleven levels is 10.92% where the modulation index is 0.8.

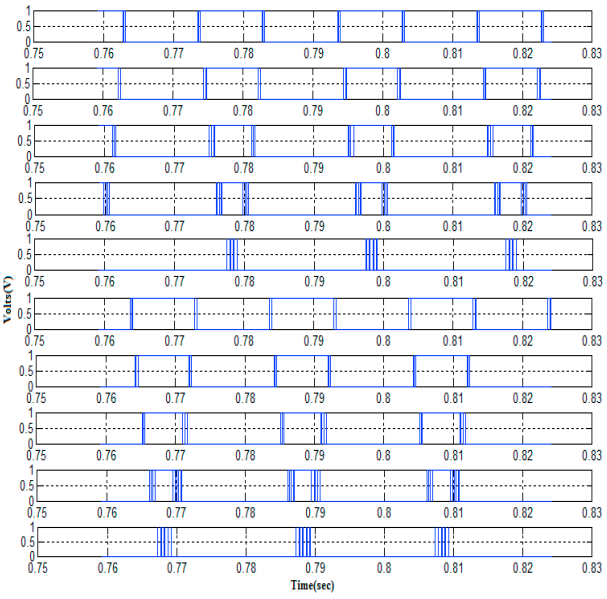
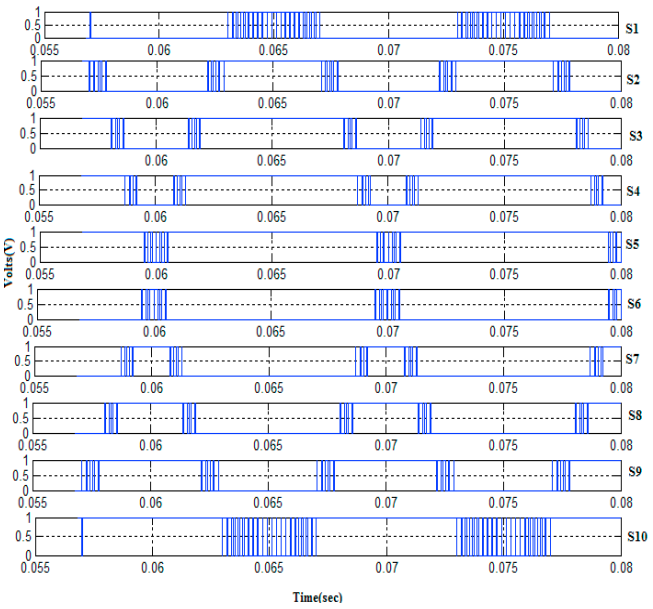
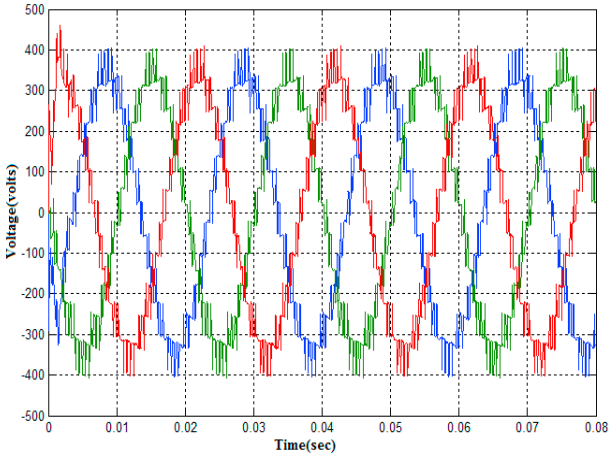


Fig.4.a) Simulated Firing Pulses for eleven level Cascaded inverter



b) Switching pattern for eleven level Dc link inverter



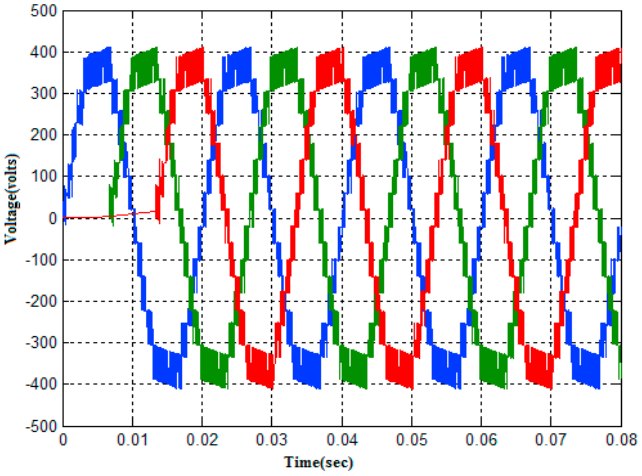
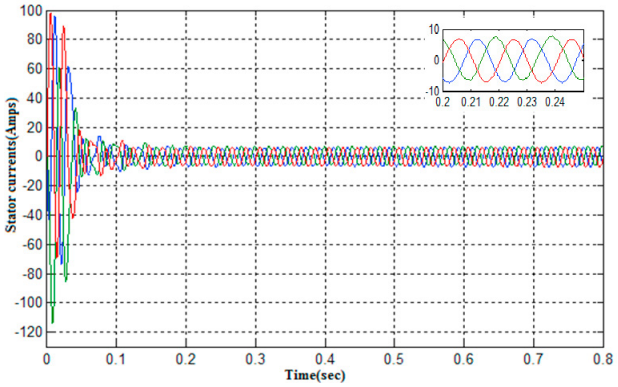


Fig.5. a) Three phase eleven-level CHB-MLI phase voltage b) Three phase eleven level DC link inverter phase voltage



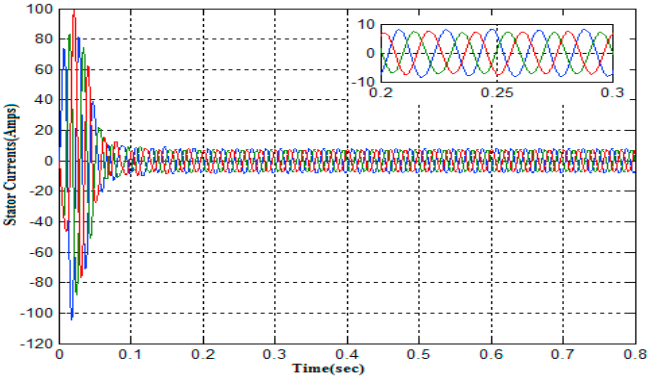
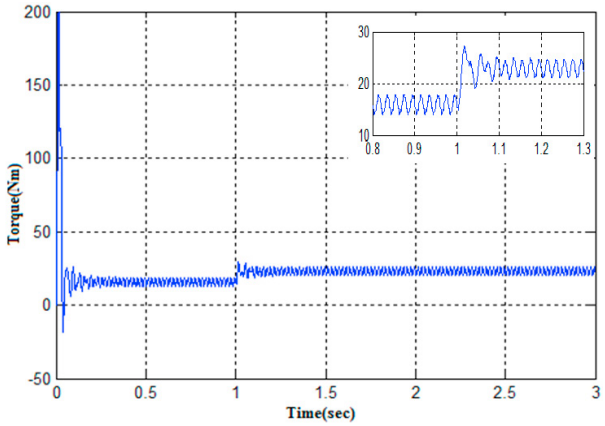


Fig.6.a) Stator currents of three phase eleven-level CHB-MLI phase voltage b) Stator currents of three phase eleven level DC link inverter



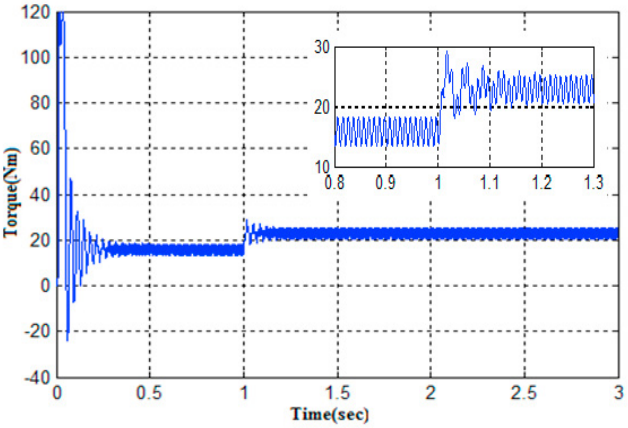


Fig.7.a) Variation in torque of 11-level cascaded fed induction motor drive b) Variation in Torque of three phase eleven level DC link inverter

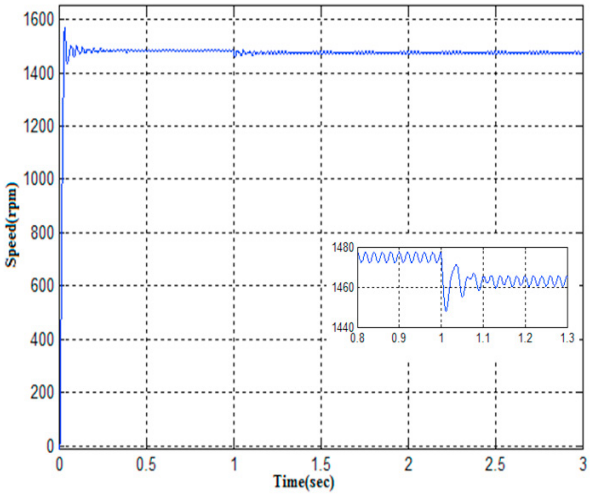
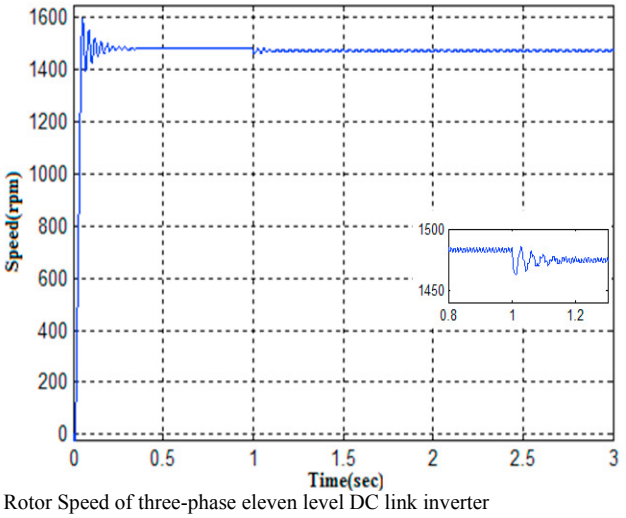
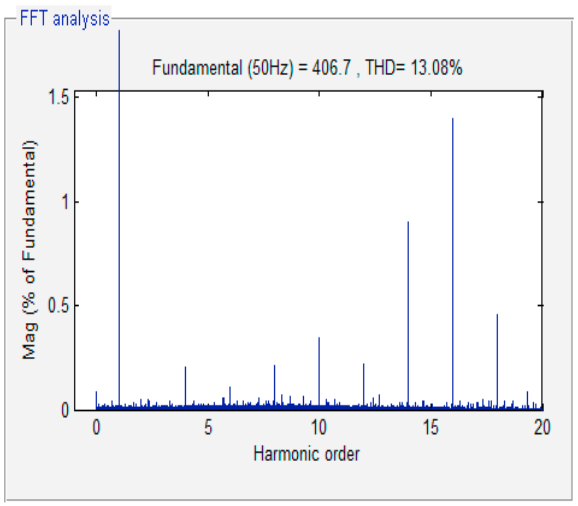


Fig.8.a) Rotor speed of eleven level CHBMLI fed induction motor



b) Rotor Speed of three-phase eleven level DC link inverter



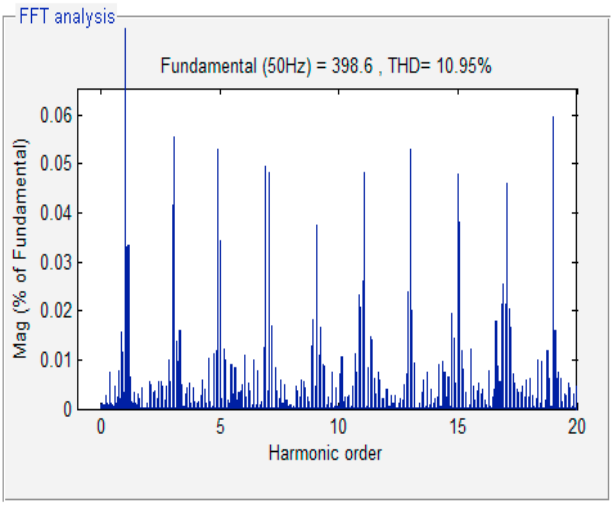


Fig.9.a) THD spectrum of 11-level CHBMLI fed induction motor drive b) THD spectrum of eleven level DC link inverter fed induction motor

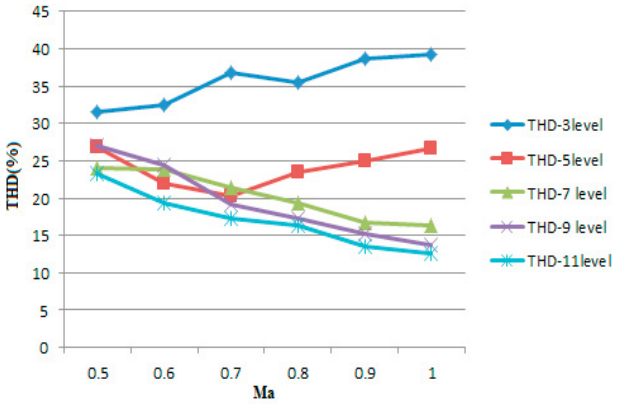


Fig.10 THD Vs Ma of 3, 5, 7, 9 and 11 level Inverter

The Fig.10 shows THD Vs modulation index (Ma) of 3, 5, 7, 9 and 11 level inverters where we can clearly observe that the harmonics are reduced greatly when increasing the number of levels of multilevel inverter. The below Table.3shows the efficiency of the multilevel DC link inverter fed induction motor is comparatively higher than CHBMLI.It can be seen that the modified inverter is superior to the existing multilevel inverter. Both the schemes are analyzed with different number of voltage levels 'm'.

Table.3 Efficiency Analysis

Various level of MLI fed to induction motor drive	Efficiency of CHBMLI	Efficiency of multi-level DC link inverter
Eleven level inverter	84.55	87.53
Nine level inverter	76.62	79.4
Seven level inverter	74.02	76.5
Five level inverter	71.44	73.2
Three level inverter	65.29	67.18

4. Conclusion:

The proposed MLDCL inverter and the conventional CHBMLI schemes are analyzed through simulation. It is observed that the Multilevel DC link inverter can eliminate roughly one third number of switches and gate drivers compared with conventional CHBMLI. This reduces the cost of the system which also leads to smaller size and volume. With proposed multilevel DC link inverter the quality of the output voltage is improved. The THD of the proposed MLI is less than the cascaded MLI for the same voltage level which serves as a better option for induction motor drives.

Appendix

Table.4
Parameters of three-phase squirrel cage induction motor drive

Rotor type	Squirrel-cage
Voltage(line-line)	415Vrms
Frequency	50Hz
Stator resistance	1.115(ohm)
Stator inductance	0.005974(H)
Rotor resistance	1.083(ohm)
Rotor inductance	0.005974(H)
Mutual inductance	0.2037(H)
Inertia	0.02J(kg.m^2)
Friction factor and pairs of poles	0.005752&2F(N.m.s)

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