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V. Raghavendra Rajan[1] / L. Premalatha[1]

Comparative Analysis of Symmetrical/Asymmetrical Quasi Z-Source Cascaded Multilevel Inverter with Alternative Phase Opposition Disposition Technique

[1] School of Electrical Engineering, Vellore Institute of Technology, Chennai Campus, Chennai 600127, India, E-mail: vraghavendra.rajan2015@vit.ac.in, premalatha.l@vit.ac.in. https://orcid.org/0000-0003-2577-6254.

Abstract:
This paper presents a detailed comparative analysis between Symmetrical and Asymmetrical Quasi Z-Source Cascaded Multilevel Inverter (QZS-CMI). The comparative analysis investigates for boost operation in both Symmetrical and Asymmetrical System. Analysis is done based on the achieved input current, capacitor voltage of the upper capacitor and parallel capacitor and the two inductors current of DC link (Quasi Z-Source network) which is combined with H-bridge. In Asymmetrical QZS-CMI, the input voltage for three DC sources are given in the ratio of 1:3:9, i. e. the system is designed for 27 level. Asymmetrical QZS-CMI is new system and proposed in this paper for comparative analysis with Symmetrical QZS-CMI. An advanced optimal Alternative Phase Opposition Disposition (APOD) technique is developed and implemented. Symmetrical system has high boosting capability of output voltage, reducing the switching losses, high voltage gain and lower spikes in switching voltage. The comparative study is done and results are verified with Experimental 250 W prototype model and also verified by using MATLAB/ Simulink.

Keywords: Symmetrical QZS-CMI, Asymmetrical QZS-CMI, APOD

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1 Introduction

Cascaded Multilevel Inverter combined with Quasi Z-Source has become an important feature for the next generation of Power Converters [1]. Recent research works have been used have mitigated the disadvantages which were been in the previous methods [2, 3]. One of the most efficient solutions is the use of the Quasi Z-Source concept. The reason behind choosing Quasi Z-Source in combination with Cascaded Multilevel Inverter to can maintain constant current in both input and output, Total Harmonic Distortion (THD) can be reduced [4–8]. The Quasi Z-Source inverter has become more popular due to its handling capability in single phase by DC sources. The choice of appropriate value of a capacitor switching stress can be reduced [9], constant capacitor voltage is maintained for avoiding the overlap of Duty cycle (D) and Modulation Index (M) which is not possible in a conventional Z-Source inverter, where the inductor value can also effectively reduce the inductor current peak in the utilization of separate DC link modules voltage can be controlled independently. QZSI has high reliability as it reinforces the shoot-through states easily and can save a third of the module, which is major advantage when compared to the traditional CMI.QZS-CMI maintains constant DC-link peak voltage control for balancing the system [10–13]. The main aim of proposing a comparative analysis through the use of the Symmetrical and Asymmetrical is to know the system performance in terms of voltage gain and its boosting capabilities in the output voltage. However, the use of conventional Cascaded Multilevel Inverter in Symmetrical and Asymmetrical systems does not provide any boost to the output voltage. QZS-CMI provides many advantages including its high quality staircase output voltage with lower harmonic distortions. It has capability to reduce output filter requirements to meet the harmonic standards, with the requirement of power semiconductor devices with low rating. It has an independent dc-link voltage for buck and boost operation, which allows an independent control of power with high reliability [10, 12, 14–16]. Alternative Phase Opposition Disposition technique (APOD) has been applied for QZS-CMI due to its less complexity in generating pulse for switches. APOD pulses are generated for comparison between the phase reference and the carrier

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L. Premalatha is the corresponding author.

reference i. e. a comparison of modulation signal (N−1)/2 triangular carriers independently. The amplitude of the modulation signal (Am) is modified based on inverter level, therefore Am = (N−1) M .Ac/2. The DC off-set difference between carriers is 2Ac [17]. The categorization of this paper is organized as follows: Section 2 provides a brief explanation of Symmetrical QZS-CMI; Section 3 deals with Asymmetrical QZS-CMI; Section 4 provides a discussion relating to the Advanced APOD technique with reduction in switching losses; verification of simulation results is done in Section 5 and Section 6 provides the conclusion.

2 Symmetrical Quasi Z-source Cascaded Multilevel Inverter

Symmetrical Quasi Z-Source Cascaded Multilevel Inverter (QZS-CMI) shown in Figure 1 has equal voltages and operates both in shoot-through and non-shoot through states. In the non-shoot through state it operates as conventional H-Bridge, but in the shoot-through it does not obtain any AC output voltage due to its stepping output as multilevel waveform. Each module (H-Bridge) of QZS-CMI has shoot-through and non-shoot through states. In the shoot through state, the diode D1, D2, D3 does not conduct due to negative voltage.

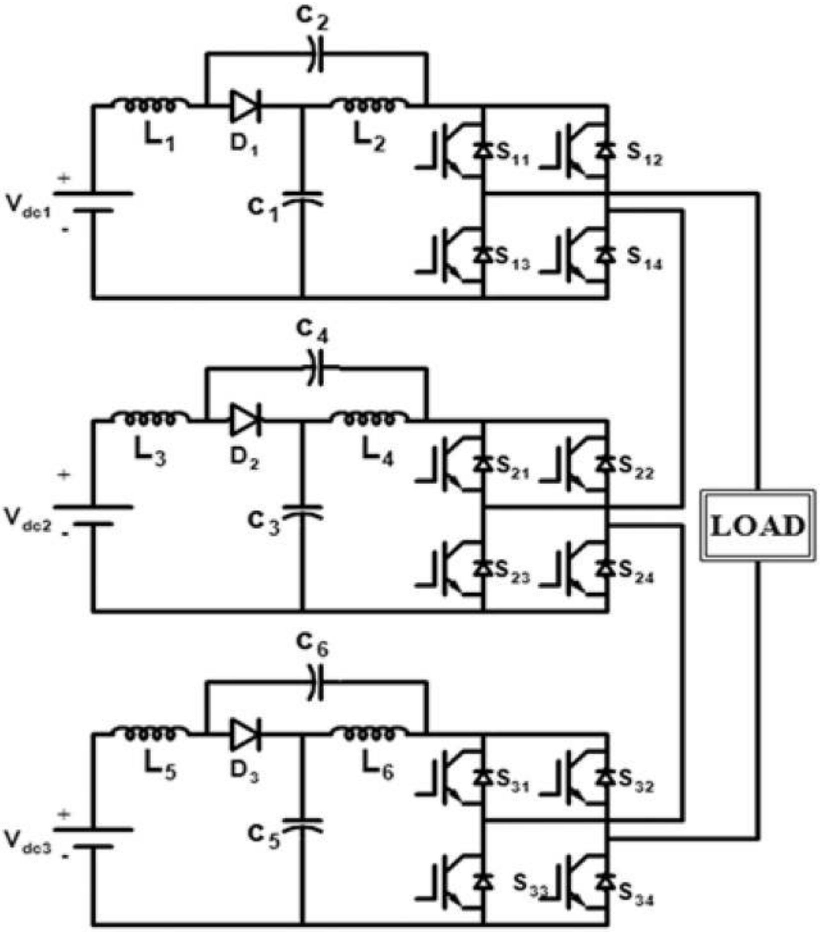

Figure 1: Circuit diagram of Symmetrical QZS-CMI.

As Quasi Z-Source Inverter in QZS-CMI it will operate in both shoot-through and non-shoot through states, In non-shoot through the state it will operate as conventional H-Bridge, but in shoot-through it will not obtain any AC output voltage because it will step as Multilevel waveform. Each module (H-Bridge) of QZS-CMI will have shoot-through and non-shoot through states. In shoot through the state the diode D1, D2, D3 will not conduct because of negative voltage which is shown in Figure 2.

$$V_{l1} = V_{dc1} + V_{c2},\ V_{l2} = V_{c1},\ V_{dc} = 0,$$

Diode Voltage, $V_{d1} = V_{c1} + V_{c2},\ I_{d1} = 0,$

$$I_{c1} = -I_{l2},\ I_{c2} = -I_{l1},\ I_{dc} = I_{l1} + I_{l2} \tag{1}$$

In non-shoot through state the capacitor and load will get charged by inductors, therefore diode will start conducting as shown in Figure 3.

$$V_{l1} = V_{dc1} - V_{c1},\ V_{l2} = -V_{c2},\ V_{dc} = V_{c1} + V_{c2},$$

Diode Voltage, $V_{d1} = 0$

$$I_{d1} = I_{l1} + I_{l2} - I_{dc},\ I_{c1} = I_{l1} - I_{dc}, I_{c2} = I_{l2} - I_{dc} \tag{2}$$

In Symmetrical system the upper capacitor will achieve low voltage for two H-Bridge's and the middle H-Bridge has very high voltage to achieve the voltage gain. The upper capacitors are used because to avoid spikes which will occur in switches. The parallel capacitor of all three H-Bridge's will produce a nominal voltage for voltage gain.

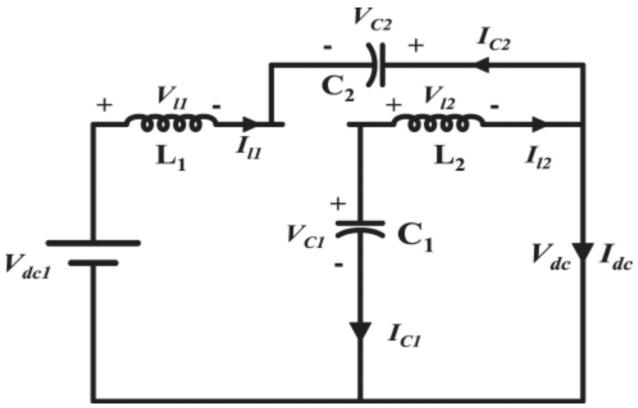

Figure 2: Shoot-through state operation of QZS-CMI.

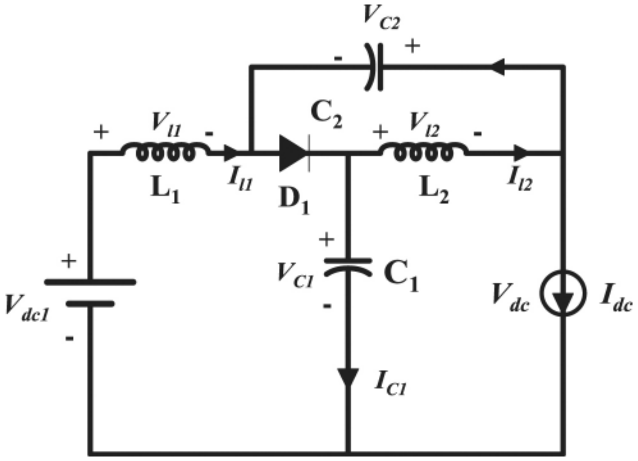

Figure 3: Non-shoot through operation state of QZS-CMI.

3 Asymmetrical Quasi Z- source Cascaded Multilevel Inverter

In Asymmetric QZS-CMI the input voltages are V_{dc1}, V_{dc2}, and V_{dc3} are in the ratio of 1:3:9.

Symmetrical QZS-CMI and Asymmetrical QZS-CMI operate in both shoot through and non-shoot through states, but there are variations in the boosting capabilities of Asymmetric when compared to these of the Symmetrical system, Asymmetrical system is shown in Figure 4. Figure 5 shows the relation between Modulation Index vs Voltage Gain. Modulation index has a voltage gain of 40 at 0.865

$$G = 35M/\ (40M - 30) \tag{3}$$

The above equation is derived from the previous equations in Ahmed et al. [18]. Figure 5 shows the relation between Modulation Index vs Voltage Gain. Modulation index has a voltage gain of 40 at 0.865.

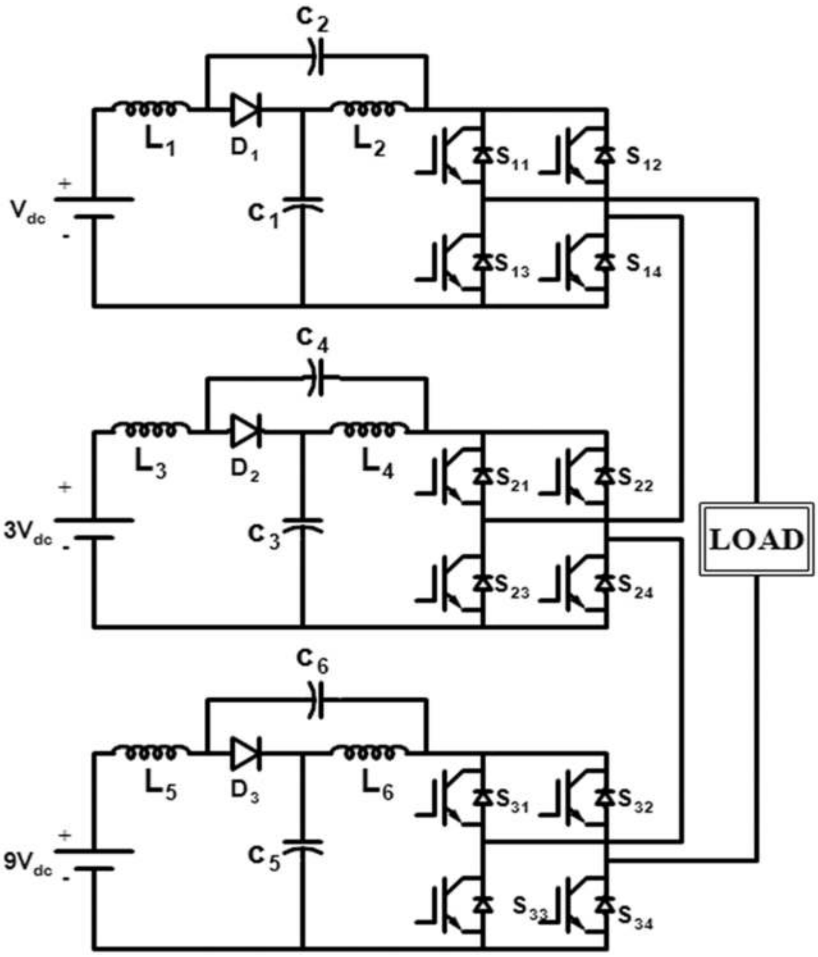

Figure 4: Circuit diagram of Asymmetrical QZS-CMI.

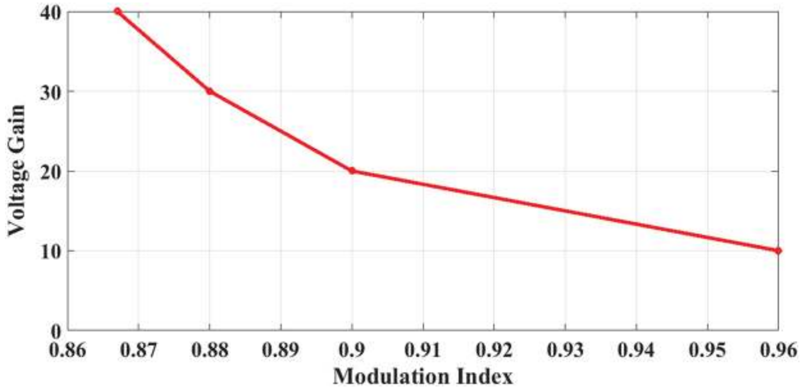

Figure 5: Modulation index vs. voltage gain.

4 Advanced APOD-PWM for QZS-CMI

Advanced APOD technique is most preferred for the generation of pulses for a large number of switches. It involves the use of the APOD technique for QZS-CMI and enables reduction in the complexity in switching action. In this system a four carrier wave of 10 kHz frequency is compared with sine wave (reference signal) of 50 Hz frequency. The gate pulse generated triggers the switches S_{11} to S_{34} as shown in Figure 6, for APOD all carriers which are in phase opposition by 180° from its adjacent carriers. In addition, the use of APOD technique helps reduction in THD. This technique plays a major role in obtaining the optimized stepped multilevel waveform. Modulation index of maximum 0.95 can be obtained and maximum Voltage gain can be obtained in the Quasi Z-Source network of QZS-CMI.

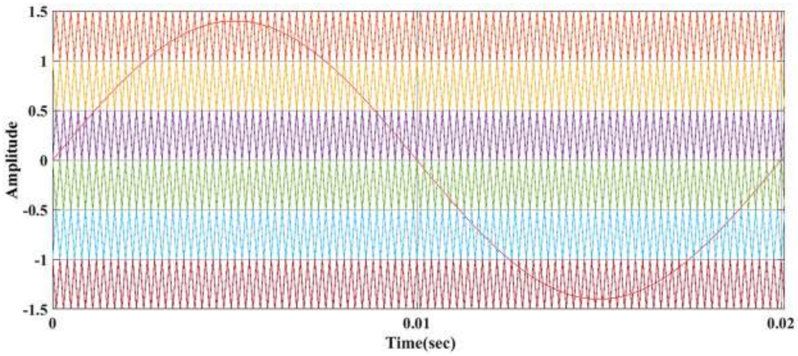

Figure 6: APOD-PWM Technique

This technique is most preferred for the generation of pulses for a large number of switches. It involves the use of the APOD technique for QZS-CMI and enables a reduction in the complexity in switching action. In this system, a four-carrier wave of 10 kHz frequency is compared with a sine wave (reference signal) of 50 Hz frequency. The gate pulse generated triggers the switches S11 to S34 as shown in Figure 6, for APOD all carriers which are in phase opposition by 180° from its adjacent carriers. In addition, the use of APOD technique helps reduction in THD.

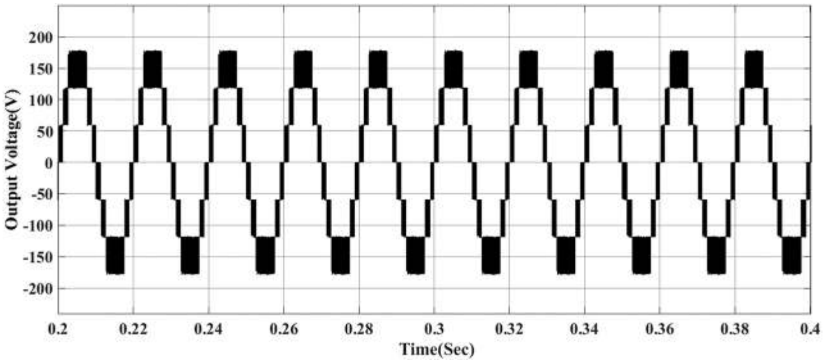

Figure 7: Output voltage of Symmetrical QZS-CMI

This technique plays a major role in obtaining the optimized stepped multilevel waveform. APOD modulator scheme is used for switching purpose for the H-Bridge in multilevel inverter, the switching sequence of APOD Govindaraju et al. [19] for any H-Bridge will be as follows;

$$S_{11} = ABC^{'} + \overline{A}B$$

$$S_{12} = \overline{A}BC^{'} + \overline{A}\,\overline{B}$$

$$S_{13} = \overline{A}\,\overline{B}C^{'} + A\overline{B}$$

$$S_{14} = \overline{A}BC^{'} + AB \tag{4}$$

5 Simulation results

Symmetrical and Asymmetrical QZS-CMI systems were simulated for comparative analysis. Advanced APOD-PWM technique was used in both the systems with low amplitude voltage. The parameters of both systems have been considered using the details provided in the previous selection. The capacitor voltage of each QZS network is shown in Table 1 and Table 2. The output voltage for Symmetrical QZS-CMI and Asymmetrical QZS-CMI is shown in Figure 7 and Figure 8 where the output voltage for Symmetrical system is 180V and the output voltage for Asymmetrical system is 175V. THD Analysis of Symmetrical QZS-CMI is shown in Figure 9 and Asymmetrical QZS-CMI is shown in Figure 10. Table 3 shows the values of the parameters used in Symmetrical and Asymmetrical QZSI-CMI.

Table 1: Input current and capacitor voltages of Symmetrical QZS-CMLI.

S.No	Input Voltage	Input Current	Capacitor Voltage (Upper)	Capacitor Voltage (Parallel)
1	30 V	2.85 A	2.7 V	50.5 V
2	30 V	1.75 A	30.2 V	75.4 V
3	30 V	2.65 A	2.5 V	48.5 V

Table 2: Input current and capacitor voltages of Asymmetrical QZS-CMLI.

S.No	Input Voltage	Input Current	Capacitor Voltage (Upper)	Capacitor Voltage (Parallel)
1	10 V	1.85 A	14.6 V	37.5 V
2	30 V	3.50 A	6.5 V	58.6 V
3	90 V	6.85 A	6.5 V	92.7 V

Table 3: Parameters used in simulation.

Parameter	Value
Capacitor (C_1,C_3, C_5)	4400 μF
Capacitor (C_2,C_4, C_6)	4400 μF
Inductor (L_1,L_3, L_5)	500 μH
Inductor (L_2,L_4, L_6)	500 μH
Switching Frequency	10 kHz
Filter Inductance	100 mH
Rated Power	250 W

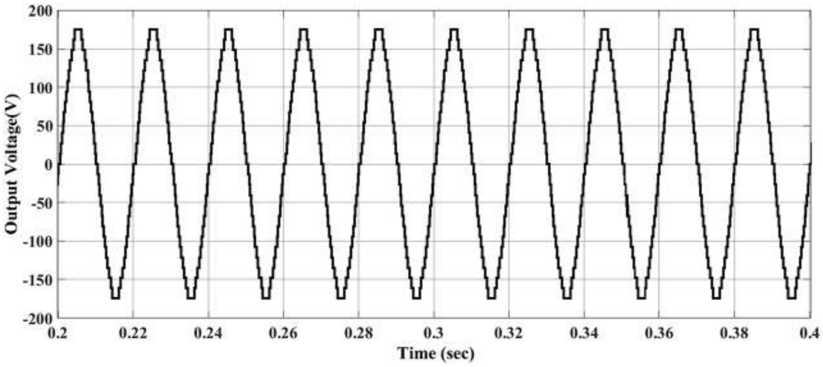

Figure 8: Output voltage of Asymmetrical QZS-CMI.

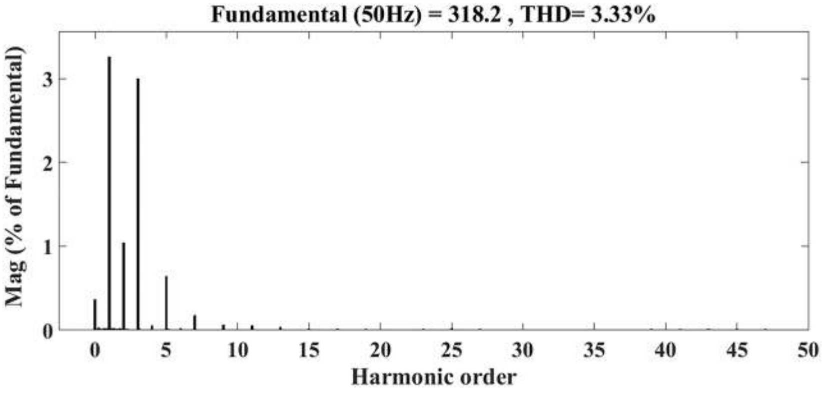

Figure 9: THD analysis of Symmetrical QZS-CMI.

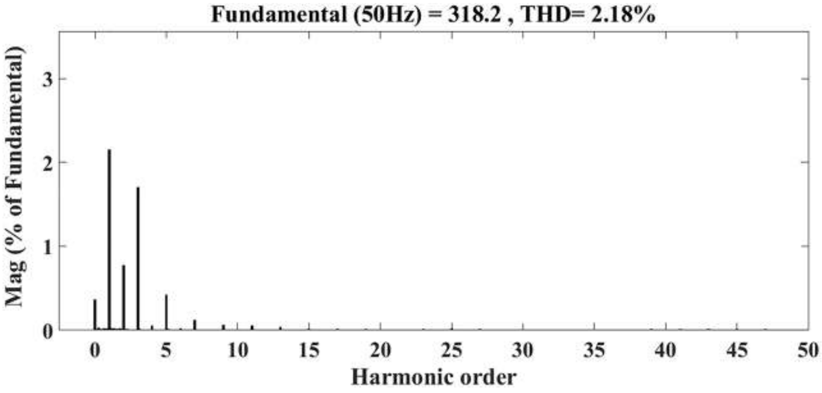

Figure 10: THD analysis of Asymmetrical QZS-CMI.

In comparison, Asymmetrical QZS-CMI has low THD due to increase in level, verification in Simulation Analysis for both Symmetrical system and Asymmetrical system is done with results. A comparison between both the systems, Symmetrical system is been having exclusive benefits such as high voltage gain, less switching stress, higher modulation index and less spikes in the switching voltage and output voltage whereas in Asymmetrical only THD is reduced due to its level increment in the output voltage. As per the efficiency calculation in Figure 11 plotted a graph for Efficiency (%) vs Power (In Watts). Symmetrical QZS-CMI has 92.76 % and Asymmetrical QZS-CMI is with 91.23 %.

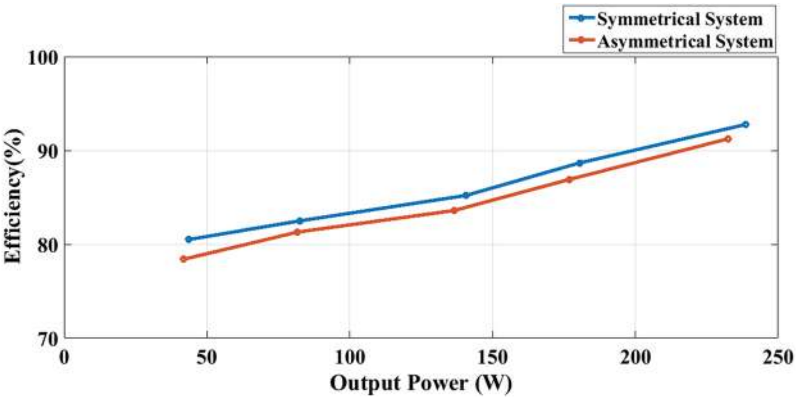

Figure 11: Efficiency calculation of Symmetrical QZS-CMI and Asymmetrical QZS-CMI.

6 Conclusion

Quasi Z-Source Cascaded Multilevel Inverter (QZS-CMI) is a high reliability inverter due to its high voltage gain by voltage boosting abilities is improved. This paper has proposed a new comparative analysis of Symmetrical input voltage and Asymmetrical input voltages. A new advanced APOD PWM has been designed with less amplitude voltage, for a comparative it involves a reduction in switching losses. The Asymmetrical system has been characterized by providing the input voltages in the ratio of 1:3:9. Moreover, the comparative analysis for the Symmetrical system has more advantages through consideration of the parameters capacitor voltages of upper, parallel and inductor current also. The output voltage is boosted approximately twice but in the case of Asymmetrical system the output voltage is boosted approximately 1.3 times.

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