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Comparative electrical bistable characteristics of ferroelectric poly(vinylidene fluoride-trifluoroethylene) copolymer based nonvolatile memory device architectures

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We report the thermal and electrical bistable characteristics of ferroelectric poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE) (72/28 mol %)] thin films as a function of varying memory device architectures. Rectangular-shaped capacitance-voltage (C-V) hysteresis loops obtained using 100 nm P(VDF-TrFE) films with a metal-ferroelectric-insulator-semiconductor (MFIS) diode architecture were more suitable for distinguishing the data-bit state compared with the symmetrical hysteresis observed using metal-ferroelectric-metal capacitors. Poly(4-vinyl phenol) used as a dielectric insulator in the MFIS prevented shifting of the C-V hysteresis curve toward the negative bias voltage. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3013835]

In recent times, the copolymers of poly(vinylidene fluoride-trifluoroethylene) (PVDF-TrFE) with VDF mole ratio between 50% and 80% have been widely studied for use in nonvolatile random access memory (NvRAM) devices.[1–5] Many researchers have used simple device architectures such as metal-ferroelectric-metal (MFM) capacitors,[6–8] metal-ferroelectric-insulator-semiconductor (MFIS) diodes,[7,9–13] and comparatively advanced ferroelectric field effect transistor (FeFET) architectures[9,12–15] to study their response to an applied external electric field. Our recent studies using P(VDF-TrFE) (72/28 mol %) copolymer thin films reported a significant increase in the degree of crystallinity for samples annealed in their Curie temperature (T_C) range (110–120 °C),[5] and drastically reduced the degree of crystallinity for spun-cast films below their threshold crystallization thickness (<130 nm).[16] However, some key factors that affect the dipole switching and memory retention capability of the spun-cast thin films still remain to be resolved. In this letter, the dependence of the ferroelectric response, which is closely related to the changes in dipole and chain orientation of the P(VDF-TrFE) copolymer during a heating-cooling cycle as a function of sample preparation methods (as cast and thermally annealed), is analyzed. From the comparative electrical hysteresis loops observed using MFM and MFIS structures, a suitable memory device architecture for identifying the on and off states is suggested.

P(VDF-TrFE) (72/28 mol %) samples (Solvay, Korea, herein referred to as VDF 72% copolymer) dissolved in methyl ethyl ketone solvent were spun cast (1500 rpm/30 s) over varying substrates such as indium tin oxide or gold-coated slide glass (for the MFM), SiO_2/n^{++}-Si (for the MFIS using a SiO_2 layer as insulator) and p^{++}-Si (for the FeFET) under an inert atmosphere at ambient temperature conditions (herein referred to as as-cast samples). The as-cast samples were thermally annealed (herein referred to as annealed samples) at 110 °C under vacuum for 3 h to improve their degree of crystallinity and thermodynamic stability. Au layers as top electrodes were formed over the films using a vacuum evaporation system (~10^{-6} torr) equipped with a shadow mask.

We also fabricated a gold (M)/P(VDF-TrFE) (F)/insulator (I)/p^{++}-Si (S) structure. Poly(4-vinylphenol) (PVP), poly(melamine-co-formaldehyde) (PMF) (used as the PVP thermal cross-linker), poly(vinyl alcohol) (PVA), and ammonium dichromate (ADC) (used as PVA cross-linker under UV irradiation) purchased from Sigma-Aldrich were used as insulators in two different combinations: PVP/PMF in hexanol and aqueous PVA/ADC. The average thickness of the spun-cast films was measured using an Alpha-step 500 surface profiler (Tencor Instruments).

Figures 1(a)-(i) and 1(a)(ii) show the Fourier transform infrared-grazing incidence reflection absorption spectra (FTIR-GIRAS, Bruker-IFS66V) for 100 nm thick VDF 72%

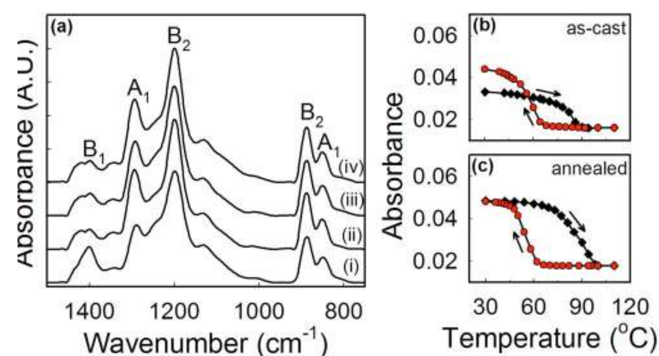

FIG. 1. (Color online) (a) FTIR-GIRAS spectra of VDF 72% copolymer thin films spun cast on Au substrate as a function of varying conditions: (i) as-cast, (ii) annealed at 110 °C, (iii) as-cast sample at 30 °C after cooling from heating-cooling study, and (iv) annealed sample with similar thermal history used for (iii) sample. The intensity of each spectrum was rescaled for clarity. GIRAS absorbance changes in crystalline phase sensitive 1296 cm^{-1} (A_1) band of VDF 72% copolymer upon heating-cooling cycle (denoted by the arrows) for (b) as-cast and (c) annealed samples.

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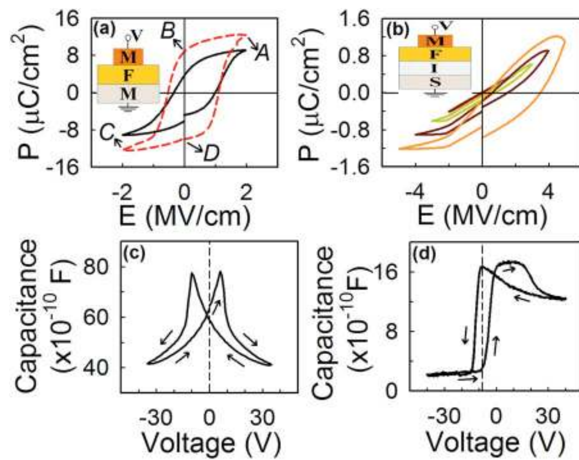

FIG. 2. (Color online) (a) Polarization-electric field (*P*-*E*) hysteresis curves of a Au/VDF 72% copolymer/Au (MFM) capacitor using 100 (dotted curve) and 50 (solid curve) nm thick VDF 72% copolymer annealed films. (b) *P*-*E* hysteresis curves of a Au/100 nm VDF 72% copolymer/100 nm SiO_2/n^{++}-Si (MFIS) diode showing dielectric-to-ferroelectric behavior with increasing external electric field from 2 to 5 MV/cm. (c) Capacitance-voltage (*C*-*V*) hysteresis curve for the MFM capacitor used in (a) with 100 nm VDF 72% copolymer. (d) *C*-*V* hysteresis curve for the MFIS diode used in (b). The arrows denote the rotation direction of the hysteresis loops in (c) and (d).

copolymer as-cast and annealed samples. The characteristic bands of the *all-trans* conformation associated with the β-crystalline phase show a significant increase in the absorption intensity for the annealed sample compared with the as-cast sample, as observed from the changes in the A_1 (1296 and 851 cm^{-1}, $\vec{\mu}\|\vec{b}$) and B_2 (1200 and 889 cm^{-1}, $\vec{\mu}\|\vec{a}$) bands. GIRAS used without a polarizer and with the IR incident angle closer to the grazing incident angle (80°–88°), predominantly detects the vibrational modes that have the transition dipoles normal to the substrate surface area.[5] Compared to the as-cast sample, the significant decrease in the 1403 cm^{-1} (B_1, $\vec{\mu}\|\vec{c}$) band intensity for the annealed sample tends to indicate the preferential orientation of the polymer chains parallel to the substrate surface.

The as-cast and annealed samples were further subjected to a heating–cooling cycle (30→110→30 °C, 0.8 °C/min). At 30 °C (after cooling from 110 °C), the as-cast sample exhibited a reversible crystalline phase transition with increased ferroelectric crystalline content [Fig. 1(b)] and decreased B_1 peak intensity [Fig. 1(a)(iii)] compared with Fig. 1(a)(i) due to the "nonisothermal annealed effect." The annealed sample exhibited a reversible crystalline phase transition [Fig. 1(c)], and a similar B_1 peak intensity [Fig. 1(a)(iv)] compared with that shown in Fig. 1(a)(ii). From the slopes of the thermal hysteresis curves [Figs. 1(b) and 1(c)], T_C during heating and cooling for the as-cast (72 and 66 °C) and annealed (76 and 62 °C) samples were determined. The heating-cooling cycle for the annealed samples exhibits a "memory effect," which can be utilized for formatting the NvRAM device by heating the annealed samples just above their T_C and then cooling to ambient temperature for reuse.

To determine a suitable memory device architecture for identifying the data-bit state, we compared MFM and MFIS structures fabricated using annealed samples of VDF 72% copolymer. Figure 2(a) shows the polarization-electric field (*P*-*E*) hysteresis for the MFM structure measured with a ferroelectric tester (Precision LC, Radiant Tech.) using an external electric field of 2 MV/cm under a single cycle of the bias electric field. Compared with the 100 nm sample, the 50 nm sample exhibited a much smaller remnant polarization (P_r) value under the same external electric field because of the reduced degree of crystallinity. Although data writing and erasing are simple for the MFM device architecture, one cannot avoid destructive data reading. For the 100 nm sample [Fig. 2(a)], the written data bit ["1," refer to D in Fig. 2(a)] and the erased data bit ["0," refer to B in Fig. 2(a)] can be read from the big difference in the current generated upon applying a bias electric field above its positive coercive field. However, when reading the bit 1, the dipole is switched to the opposite direction resulting in the bit 0 state. Thus, an additional programming process is required to return to the original bit 1 state. In the MFIS architecture case shown in Fig. 2(b), the P_r values were reduced because of the presence of the insulating layer (SiO_2) and the Si wafer. The purpose of using the SiO_2 insulator is to avoid electrical shorting, and increase the thermal stability as well as memory retention time characteristics.

Figure 2(c) shows the capacitance-applied voltage (*C*-*V*) pattern [measured using an *LCR* meter (ZM-2353) connected to a Keithley2400 for applying variable dc-bias voltages to the sample] for the VDF 72% (100 nm) sample using the MFM architecture. Typical symmetrical loops having similar patterns for both positive and negative electric field directions [Fig. 2(c)] were observed. This makes it still difficult to identify the data-bit state at the zero bias voltage. The MFIS device using VDF 72% (100 nm) and SiO_2 (100 nm) as an insulating layer on a n^{++}-Si wafer exhibits asymmetrical *C*-*V* hysteresis loops [capacitance on/off ratio (C_{on}/C_{off})=5.66] shifting toward the negative side, as shown in Fig. 2(d). The data-bit state can be clearly identified with the C_{on}/C_{off} ratio at −8 V. However, to continuously maintain the written data state, it is necessary to apply −8 V to the MFIS device. Hence, this is not a viable option in our attempt to find a workable NvRAM device structure.

Fujisaki *et al.* suggested the fabrication of a MFIS structure using Ta_2O_5 as an insulating layer to prevent the shifting of the *C*-*V* hysteresis curve toward a negative electric field direction.[7] In our study, PVP (130 nm) on a p^{++}-Si wafer instead of SiO_2 prevented the shifting of the *C*-*V* hysteresis curve in the MFIS toward the negative direction [Fig. 3(a)(i)], enabling an easier identification of the on and off states (C_{on}/C_{off}=3) at zero bias voltage. When the PVP layer thickness is reduced to 40 nm, a drastically reduced programming voltage is observed with a slightly higher C_{on}/C_{off} ratio of 3.82 [Fig. 3(a)(ii)]. Replacing PVP with a thinner UV-irradiated PVA-ADC layer (80 nm) [Fig. 3(a)(iii)] also showed a good C_{on}/C_{off} ratio (4.07), as well as a low programming voltage. To see the effect of the ferroelectric layer on the bistability of the MFIS device, we also used a Au (M)/130 nm PVP (I)/p^{++}-Si (S) structure [inset in Fig. 3(a)]. Although the memory window in the MIS is much smaller (C_{on}/C_{off} ratio=2.19) than in the MFIS structure with identical PVP thickness, the advantage of MIS is that the operating voltage is much lower than that used in the MFIS case. But the disadvantage in MIS is the shifting of *C*-*V* hysteresis toward the positive bias voltage and a short memory retention time. The *C*-*V* hysteresis in the MIS may originate from the PVP exhibiting a quasipermanent electrical charge or dipolar polarization, even though it is known to be a dielectric

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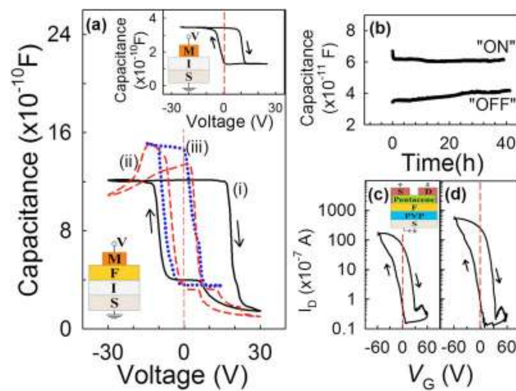

FIG. 3. (Color online) (a) C-V hysteresis loops of (i) Au/100 nm VDF 72% copolymer/insulator/p^{++}-Si (MFIS) diodes using 130 nm PVP (solid line), (ii) 40 nm PVP (long dash line), and (iii) 80 nm PVA-ADC (dotted line) as insulator. The inset shows the C-V hysteresis curve of a Au/130 nm PVP/p^{++}-Si MIS device structure. (b) Data retention properties of the on and off states of the MFIS diode with VDF 72% copolymer (100 nm) and PVP (320 nm) as insulator. Transfer curves at constant drain voltage=−10 V for a pentacene based FeFET device structure having a bilayered VDF 72% copolymer (100 nm)/PVP (130 nm) gate insulator with 800 μm channel width and varying source-drain channel lengths of (c) 100 μm and (d) 20 μm. The arrows denote the rotation direction of the hysteresis loops.

material rather than a ferroelectric material. Other reason may include charge trapping at the interface between PVP and Si and/or in the PVP layer near the interface.[17] This kind of charge trapping cannot be maintained for a long time because of the slow leakage of trapped charge by thermal relaxation. Thus, another ferroelectric layer having a permanent dipolar polarization is needed as in the MFIS to increase the memory retention time.

Figure 3(b) shows data retention properties of the on and off states measured using a Au (M)/100 nm VDF 72% (F)/320 nm PVP (I)/p^{++}-Si (S) structure. The MFIS device was biased after applying ±40 V for 10 s so that the device completely turns on at −40 V and turns off at +40 V. The device capacitance was found to exhibit only a slight reduction from the initial value after 10 h. The on/off ratio reduced by 25% during the measuring time of 40 h.

In another study, we prepared a pentacene-based (30 nm thick, positive organic semiconductor) FeFET device with a bilayered P(VDF-TrFE) (180 nm)/PVP (70 nm) gate insulator. The transfer curve [Fig. 3(c)] scanned with the sweep gate voltage of ±60 V at a fixed drain voltage of −10 V (source-drain channel length: 100 μm; channel width: 800 μm) clearly displays a typical ferroelectric clockwise hysteresis with the drain current on/off ratio of 70 at zero gate bias. As expected, the measured drain current values increased and the on/off ratio also increased to 282 at zero gate bias with decreasing source-drain channel length (20 μm) for the same channel width [Fig. 3(d)].

In summary, the FTIR-GIRAS data were useful to assign the working temperature limit (below their T_C during heating) of NvRAM devices based on VDF 72 mol % copolymer annealed nanoscale films. Using C-V measurements, the MFIS device structure was found to be more suitable for the easier identification of the data-bit state than the MFM device. The disadvantage of using SiO_2 as an insulating layer was eliminated by using a PVP layer or cross-linked PVA layer, which prevented the shifting of the C-V hysteresis curve in the MFIS toward a positive or negative bias voltage, thereby enabling the written data to be distinguished even at zero bias voltage.

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