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Control Architecture for Cascaded H-Bridge Inverters in Large-Scale PV Systems

Sridhar V.[a] , Umashankar S.[b]*, Sanjeevikumar P.[c],
Vigna K. Ramachandaramurthy[d], Lucian Mihet-Popa[e], Viliam Fedák[f]

[a,b] *School of Electrical Engineering, VIT University, Vellore, 632014, India.*
[c] *Department of Energy Technology, Aalborg University, 6700 Esbjerg, Denmark.*
[d]*Power Quality Research Group, Universiti Tenaga Nasional, 43000, Kajang, Selangor, Malaysia.*
[e] *Faculty of Engineering, Østfold University College, Kobberslagerstredet 5, 1671 Kråkeroy-Fredrikstad, Norway.*
[f] *Department of Electrical Engineering & Mechatronics, Technical University of Košice, Košice, Slovak Republic.*

Abstract

An H-bridge along with the auxiliaries is the fundamental power module to build the cascaded H-bridge (CHB) inverter. In this paper, the design of basic building block of CHB inverter for PV applications with bypassing feature is discussed. Independent MPPT controls of each PV array at module level are proposed in this work. Instead of processing entire controls in one processor, different stages of controls and distributed processing of various functions of the system are proposed to improve the speed of computation. With this control architecture, hardware requirements of the individual processor cards also reduced. Functionalities of each controller card namely module level control card, phase-level control card, and master controller cards are explained in detail. Detailed interfacing and signal exchange between H-Bridge modules and the other controller cards are also presented. Simulation results are presented to verify the operation of the system with the proposed control architecture.

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Keywords: Cascaded H-Bridge; Control architecture; Multilevel; PV inverter

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* Corresponding author. Tel.: +91-9003260199.
E-mail address: shankarums@gmail.com.

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1. Introduction

Cascaded H-Bridge based multilevel inverter topology is very popular for high voltage, high power applications. There is a lot of demand in the market for this configuration due to the features such as modular in construction, power quality, better THD, low filter size, etc... Cascaded H-Bridge based PV inverters are suitable for high power PV applications. Independent maximum power point tracking (MPPT) controls for each PV array is possible through this configuration. A review on Cascaded H-Bridge (CHB) inverters is carried out in [1]-[4]. Controls for independent MPPT for CHB based PV inverter is presented in [5]-[6] and both the works are mainly focused on the MPPT controls, where as the present work focuses mainly on the control architecture.

Since a CHB inverter consists of multiple PV arrays, the MPPT of each module with a common controller will affect the speed of computing or processing. To improve the processing speed and to maintain the modularity, three different levels of controllers are proposed in this work. Each H-Bridge module is interfaced with a module level controller card (MLC) and all the MLC cards of one phase communicate with the Phase controller card (PC) of respective phases. Three numbers of phase controller cards communicate with the Master controller. Master controller receives the signals such as grid voltages and currents for regulating the power flow through the PV inverter. The block diagram of the control interface is shown in Fig.1. In this work, basic introduction to the H-Bridge module, details of module-level card, the signal exchange between module level card and phase card and the functionalities of Master controller are explained in detail.

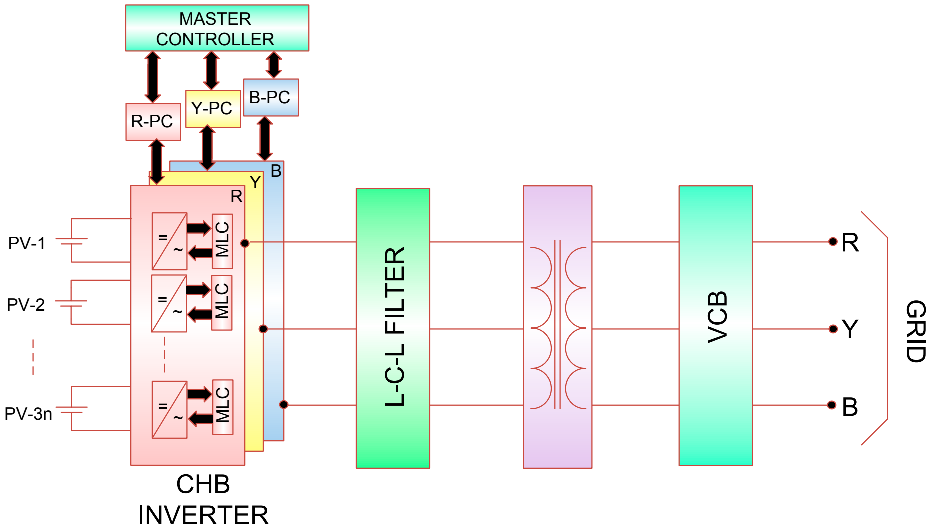


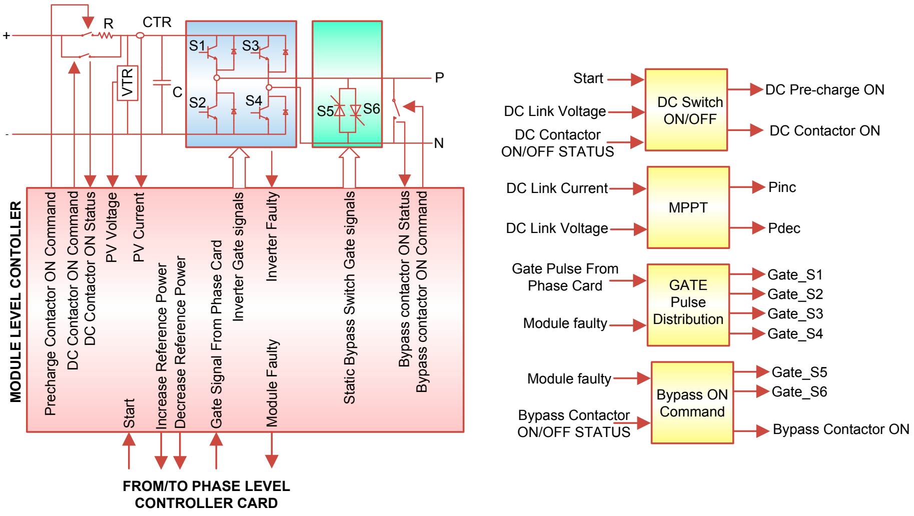
Fig. 1. Block diagram of a Grid-connected CHB based PV-Inverter

Nomenclature

CHB	Cascaded H-Bridge
DAB	Dual Active Bridge
ESS	Energy Storage System
MLC	module Level Card

2. Basic Building Block of CHB Inverter

Fig. 2(a) shows the basic building block of a CHB inverter. This module comprises of an IGBT based H-Bridge, Thyristor based static bypass switch, DC voltage transducer and DC current transducer, DC contactor, pre-charge contactor and the bypass contactor. Module level card is also the integral part of this module.



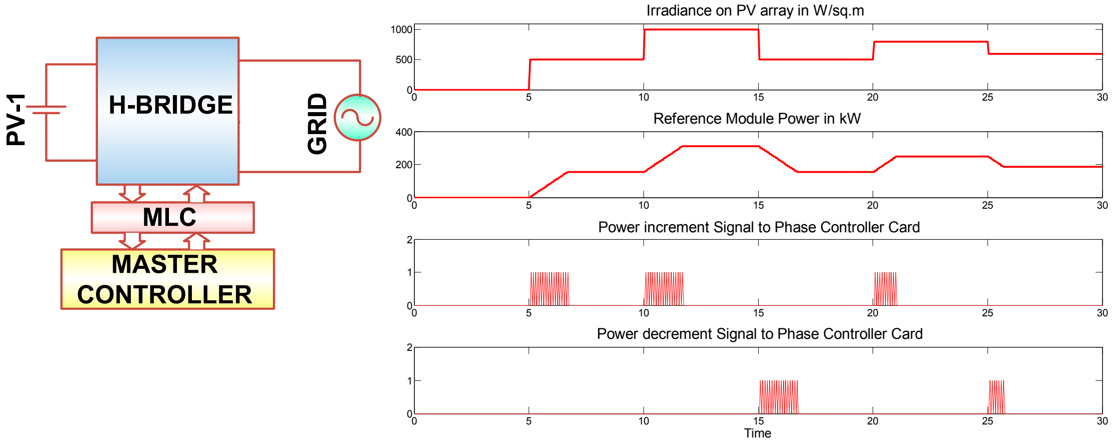
(a) (b)

Fig. 2. (a) Block diagram of building block of CHB inverter (b) Functional block diagram of Module level Card

Functional operation of module-level card for PV applications is shown in Fig 2(b) and explained below

a) When the start command is received from the Phase level card, then the module level controller gives on command to pre-charge contactor and subsequently to the main DC contactor.
b) Four gate signals for the inverter are derived from one gate signal received from the phase card.
c) If the inverter fault signal becomes high, then that information will be communicated to the phase level card and the bypass switch will be operated for continuous operation. Thyristor based static bypass switch is used for faster switching and this is for short time operation. Bypass contactor in parallel to the static bypass switch is required for continuous operation.
d) The main functionality of the module level controller card is tracking the maximum power point (MPP) of the associated PV array connected to DC link. PV voltage and currents are monitored and then MPP tracking is carried out in this processor itself.
e) Based on MPP, increase or decrease power reference command will be sent to the phase level controller card. In case both the signals are Low/high, then the reference power has to be maintained same.

To verify the operation of the Module level controller card, a single phase grid connected H-bridge module fed from a PV array as shown in Fig.3 (a) is simulated. In this phase controller card is not used, since the system is very small.



(a) (b)

Fig. 3. (a) Grid Connected Single phase Inverter (b) Tracking of Maximum Power Point in Module level Card

Maximum PV array Power Rating = 350kW
Step change in Power during MPPT = 2 kW
Reference power Pn = P(n-1) + (Pinc X 2kW) – (PdecX 2kW) ------------ (1)
Where
P(n-1) is Inverter power at previous sample time
Pinc is "Increase the reference power" signal generated in Module level controller card
Pdec is "Decrease the reference power" signal generated in Module level controller card

Maximum power point tracking with the change in irradiance values is shown in Fig.3(b). in equation (1) , initially 'P(n-1)' is Zero and when the Irradiance is increased from Zero to 500W/sq.m at time 5 sec, Pinc signal is generated and accordingly the reference power is increased in steps of 2kW. Similarly, when the irradiance is reduced from 1000 to 500W/sq.m at time 15 sec, Pdec signal is generated and accordingly the reference module power is reduced in steps. In this system Perturb and observe method of MPPT is adapted. The MPPT methods presented in [7]-[13] can also be adapted for this system.

3. Phase Level Control Card

Fig. 4. Shows the signal exchange between module level controller cards and the Phase level controller card. N number of MLC cards are interfaced with one Phase level card where 'N' is the number H-bridges per phase. Phase level controller receives the start command and reference voltage signal from the master controller and performs the following functions

a) Depending on the number of healthy H-bridges, one gate signal for each module is derived internally. A level shifted PWM technique is adopted in this work.

b) By compiling the Increase/decrease reference power signals received from each MLC card, the reference voltages for each module are derived and the gate pulse is generated accordingly.

c) It also generates an overall increase/decrease reference power signal and provides the signal to the master controller card.

d) A Phase faulty signal is generated if the number of faulty modules is more than the minimum number of modules required for continuous operation.

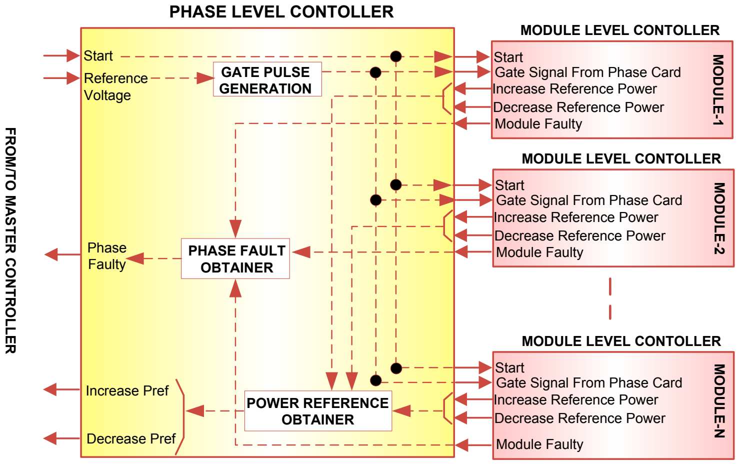


Fig. 4. Functional Block diagram of Phase level Controller card

4. Master Controller

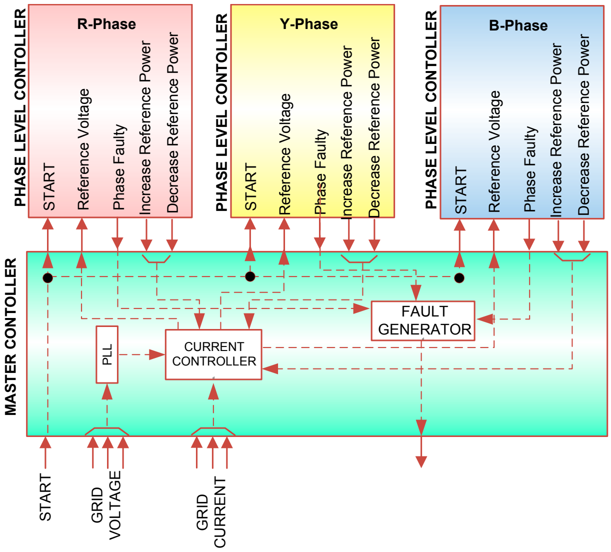


Fig. 5. Functional block diagram of Master Controller Card

Fig. 5 shows the signal exchange between the master controller and the three numbers of Phase level controller cards. Master controller performs the following functions

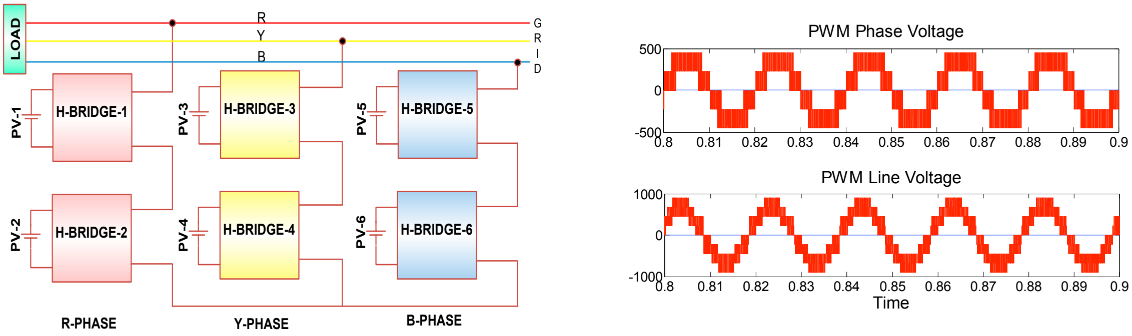
a) Based on the increase/decrease reference power signals received from the phase controller cards, reference active power is calculated in the main controller.
b) Based on the reference power, reference inverter current is calculated.
c) The main controller monitors the grid voltages for PLL and the grid currents for the closed loop current control.
d) Based on the current controller output, the reference voltage signal for each phase is generated.

5. Results and Discussions

Three phase CHB inverter with two numbers of H-Bridges per phase shown Fig.6 (a) is simulated to verify the operation of the system with the proposed control architecture. Electrical specification of the system is as given in Table.1. Fig.6(b) Shows the Phase and Line voltages of Inverter PWM output. Since the number (N) of H-bridges used per phase is Two, the number of levels in the phase voltage is Five (2N+1) and the number of levels in the Line voltage is Nine (4N+1). Fig.7 shows the Inverter output current with the change in the irradiance. Initially, irradiance of 1000W/sq.m is adjusted and reduced it in steps of 200 W/sq.m in each 0.15 sec. Equal irradiance is considered for all the PV arrays. Hence when the irradiance is reduced, the reference power is reduced, so the reference inverter current also reduced. When the irradiance becomes Zero, the inverter current is also Zero.

Table 1. Electrical specification for the CHB based PV- inverter

Electrical parameter	Value	Units	Description
Grid Voltage	400	V	Three Phase
Rated Power of the system	500	kW	
No of H-Bridges per phase (N)	2	No's	
No of PV arrays	6	No's	
Peak power of each PV array	100	kW	Total 600 kWp > Rated Power
PV Array Nominal voltage	250	V	
No. of levels in Phase voltage	5	Levels	2N+1
No. of levels in Line output	9	Levels	4N+1



(a) (b)

Fig. 6. (a) Three-Phase 5-Level CHB Inverter (b) Phase Voltage and Line voltages of Inverter PWM output

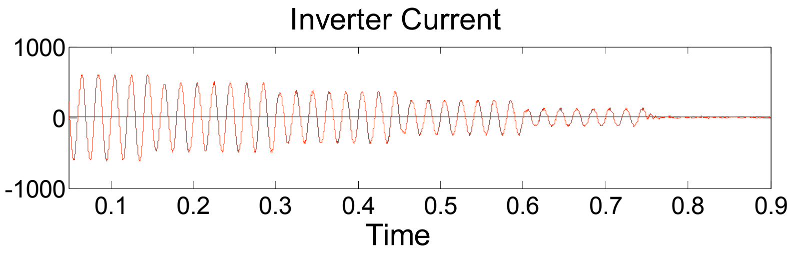


Fig. 7. Inverter Output current with the gradual Change in the Irradiance from 1000 W/sq.m to Zero W/sq.m

When a fixed resistive load is connected to the grid, the Load current is always constant since the Grid voltage is also fixed. Since the load is purely active, the Load current is lagging the Load voltage by 30 electrical degrees as shown in Fig.8. Initially, inverter power is more than the load requirement, hence the additional power is fed to the grid, and hence the grid power is negative. When the irradiance is reduced at time 0.45 sec, the PV power is less than the load requirement; hence the grid supplies the remaining power. In this case, grid power is also positive as shown in Fig.8. Since the inverter is always supplying the power to the Grid/load, inverter power is always positive. From the presented results, it is observed that the dynamic performance of the system is good for the changes in the irradiance values.

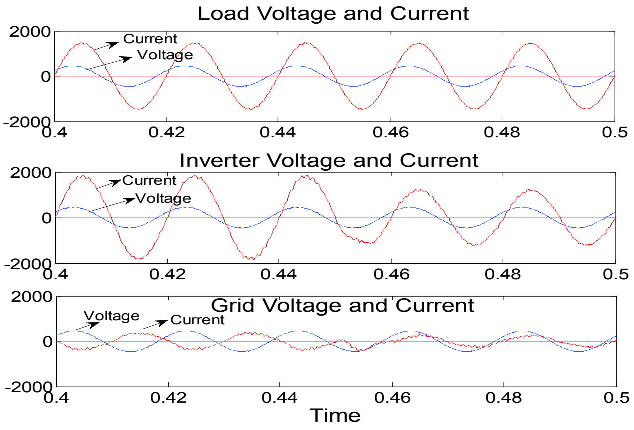


Fig. 8. Line voltage and Currents of Load, Inverter, and Grid at Two different Irradiance values

6. Conclusions

In this work, the control architecture of a CHB inverter for PV applications is proposed. The functionality of various controller cards, the signal exchange between the cards are explained in detail. The main functionalities of module-level controller are MPP tracking and Gate pulse distribution. Phase controller card is required for independent voltage control of each H-Bridge. The master controller processes the current control and provides the reference voltage single. Computational speed of the master controller is improved since the MPP tracking is carried out at module level itself. Since various functions of the system are distributed among three different cards; the hardware requirements of each processor card are minimized. The proposed control architecture is verified through simulation studies on a grid-connected 5-Level CHB based PV inverter. To validate the performance of the proposed control architecture for large-scale systems, Controller in Loop Simulations can be carried out with the help of real-time digital simulator as future work.

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