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Control strategies for seamless transfer between the grid-connected and islanded modes of a microgrid system

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ABSTRACT

Design of control strategies for Distributed generation systems is very important to achieve smoother transition between the grid connected and islanding modes of operation. The transition between these two modes of operation should be seamless, without any severe transients during the changeover. In this paper, two different control strategies namely inverter output current control and indirect grid current control for the seamless transfer between the modes of operation has been explored for the suitability. The design and analysis of the cascaded control loops based on Proportional Integral (PI) controller has been dealt in detail for both inverter output current control and indirect grid current control strategy. Control parameters are designed using the control system toolbox in MATLAB. A 10kW grid connected microgrid system has been designed and simulated in MATLAB/Simulink and the results are presented under grid connected operation, islanding operation and the transition between the modes considering fault condition in the grid side. The simulation studies are carried out using both the control strategies and the results are presented to validate the design methodology.

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1. INTRODUCTION

As the conventional energy resources are fast depleting and are of polluting nature, renewable energy resources are being harnessed in meeting the ever increasing demands [1]. Recently, Distributed Generators which are mainly based on the resources such as Wind, Solar PV, hydro, natural gas, biogas, fuel cells etc., has gained lot of interest due to the increase in demand for the reliable and quality power [2]. Distributed Energy Resources (DER) can either be coupled straightaway to the distribution network at the point of common coupling (PCC) or can be interconnected to form a Microgrid (MG) [3]. Power electronics play a major role in integrating the renewable energy sources (RES) into the utility grid [4-6]. A microgrid is a collection of energy sources which are of smaller capacity, energy storage schemes and a group of loads which are being operated at distribution voltage levels [7]. Generally microgrids are associated with the main grid at PCC and are operated as grid connected system. But under certain circumstances, microgrids can be moved to the islanded mode of operation either intentionally or unintentionally [8]. The interfacing inverter is to be controlled in such a manner that the microgrid works in asscociation with the main grid , independently as islanded case when needed , and also while moving from one mode to other mode seamlessly [9-11].

In the case of grid connected operation, the interfacing power electronic converter is being controlled so as to supply the main grid with the preset / stated power while the load voltage is being maintained by the utility [12]. Under islanded mode, control of the inverter is mainly focussed to provide

uninterrupted supply of electricity to the critical loads, with voltage and frequency within the stipulated bounds [13].When the utility grid fails, because of any faults; the microgrid gets disconnected and operates in autonomous mode. The islanding detection system detects the occurrence of faults in the utility side and isolates the microgrid [14-16]. After the confirmation of islanding, the switch in the grid side is to be opened and the load voltage is controlled by the inverter control system.

Hence, there will be a short duration in which the voltage across the load will not be the same as the utility voltage or the microgrid system voltage maintained by the DG system and consequently the quality of the voltage gets deprived under such circumstances [17]. Many control strategies have been proposed in the literature for attaining smooth transition between the operating modes of microgrid [18-21]. The inverter is controlled as a current source in grid connected mode for transferring power to the grid and as a voltage source during islanding mode for maintaining voltage within the limits. Separate controllers are needed for the two modes of operation and the switching between the control actions leads to poor voltage quality especially during the transient process [22, 23].

For seamless transition between the modes, voltage source based droop controllers are employed [24]. Droop controllers that are implemented [25] for the power sharing among the DG systems that are connected in parallel to feed the total connected load, leads to poor dynamics. A Master-slave control is another common approach in microgrid where a Master unit i.e., the Voltage Source Inverter (VSI) which is being controlled by PQ control structure for regulating the real and reactive power fed into the grid and under islanding mode, the master unit is to be controlled as Voltage/frequency (V-f) control for maintaining the voltage and frequency [26]. A novel control scheme has been developed in [27] which consist of capacitor voltage controller as outer loop and inductor current controller as inner loop for improving the voltage quality during the transition.

In another control scheme [28], the inverter output current is being controlled. The current fed to the utility is regulated with the help of the filter inductor current control which in turn controls the capacitor voltage and hence the microgrid voltage quality can be improved during the mode transition. In [17], the current fed to the utility grid is regulated indirectly by having proper control of the voltage across the filter capacitor. So among the existing inverter control techniques for achieving seamless transfer between the modes and also to maintain the voltage that appears across the load during transition, output current control and indirect current control or grid current control strategy has been preferred mostly.

In this paper, the design and analysis of two different control strategies namely, output current control and indirect grid current control are explored for the suitability in grid connected microgrid system. The cascaded control loops are designed based on Proportional Integral (PI) controller. Control parameters of the control loops are designed using the control system toolbox in MATLAB. A 10kW grid connected microgrid system has been designed and simulation studies are being carried out in MATLAB/Simulink environment and the various simulation results under grid connected operation, islanding operation and the transition between the modes, considering fault condition in the grid side are presented. The main contribution of this paper is that, simulation studies have been carried out using both the control strategies and the results are presented to validate the design methodology and the performances of the control strategies are compared.

This paper deals with design, analysis and simulation studies of the control strategies for seamless transfer in grid connected microgrid system. Section 2 presents the modelling of three phase inverter system. Control strategies for seamless transfer are discussed in section 3. Sections 4 and 5 deals with the analysis and design of control parameters for the control strategies discussed in section 3. Simulation results are discussed in section 6. Section 7 proposes the conclusion.

2. MODELLING OF A THREE PHASE INVERTER SYSTEM

The power stage of a three phase inverter system is modelled based on synchronous reference frame and the control strategies for the seamless transition using inverter output current control as well as the indirect current control are presented.

2.1. Power stage of a three phase inverter in microgrid

The power stage of a three phase MG system is shown in Figure 1. The input side of the inverter is considered as a stiff dc voltage. The energy sources can be of solar PV/ fuel cell or any renewable energy sources. However the output voltages from these sources are very less and needs be boosted to the required level with the help of the DC-DC converter. A voltage controller can be used to attain the desired dc link voltage which is not dealt in this paper.

The output voltage from the three phase inverter is filtered with the help of LC filter consisting of inductor L_f and the capacitor C_f. The filtered output is then connected to the local loads which may be

critical/non-critical loads and it is coupled to the main grid via an inductor L_g called grid-side inductor. The static transfer switch S_i, present in the inverter side is being actuated by the inverter side controller and the switch S_g present in the grid side is being actuated by the grid. Under normal working conditions of the utility, both the switches S_i and S_g are in the closed position and hence the three-phase DG inverter is operated in the grid connected manner. In case of any faulty conditions or operations in the grid, the switch S_g is opened which makes the DG system islanded.

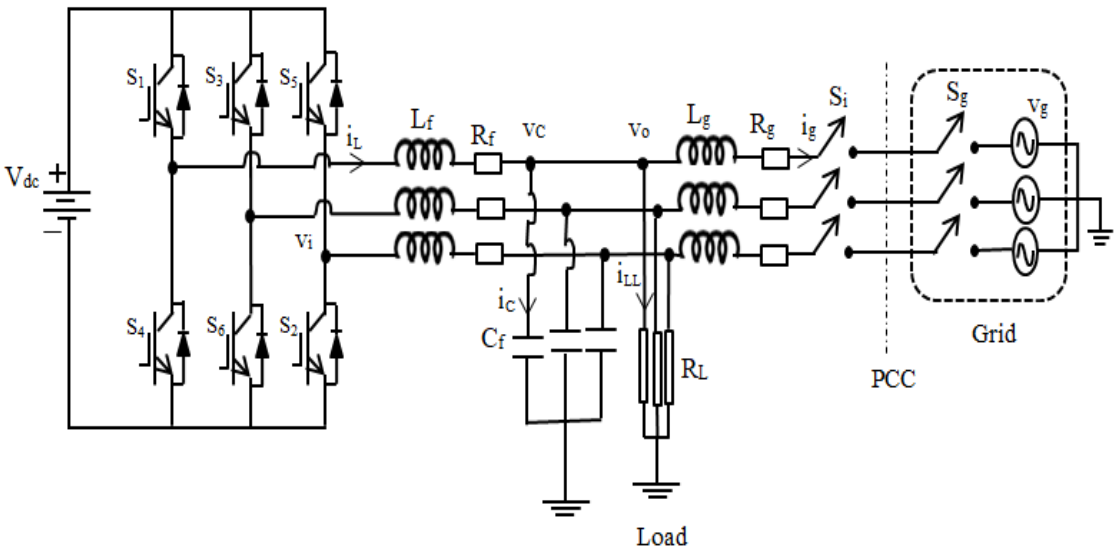

Figure 1. Power stage of a three phase MG system

After the islanding detection, the inverter side switch S_i is also opened and DG enters in to standalone mode. Once the fault is cleared, the switch S_g is being closed. The DG side switch S_i is closed to make the system to be operated in association with the utility only after the resynchronization process takes place.

2.2. Modelling of the power stage

The average mathematical model of a three phase inverter system is given by (1) and (2).

$$\frac{V_{dc}}{2}.\begin{pmatrix} d_a \\ d_b \\ d_c \end{pmatrix} = L_f.\frac{d}{dt}\begin{pmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{pmatrix} + R_f.\begin{pmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{pmatrix} + \begin{pmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{pmatrix} \quad (1)$$

$$\begin{pmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{pmatrix} = C_f.\frac{d}{dt}\begin{pmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{pmatrix} + \begin{pmatrix} i_{LLa} \\ i_{LLb} \\ i_{LLc} \end{pmatrix} + \begin{pmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{pmatrix} \quad (2)$$

In synchronous reference frame modelling, the equations governing the system shown in Figure 1 are given by (3) to (5).

$$\frac{V_{dc}}{2}.\begin{pmatrix} d_d \\ d_q \end{pmatrix} = L_f.\frac{d}{dt}\begin{pmatrix} i_{Ld} \\ i_{Lq} \end{pmatrix} + \begin{pmatrix} 0 & -\omega L_f \\ \omega L_f & 0 \end{pmatrix}.\begin{pmatrix} i_{Ld} \\ i_{Lq} \end{pmatrix} + R_f.\begin{pmatrix} i_{Ld} \\ i_{Lq} \end{pmatrix} + \begin{pmatrix} v_{Cd} \\ v_{Cq} \end{pmatrix} \quad (3)$$

$$\begin{pmatrix} i_{Ld} \\ i_{Lq} \end{pmatrix} = C_f.\frac{d}{dt}\begin{pmatrix} v_{Cd} \\ v_{Cq} \end{pmatrix} + \begin{pmatrix} 0 & -\omega C_f \\ \omega C_f & 0 \end{pmatrix}.\begin{pmatrix} v_{Cd} \\ v_{Cq} \end{pmatrix} + \begin{pmatrix} i_{LLd} \\ i_{LLq} \end{pmatrix} + \begin{pmatrix} i_{gd} \\ i_{gq} \end{pmatrix} \quad (4)$$

$$\begin{pmatrix} v_{Cd} \\ v_{Cq} \end{pmatrix} = L_g.\frac{d}{dt}\begin{pmatrix} i_{gd} \\ i_{gq} \end{pmatrix} + \begin{pmatrix} 0 & -\omega L_g \\ \omega L_g & 0 \end{pmatrix}.\begin{pmatrix} i_{gd} \\ i_{gq} \end{pmatrix} + R_g.\begin{pmatrix} i_{gd} \\ i_{gq} \end{pmatrix} + \begin{pmatrix} v_{gd} \\ v_{gq} \end{pmatrix} \quad (5)$$

Where d_d and d_q are the duty cycles of three phase inverter system in synchronous reference frame, R_f represents the resistance of filter inductor L_f, i_{Ld} and i_{Lq} represents the currents through the inductor L_f, i_{LLd} and i_{LLq} represents the load currents in 'd q' frames respectively and R_g indicates the resistance of the grid side inductor L_g. Figure 2 represents the block diagram of power stage modelling of MG system in Synchronous reference frame (SRF).

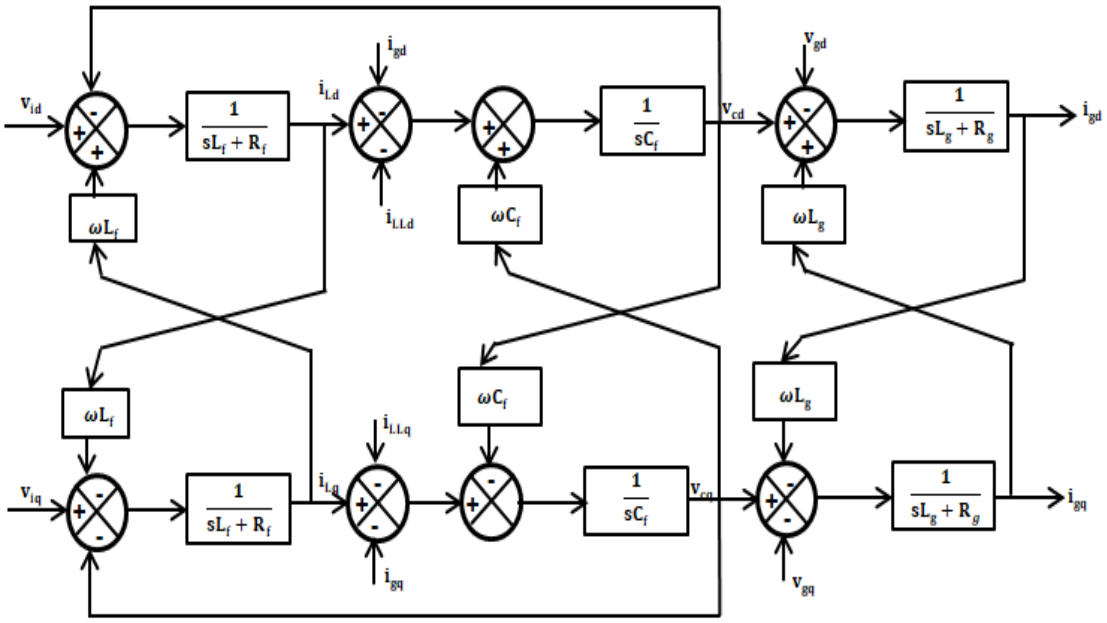

Figure 2. Power stage model of the MG system in SRF

3. CONTROL STRATEGIES FOR THE SEAMLESS TRANSFER

3.1. Inverter output current based seamless transfer

The current fed to the grid can be regulated by controlling the inverter output current. The inductor current $i_{L,abc}$ and the capacitor voltage $v_{C,abc}$ are sensed and are transformed to dq components using Park's transformation. The basic structural diagram of the output current control scheme is shown in Figure 3. The control includes three loops viz., output current loop, inner voltage control loop, innermost inductor current loop and a phase locked loop (PLL) for phase detection.

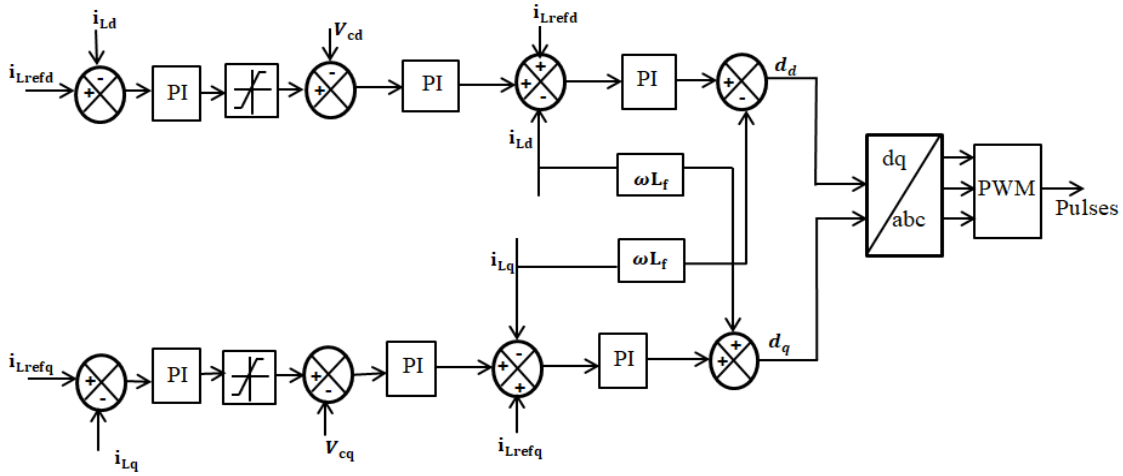

Figure 3. Control scheme based on output current control

The output current controller is being realized with the help of a proportional-integral (PI) controller. The output of the current controller generates the reference values for the capacitor (load voltage) voltage loop i.e., v_{Crefd} and $v_{Crefq.}$ A PI controller based inner voltage control loop regulates the capacitor voltage v_{Cd} and v_{Cq} to follow the reference voltages generated by the outer loop. The innermost current controller is mainly intended to maintain the required output current from the inverter which comprises of the current that is to be fed to the utility as well as the current required by the load. Hence the grid current is controlled with the help of inverter output current control. PLL used in the system is based on SRF to measure the utility frequency and phase angle, which mainly includes a PI controller and a magnitude limiter to maintain the frequency of the local load within the acceptable limits especially during islanding mode of operation.

3.2. Indirect current control based seamless transfer

The structural diagram of the indirect grid current control scheme is shown in Figure 4. Seamless transfer based on this control scheme involves grid current control by regulating the load voltage (capacitor voltage) when operating under grid connected mode. Control scheme comprises of three control loops viz., outer grid current control loop, inner capacitor voltage loop and the innermost filter inductor current loop. The outer grid current controller along with a limiter sets the reference voltage during the islanding condition. Under grid connected condition, the voltage is going to be within the limits. The inner capacitor voltage loop is a PI controller which generates the reference currents in d and q axis for the innermost filter inductor current loop. The inductor current loop is a PI controller which produces the reference signal in dq frame. The reference signal is transformed into 'abc' frame using dq-abc transformation and then given to PWM generator for generating the firing pulses for the inverter switches.

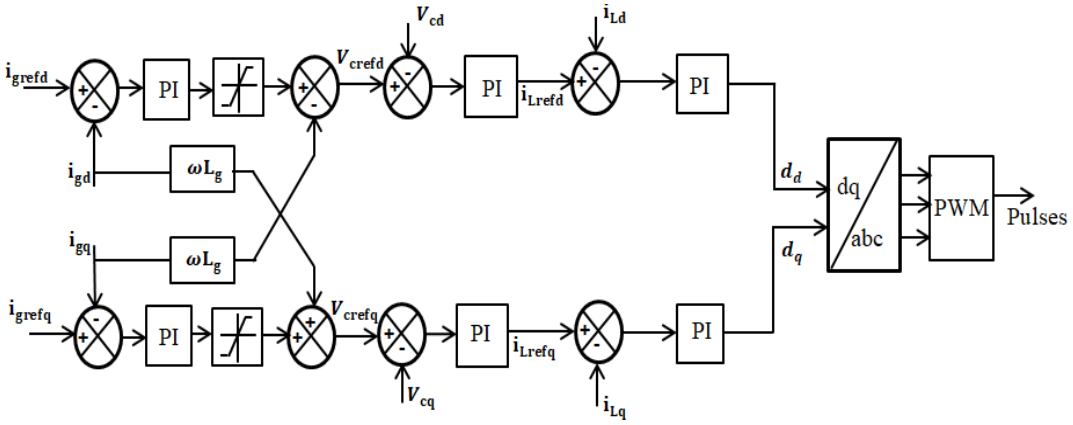

Figure 4. Indirect grid current control scheme

When the main grid is working without any faults, the MG is treated as current source so as to feed in the required active and reactive power to the grid. The reference currents in d and q axis can be calculated based on the complex power that is to be fed to the grid. The grid current is controlled using a PI controller. The coupling introduced due to the grid side inductor L_g is being attenuated by decoupling in the current control loop. When any fault occurs in the grid side, the utility side switch, S_g opens and the MG is moving to islanding mode of operation. The inverter switch S_i is still in the closed position as the MG has to confirm the occurrence of islanding. The switch S_i opens, once the islanding is confirmed by the islanding detection method. The active and reactive power injected into the grid is given by (6) and (7).

$$P_g = \frac{3}{2} . \left(v_{gd} i_{gd} + v_{gq}\, i_{gq}\right) = \frac{3}{2} . v_{gd} i_{gd} \quad (6)$$

$$Q_g = \frac{3}{2} . \left(v_{gq} i_{gd} - v_{gd}\, i_{gq}\right) = -\frac{3}{2} . v_{gd} i_{gq} \quad (7)$$

In islanding mode of operation, the switches S_i and S_g are open and PLL cannot track the grid phase angle. Under this condition, the MG is operated as a voltage source and therefore voltage fixed by the limiter acts as the reference voltage. PLL consists of a PI controller and a limiter, which is used to regulate the frequency within allowable limits.

4. ANALYSIS AND DESIGN OF CONTROL PARAMETERS OF OUTPUT CURRENT BASED SEAMLESS TRANSFER

4.1. Design of voltage magnitude limiter

The voltage limiter present in the Figure 3 and in Figure 4 is used to provide a stabilized voltage without any deviation when the system gets transferred from grid connected mode to islanded mode. As per the IEEE standard 1547_2018 [29], the voltage limiter in d and q axis can be represented by (8) and (9).

$$v_{d,max} = 1.1 * \sqrt{2} * V_{nominal} \quad (8)$$

$$v_{d,min} = 0.9 * \sqrt{2} * V_{nominal} \quad (9)$$

where, $v_{d,max}$ and $v_{d,min}$ represents the maximum and minimum values of the voltage magnitude in the d axis, $V_{nominal}$ is the nominal per phase grid voltage. When the MG transfers from grid connected mode to islanded mode, the voltage limiter in the q axis is to be designed based on (10) and (11), so that the load voltage is within the normal range.

$$v_{q,max} = +\varepsilon \quad (10)$$

$$v_{q,min} = -\varepsilon \quad (11)$$

where, $v_{q,max}$ and $v_{q,min}$ represents the maximum and minimum values of voltage in q axis.

4.2. Design of frequency / phase limiter

The frequency and phase of the grid voltage can be obtained with the synchronous reference frame based PLL, when the MG system is operating in grid connected mode. When the fault occurs in the grid side, the frequency and phase may get deviated. In order to limit the deviations beyond a level, a limiter is being introduced to restrict the frequency and phase deviations during islanding. The basic block diagram of SRF-PLL is shown in Figure 5.

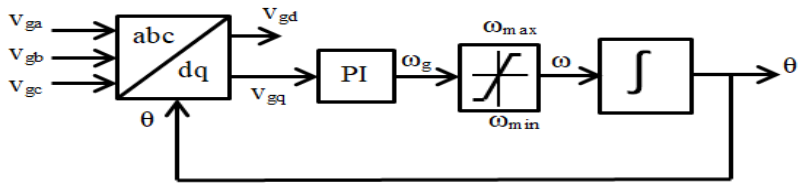

Figure 5. Block diagram of SRF-PLL

4.3. Design of filter and control loops

The specification of the parameters used in the DG system considered is given in Table 1. The filter and the control loop parameters are designed based on the DG specifications.

Table 1. Parameters of the MG system

Parameters	Symbol	Value
DC link voltage	V_{dc}	700 V
Filter inductor	L_f	3.11 mH
Resistance of filter inductor	R_f	1 Ω
Filter capacitor	C_f	10 μF
Switching frequency	f_s	20 kHz
Grid side inductor	L_g	3.11 mH
Resistance of grid side inductor	R_g	1 Ω
Grid frequency	f_g	50 Hz
Grid voltage	V_g	220 V(rms)
Rated power of DG	P_{DG}	10 kW
Power rating of Load	P_L	5 kW

4.3.1. Design of LCL filter

The output from the three phase inverter is filtered with the help of LCL filter [30] to suppress the harmonics introduced due to the presence of power electronic interface. The base impedance and the base capacitance are obtained based on the (12) and (13).

$$Z_{base} = \frac{V_{L-L}^2}{P_{nominal}} \tag{12}$$

$$C_{base} = \frac{1}{\omega_g Z_{base}} \tag{13}$$

As the maximum power factor variation seen by the grid is 5%, the filter capacitance can be designed based on (14).

$$C_f = 0.05 * C_{base} \tag{14}$$

The maximum ripple allowable can be considered as 10% of the maximum rated current and the ripple is given by (15),

$$\Delta I_{max} = 10\% * I_{max} \tag{15}$$

where I_{max} is given by (16).

$$I_{max} = \frac{\sqrt{2} P_{nominal}}{3 V_{ph}} \tag{16}$$

The inverter side filter inductor, L_f is given by (17) and the grid side inductor, $L_g$is given by (18),

$$L_f = \frac{V_{dc}}{16 f_s \Delta I_{max}} \tag{17}$$

$$L_g = r L_f \tag{18}$$

where, V_{dc} represents dc link voltage, f_s , the switching frequency of the inverter switches and r is the ratio between L_f and L_g and the value of r is to be considered based on the nominal grid impedance and the resonant frequency from the transfer function of the filter. The resonant frequency and the frequency constraint are given by (19) and (20).

$$\omega_{res} = \sqrt{\frac{L_f + L_g}{L_f L_g C_f}} \tag{19}$$

$$10 f_g < f_{res} < 0.5 f_s \tag{20}$$

4.3.2. Design of innermost inductor current control loop

Figure 6 represents the basic structure of the innermost inductor current control loop.

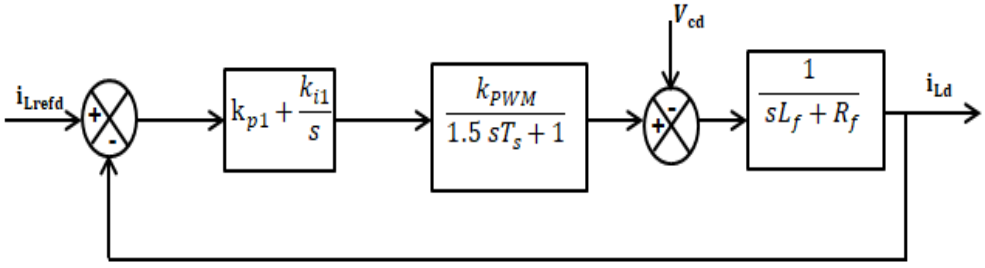

Figure 6. Control structure of inductor current control loop

From the Figure 6, the open loop transfer function of current control loop is given by (21).

$$G_{OL,IC}(s) = \frac{K_{PWM}\left(k_{p1}+\frac{k_{i1}}{s}\right)}{(1+1.5\,s\,T_s)(sL_f+R_f)} \quad (21)$$

Where, the digital delay is considered to be of 1.5 times the switching period T_s, K_{PWM} is the gain of the converter and is considered as 1 for simplicity. The controllers are designed in MATLAB using control system designer tool box. The bode diagram of the innermost inductor current loop with and without PI controller is shown in Figure 7, where G represents Transfer function without controller and LTF represents Loop transfer function with PI controller. The controller is designed to attain cut off frequency of around 1200 Hz and phase margin of 60°. The k_{p1} and k_{i1} values of the PI controller are about 27.014 and 8371.

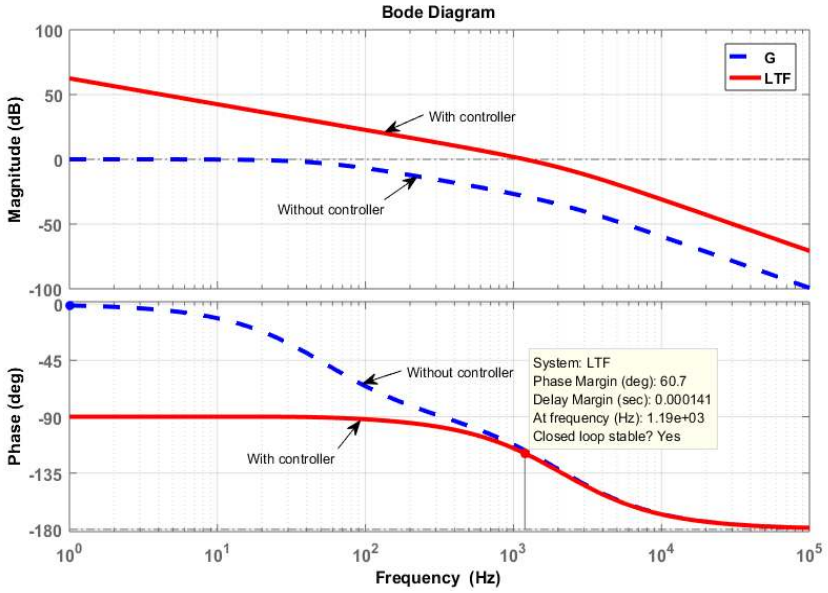

Figure 7. Bode plot of innermost inductor current control loop

4.3.3. Design of inner capacitor voltage control loop

The basic structural diagram of capacitor voltage control loop is presented in Figure 8. From the Figure 8, the open loop transfer function of the voltage control loop is given by (22).

$$G_{OL,V}(s) = \frac{\left(k_{p2}+\frac{k_{i2}}{s}\right)G_{CL,IC}(s)}{(1+1.5\,s\,T_s)(sC_f)} \quad (22)$$

Where, the digital delay is considered to be of 1.5 times the switching period T_s and $G_{CL,IC}(s)$ is the closed loop transfer function of the innermost inductor current loop.

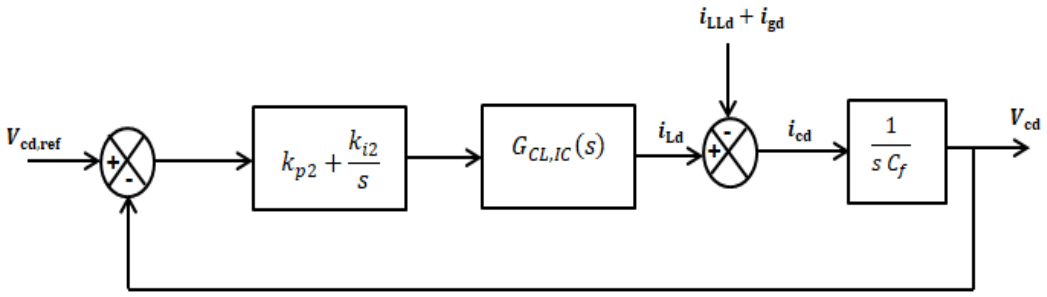

Figure 8. Control structure of capacitor voltage control loop

The bode plot of the voltage control loop with and without PI controller is shown in Figure 9. The controller is designed to attain cut off frequency of around 800 Hz and phase margin of 45°. The k_{p2} and k_{i2} values of the PI controller are about 0.063207 and 38.755.

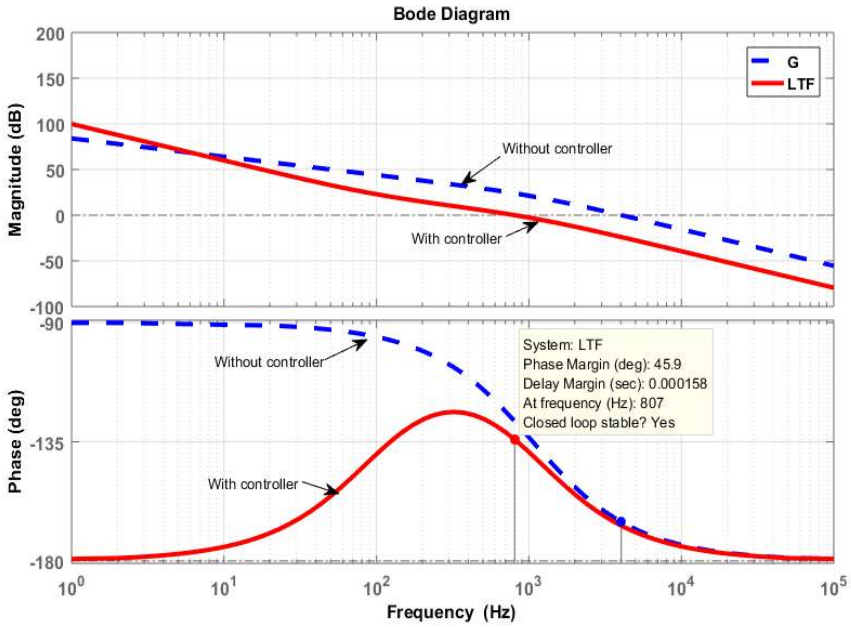

Figure 9. Bode plot of inner capacitor voltage control loop

4.3.4. Design of outer current control loop

The block diagram of outer current controller is given in Figure 10.

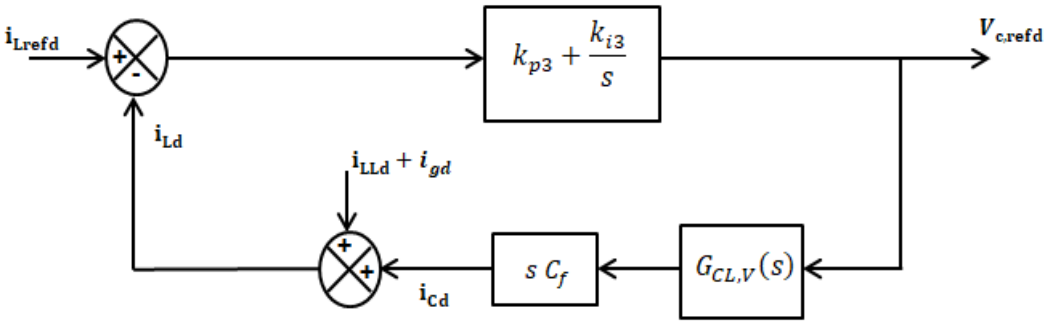

Figure 10. Control structure of outer current control loop

From the Figure 10, the open loop transfer function of the outer current control loop is given by (23).

$$G_{OL,OC}(s) = \left(k_{p3} + \frac{k_{i3}}{s}\right) G_{CL,V}(s)\ s\ C_f \quad (23)$$

where, $G_{CL,V}(s)$ is the closed loop transfer function of the voltage control loop. The bode plot of the open loop transfer function of outer current control loop with and without controller is shown in Figure 11. The values of k_{p3} and k_{i3} are found to be 0.25504 and 142570.

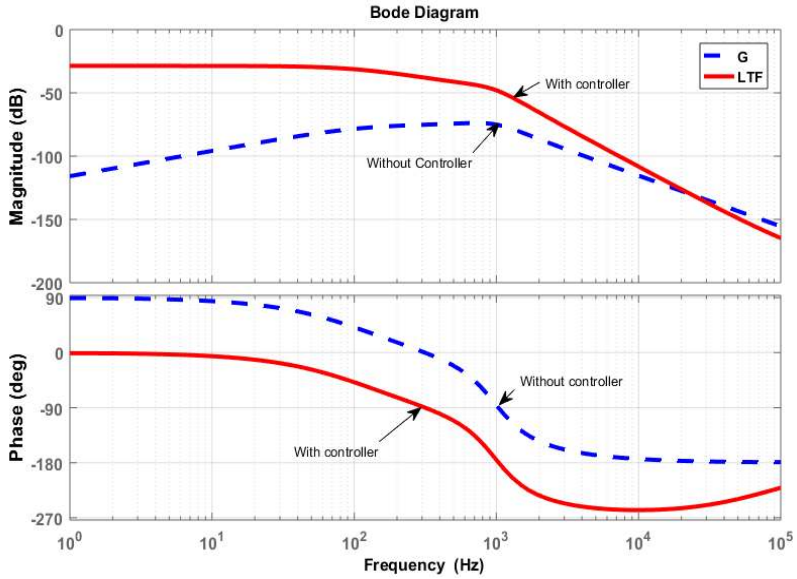

Figure 11. Bode plot of outer current control loop

5. ANALYSIS AND DESIGN OF CONTROL PARAMETERS OF INDIRECT CURRENT CONTROL BASED SEAMLESS TRANSFER

5.1. Design of innermost inductor current control loop

The block diagram of innermost inductor current loop is same as shown in Figure 6. The innermost inductor current loop is designed using control system designer tool box in MATLAB by considering a cut off frequency of 2000 Hz with a phase margin of around 41°. The bode plot of the system with and without the PI controller is shown in Figure 12. The k_{p1} and k_{i1} values of the PI controller are about 52.574 and 87583.

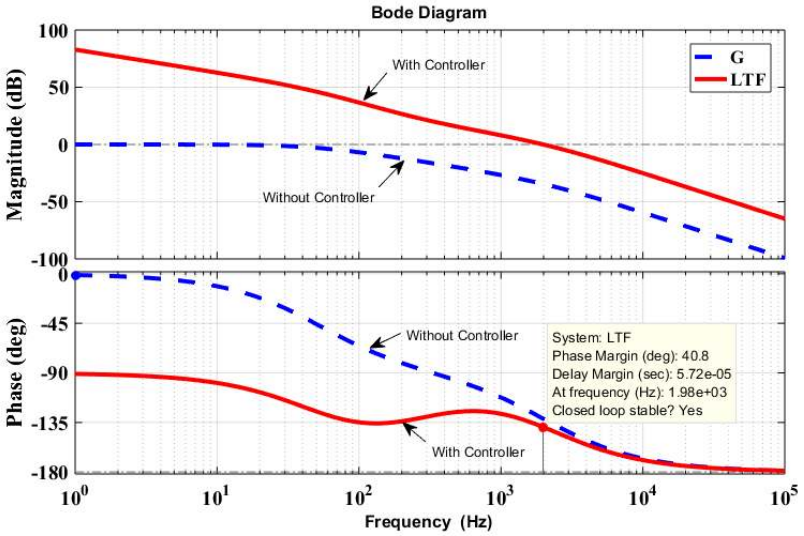

Figure 12. Bode plot of innermost inductor current control loop

5.2. Design of inner capacitor voltage control loop

The block diagram of inner capacitor voltage loop is same as that shown in Figure 8. The voltage loop is designed by considering a cut off frequency of 1000 Hz with a phase margin of around 21°. The bode plot of the system with and without the PI controller is shown in Figure 13. The k_{p2} and k_{i2} values of the PI controller are about 0.053285 and 128.83.

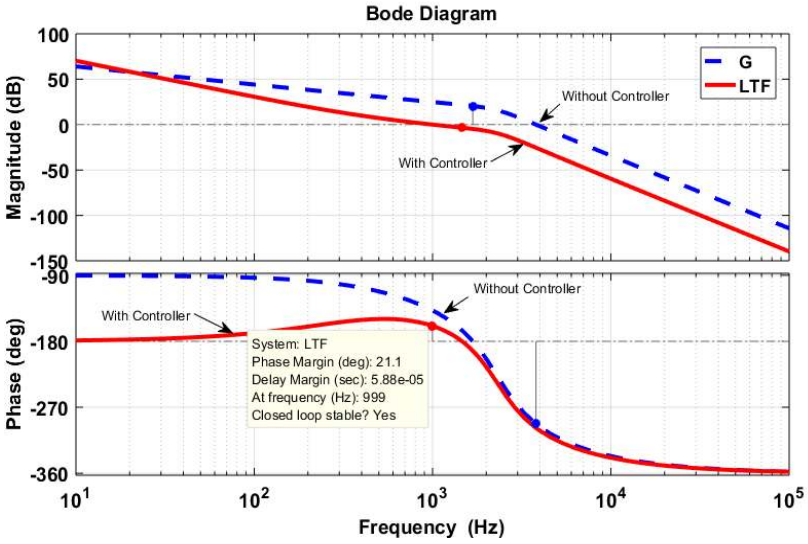

Figure 13. Bode plot of inner capacitor voltage control loop

5.3. Design of external grid current control loop

The block diagram of external grid current control loop is illustrated in Figure 14. The grid current is controlled by considering the gain of the inner loops as unity as the bandwidth of the inner voltage control loop is high. Design of the grid current controller is carried out by considering the cut off frequency to be 150 Hz and a phase margin of around 28°. The bode plot of the system with and without the PI controller is shown in Figure 15. The values of k_{p3} and k_{i3} are found to be 0.89949 and 2802.

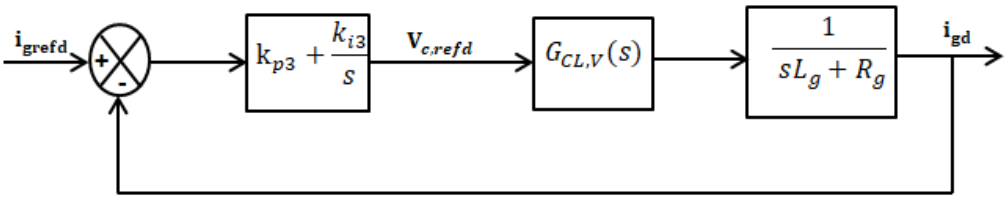

Figure 14. Block diagram of external grid current control loop

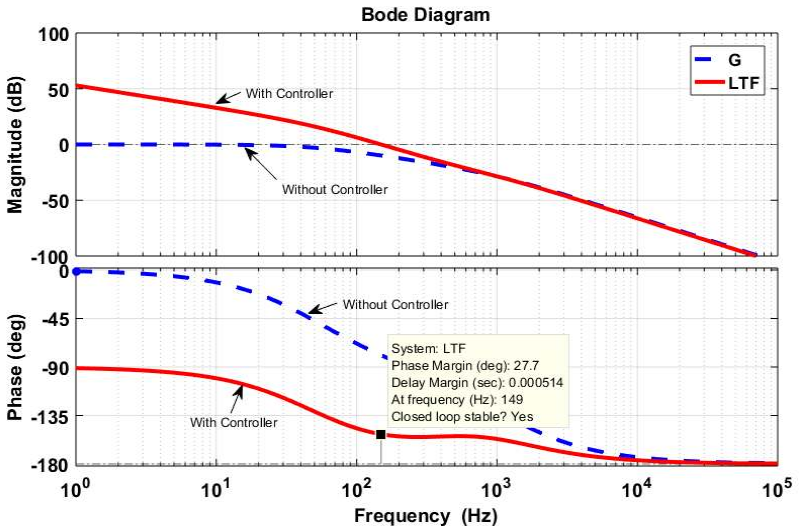

Figure 15. Bode plot of external grid current control loop

6. RESULTS AND DISCUSSION

The simulation studies have been carried out in MATLAB Simulink for the system shown in Figure 1. The parameters considered for the simulation studies are shown in Table 1 and Table 2.

Table 2. Parameters of the control system

Parameters	Symbol	Value
Maximum limit of the voltage in d axis	$V_{d,max}$	326.68 V
Minimum limit of the voltage in d axis	$V_{d,min}$	295.57 V
Maximum limit of the voltage in q axis	$V_{q,max}$	+ 0.05 V
Minimum limit of the voltage in q axis	$V_{q,min}$	- 0.05 V
Grid current reference in d axis	I_{grefd}	10 A
Grid current reference in q axis	I_{grefq}	0 A
Inductor current reference in d axis	I_{Lrefd}	20 A
Inductor current reference in q axis	I_{Lrefq}	0 A

6.1. Simulation results of output current based seamless transfer

Initially, MG operates under grid connected mode by considering the grid is working normally without any faults. MG is supplying the local load as well as the grid until the grid connected switch (S_g) is in closed position. Once fault occurs, at 0.2s, the grid connected switch is opened. Then switch in the inverter side (S_i) opens after detecting the islanding condition. At around 0.225 s, utility gets disconnected and the MG enters into islanding mode and feeds the local load within the specified voltage / frequency limits. The controllers that are designed ensures the reference current tracking and hence the inverter output (inductor) current keeps track of the reference (I_{Lrefd} and I_{Lrefq}).

The currents are drawn from the inverter for providing power to the load as well as the grid under grid connected condition. As the islanding happens at 0.225s, the grid current drops to zero and hence the inverter output current drops to a current which is demanded by the load. The simulation results of seamless transfer from grid connected to islanding mode are shown from Figure 16 to Figure 22. The inverter current in d axis is shown Figure 16, which is tracking the reference currents. At 0.225 s, the inductor current drops to 11 A, to supply the local loads. The inverter voltage and current waveforms are shown in Figure 17.

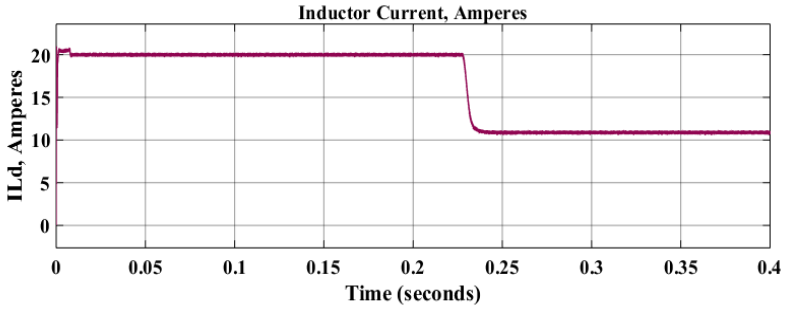

Figure 16. Inductor current tracking the reference currents

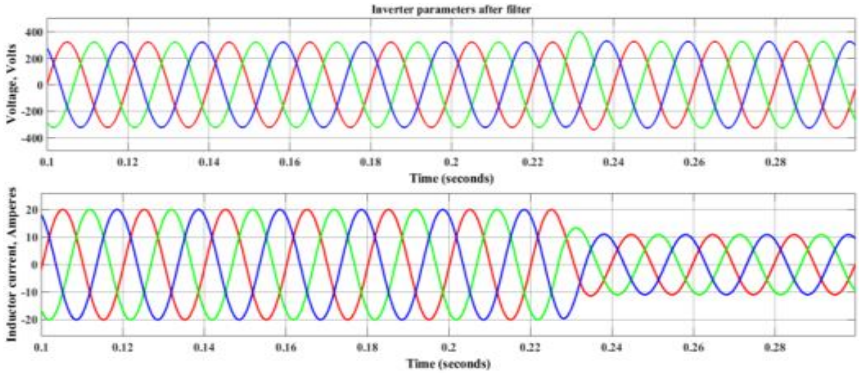

Figure 17. Inverter output voltage and current waveforms

The grid voltage and grid current waveforms are shown in Figure 18. The dq components of the capacitor voltage, waveforms of capacitor voltage and currents are shown in Figure 19 and Figure 20 respectively. The voltage across the load and the current drawn by the load are shown in Figure 21. Active and reactive power drawn by the load is shown in Figure 22. From the Figure 17, it is clear that during islanding, the voltage magnitude is within the limit and quality of voltage waveform is also good without any big transients and settles down quickly within a cycle time period.

The dynamic performance of the control strategy has been verified by changing the reference currents and the results are shown in Figure 23 and Figure 24. The inductor reference currents are set as 15 A from 0 to 0.1s and changes to 18A at 0.1s and to 20 A at 0.15s. At 0.225 s, the MG enters in to islanding mode and hence the inverter current drops and the inverter supplies the local load current of 11A.

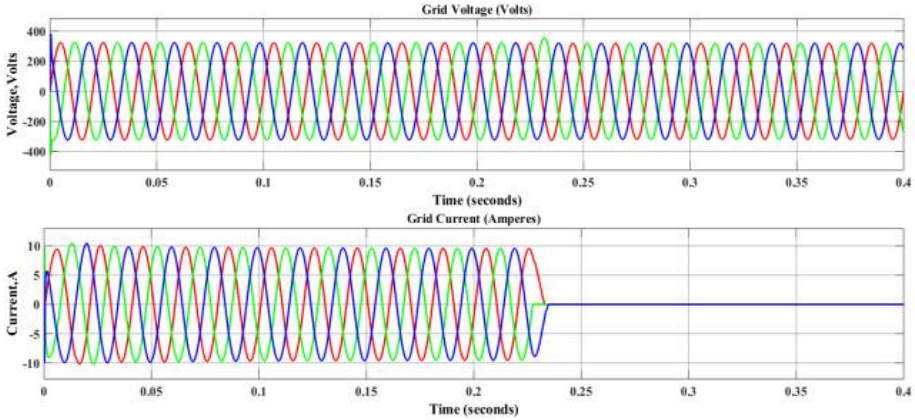

Figure 18. Grid voltage and grid current waveforms

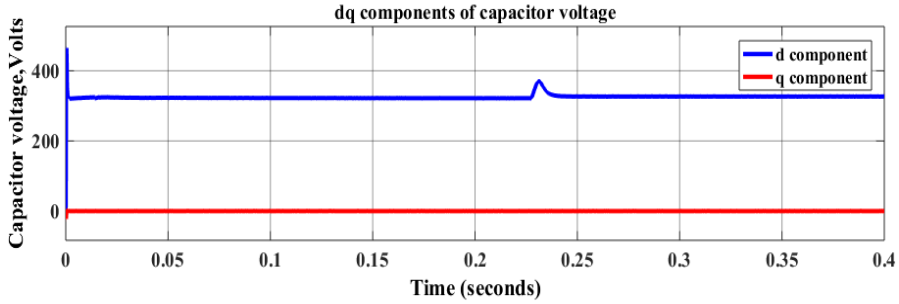

Figure 19. dq components of capacitor voltage

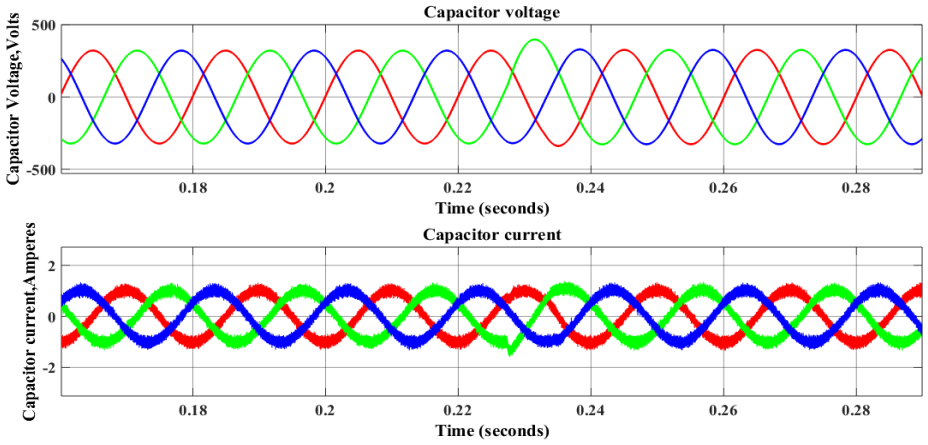

Figure 20. Capacitor voltage and capacitor current loop waveforms

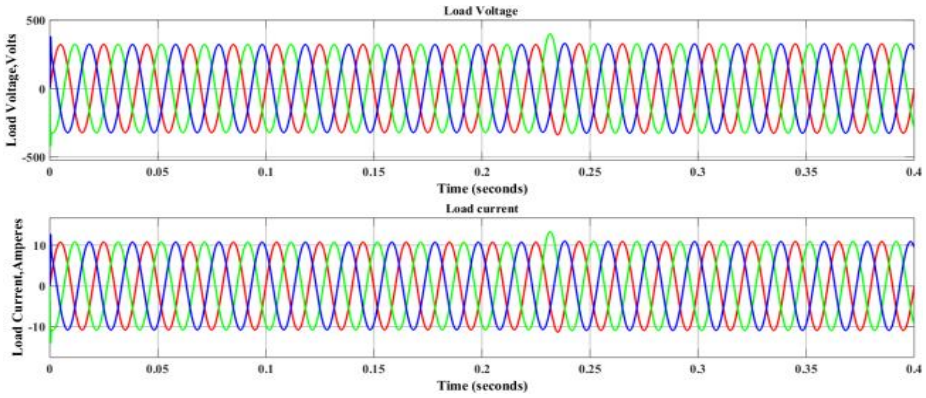

Figure 21. Load voltage and load current waveforms

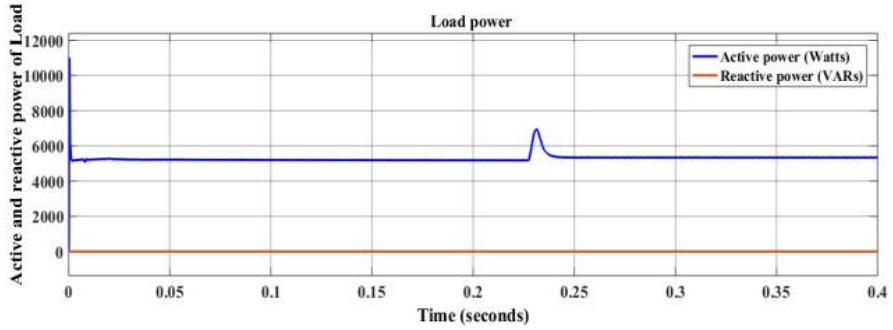

Figure 22. Active and reactive power of the local resistive load

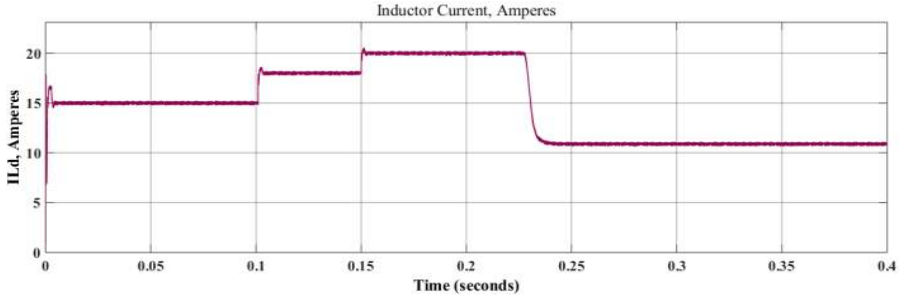

Figure 23. Inductor current under varying reference values

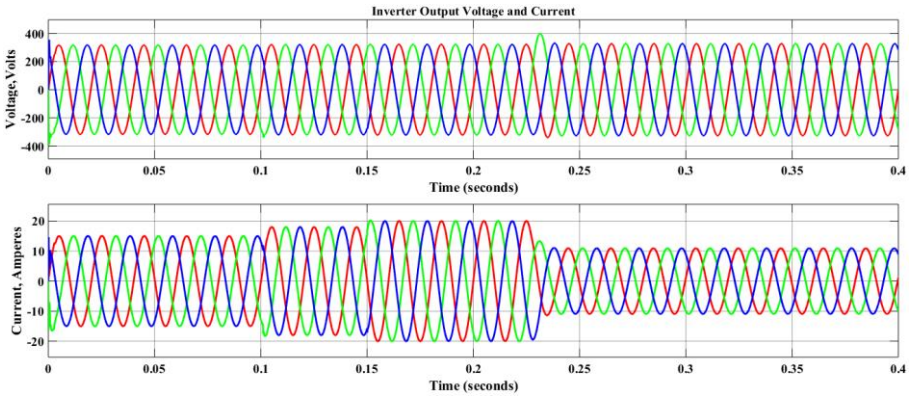

Figure 24. Inverter output voltage and current waveforms under varying reference currents

6.2. Simulation results of indirect grid current control based seamless transfer

Simulation studies have been carried out by considering that the system is initially grid connected and supplying power to the local load as well as feeding power to the utility grid. MG is moving to islanded mode when fault occurs in the grid side. The parameters of the system under study are same as shown in Table 1 and Table 2. At 0.35s fault occurs in the grid side and hence the grid connected system changes to standalone mode. The grid current reference considered is 10 A and the results are shown in Figure 25 to Figure 30. The tracking of the grid reference current is shown in Figure 25.

Comparing the results of the control strategies, the output current control strategy gives better dynamic response. From Figure 23 and Figure 25, it is very clear that the output current control strategy tracks the reference current faster within half cycle and without any transients whereas in the grid current control, transients takes place when the reference changes and also it takes around 2 to 3 cycles to settle down to the reference value.

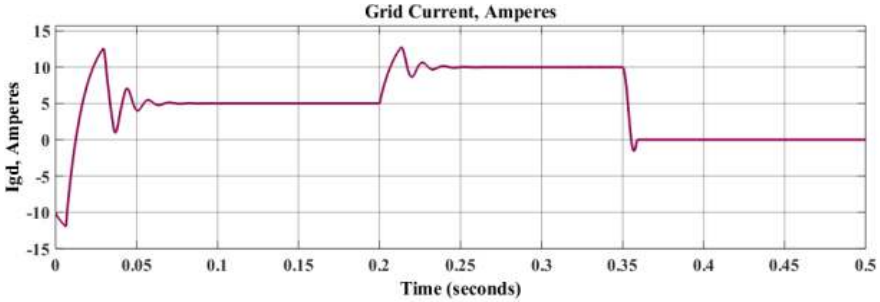

Figure 25. Grid current (I_{gd}) reference tracking

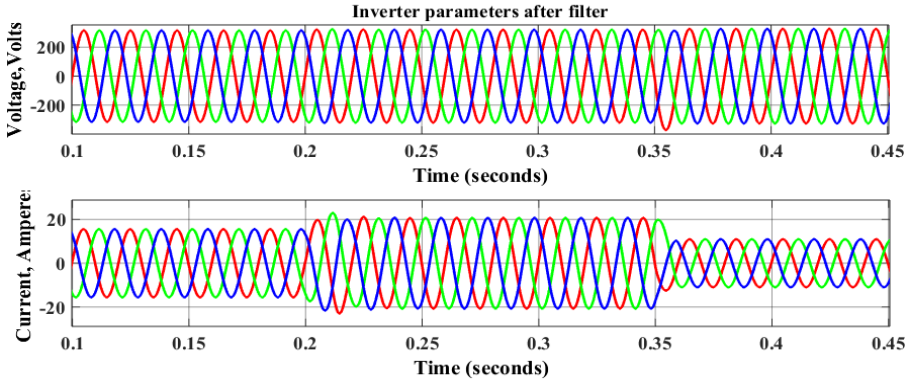

Figure 26. Inverter voltage and current waveforms

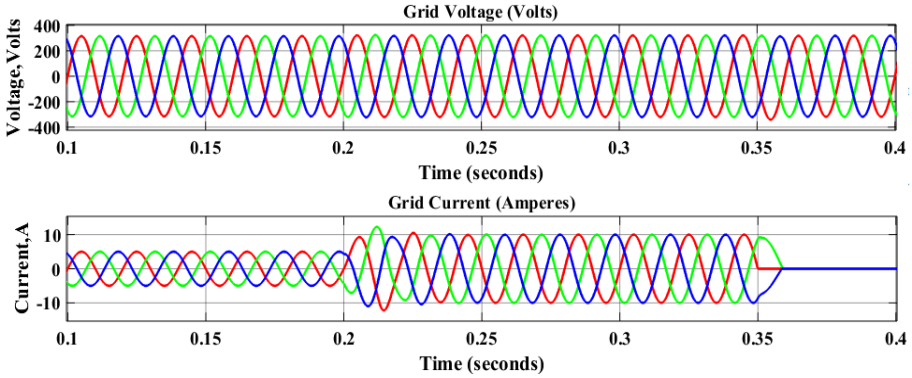

Figure 27. Grid voltage and grid current waveforms

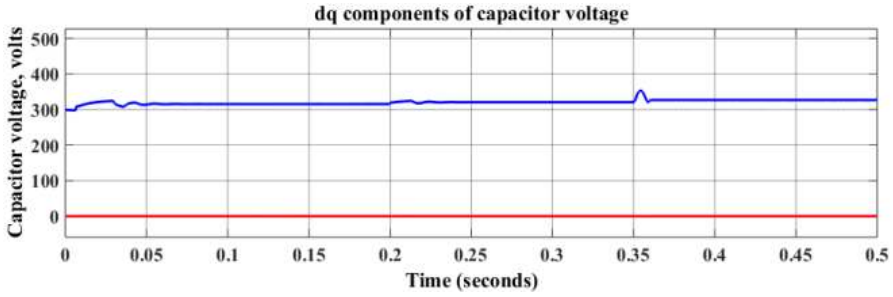

Figure 28. dq components of Capacitor voltage and current waveforms

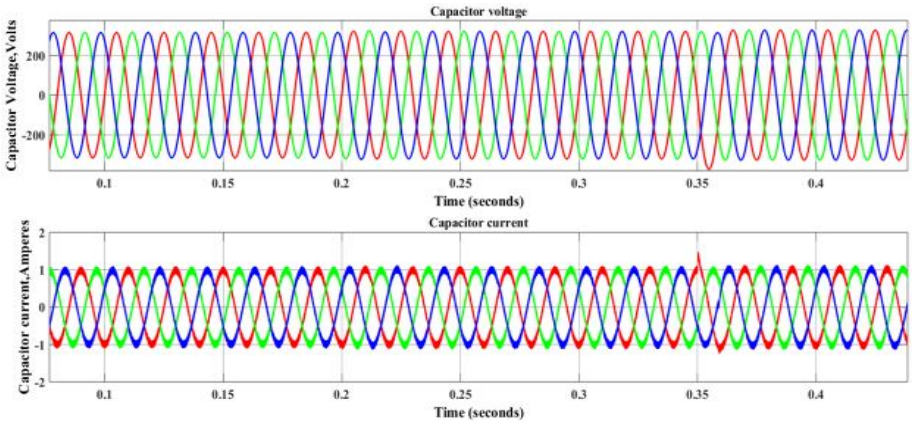

Figure 29. Capacitor voltage and current waveforms

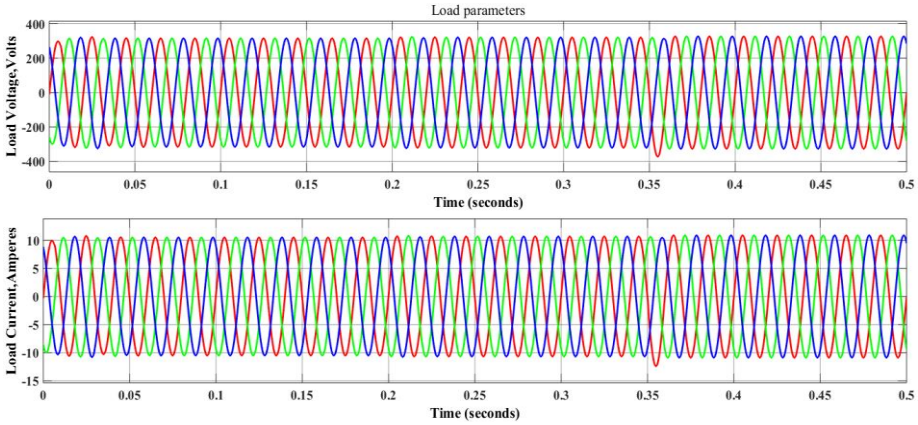

Figure 30. Load voltage and load current waveforms

7. CONCLUSION

This paper discusses about the control strategies for attaining seamless transfer between the grid connected and islanding modes of operation of a Microgrid system. Simulation studies have been carried out using both indirect current control strategy and output current control strategy for a grid connected microgrid system to achieve seamless transfer. The Simulation results demonstrate that the smooth transition is achieved from grid connected to islanding mode when the switch in the grid side is opened under faulty conditions. The design of control loop is also validated from the simulation results by considering the settling time and steady state error as the performance parameters. Simulation results demonstrate that when the changeover takes from grid connected to islanded mode, the transients in load voltage, inverter output current settle within 10ms.

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