Design and dSpace interfacing of current fed high gain dc to dc boost converter for low voltage applications

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Design and dSpace interfacing of current fed high gain dc to dc boost converter for low voltage applications

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Abstract. In this paper a current fed interleaved DC - DC boost converter which has an isolated topology and used for high voltage step up is proposed. A basic DC to DC boost converter converts uncontrolled DC voltage into controlled DC voltage of higher magnitude. Whereas this topology has the advantages of lower input current ripple, lesser output voltage, lesser stress on switches, faster transient response, improved reliability and much lesser electromagnetic emission over the conventional DC to DC boost converter. Most important benefit of this interleaved DC to DC boost converter is much higher efficiency. The input current is divided into two paths, substantially ohmic loss (I^2R) and inductor ac loss gets reduced and finally the system achieves much higher efficiency. With recent mandates on energy saving interleaved DC to DC boost converter may be used as a very powerful tool to maintain good power density keeping the input current manageable. Higher efficiency also allows higher switching frequency and as a result the topology becomes more compact and cost friendly. The proposed topology boosts 48v DC to 200 V DC .Switching frequency is 100 kHz and PSIM 9.1 Platform has been used for the simulation.

1. Introduction

Technology has redefined the luxury of our daily life. And with the development in technology the energy demand has also increased drastically. Probably it will take thousands of years to reproduce the amount of fossil fuels that we have used in last few decades. Unfortunately the amount of stored non-renewable energy is fixed and that's why it is high time to focus more towards the renewable energy sources. Government of different countries are taking effective measures to encourage their fellow citizens to use different renewable energy sources. As per India is considered the government has targeted to reach a renewable Power capacity of 175 GW by 2022 .But the main problem with the renewable energy is it's low output voltage[1-4]. So it is necessary to have a converter between the source and the load that will give boosted output voltage. But conventional boost converters cannot give much higher voltage boost due to the presence of parasitic components. So it is required to install bulk input filters to mitigate huge input current ripple[5]. But this reduces the durability of the source and finally affects the overall performance. These problems does not come into account in our proposed topology Interleaved DC to DC converter reduces input side current ripple & output side voltage ripple and gives much higher efficiency than the conventional boost converters[6].

2. Circuit Topology

The proposed converter consists of two legs in the input side. The legs are interleaved boost converter fashion. It aids to minimize the ripple current in the source side [7,8]. In the output side two uncontrolled bridge converter circuits are presented, to minimize the voltage ripples in the output voltage [9, 10].

The input and output circuits are isolated through high frequency 1:2 step up isolated with the aid of transformers. The inductors are used here is a high frequency ferrite amorphous core inductors are used, to minimize the internal inductance resistance. It will minimize the inductor internal losses.

The metalized polypropylene capacitors are used in output stages, it has low internal resistance, to minimize the internal drop due to capacitor under loading conditions. The circuit topology has been given is shown in Figure 1.

The two legs are connected in parallel with 180 degree phase shift between them with inductance L_{INPUT1} & L_{INPUT2} are present to reduce the high inrush current respectively. During the conduction of all the switches, $L_{leakagek1}$ and $L_{leakagek2}$ keeps the continuous flow of current in the respective circuit.

The use of transformer results in the isolation between low voltage on input and high voltage on output side. For reduction of low input and output ripple, the filter capacitors C_1 and C_2 are being installed on the output side of the system. Low ripple current provides the stability of the system and increases the working efficiency of the system.

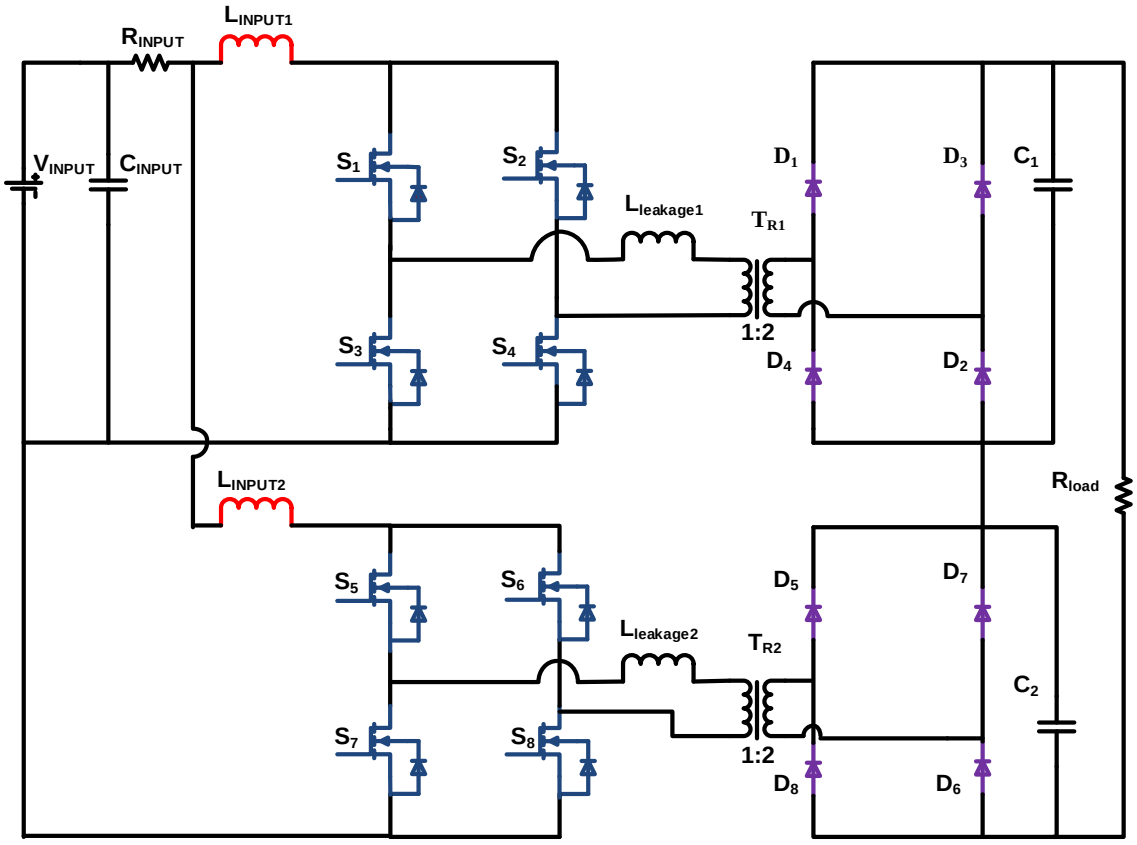

Figure 1. Circuit topology

3. Different modes of operation

The converter operation has three modes. The respective modes of operation are given in the subsequent sessions.

3.1. Mode I operation

In first Mode, the two respective switches S_1 and S_4 works in upper bridge inverter. As these respective inverters are having 180 degree phase difference, the second sets two of switches S_5 and S_8 will be working at 180 degree phase shift which makes D_1, D_2, D_7, and D_8 to be forward biased and D_3, D_4, D_5, and D_6 to be reversed biased. The path of current will be from transformer 1 – D_1 – R_{Load} – D_8 - transformer 2 – D_7 - D_2 – transformer no 1.The necessary diagram has been shown below Figure 2.

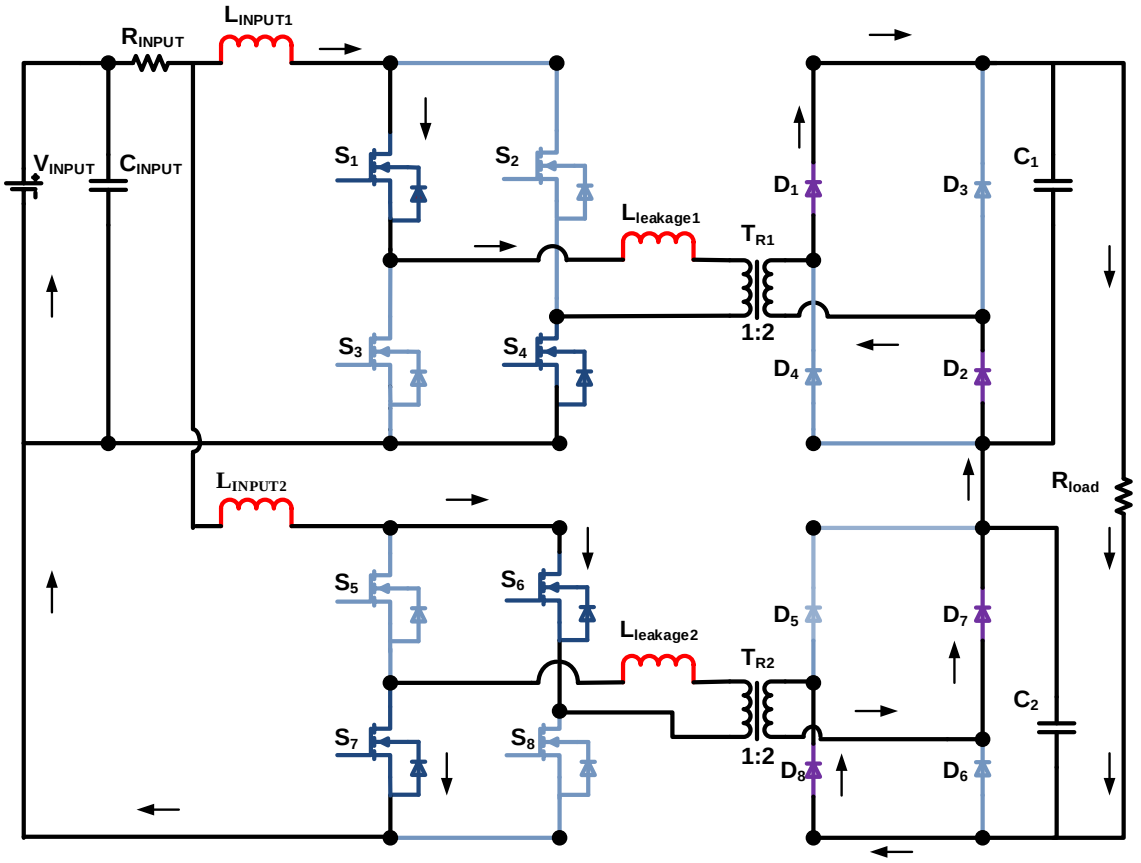

Figure 2. Circuit diagram during Mode I operation

3.2. Mode II operation

The switches of both cells are conducting. During this period the two source inductances L_{INPUT1} and L_{INPUT2} gets charged as a result of this the output voltage is equal to zero thereby creating finite current which is observed due to the presence of $L_{leakage1}$ and $L_{leakage2}$. The circuit is shown below in Figure 3.

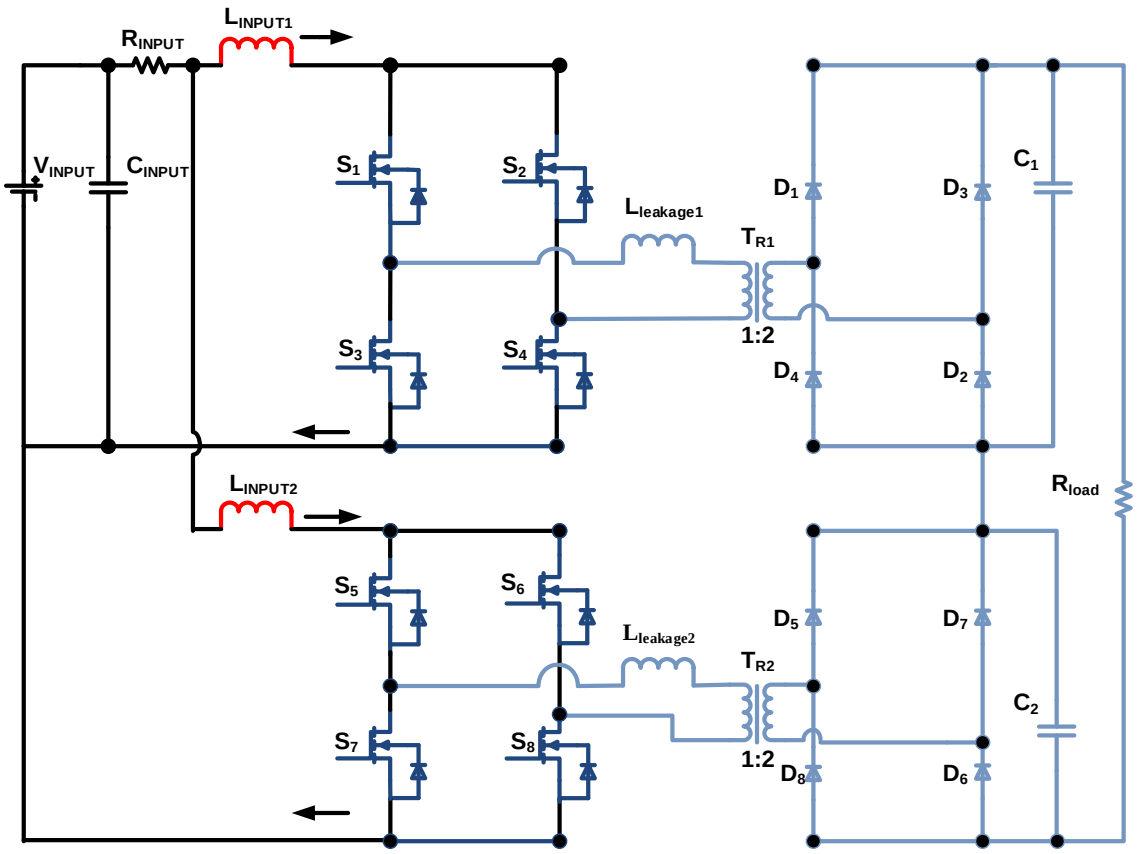

Figure 3. Circuit diagram during Mode I operation

3.3. Mode III operation

During this mode there is a conduction of necessary four switches simultaneously. The switches S_3, S_4 and S_5, S_6 works simultaneously. The diodes D_3, D_4, D_5, D_6 will be forward biased and D_1, D_2, D_7, D_8 will be biased reversely due to the transformer voltage. The current will flow from transformer 1 D_3 – R_{Load} – D_6 - transformer 2 – D_5 - D_4 – transformer 1. The figure is given below Figure 4.

4. Design specification

The project design specification is given in the Table 1.

Table 1. Design specification

Parameters	Values
Boost Inductors (L_{input1},L_{input2})	1000 µH
Transformer Trans-ratio	1:2
Transformer Leakage Inductance (L_{lk1},L_{lk2})	0.1 µH
Input capacitor(C_{input})	0.1 µF
filter Capacitors(C_1,C_2)	20 µF

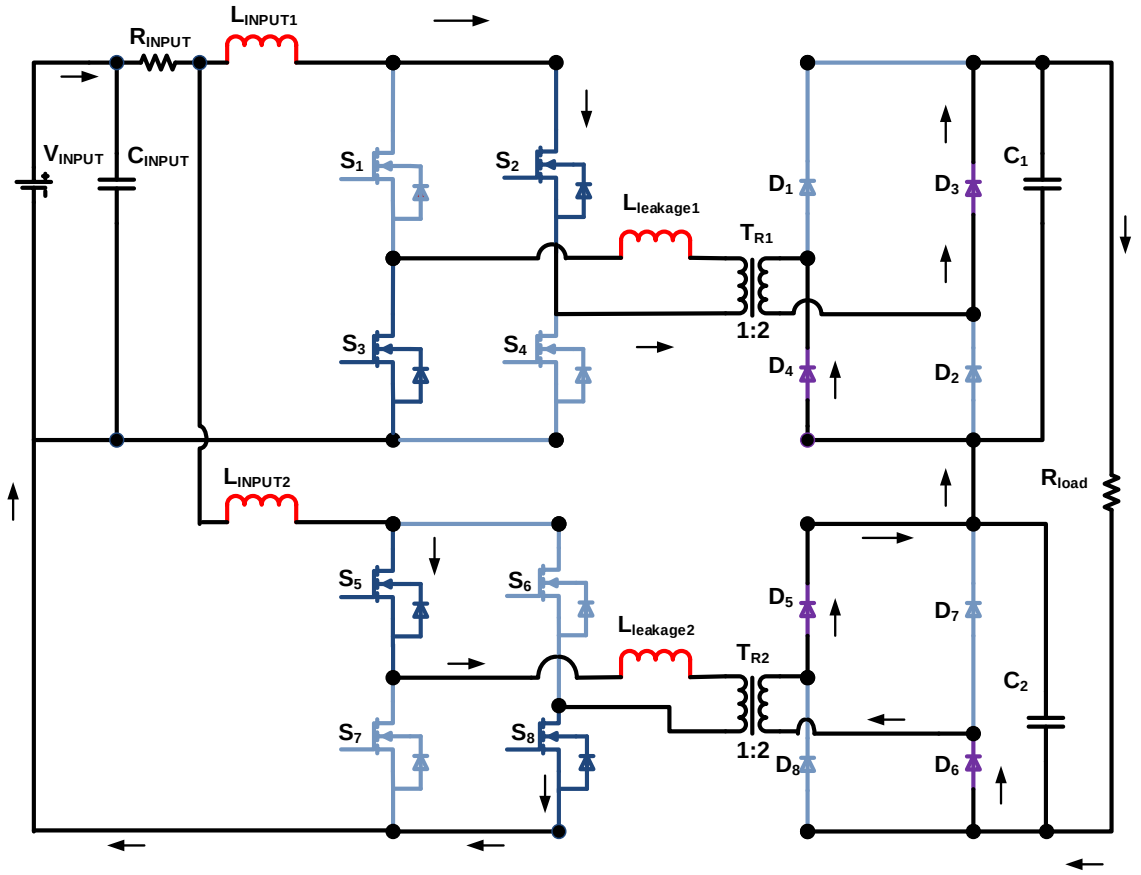

Figure 4. Circuit diagram during Mode I operation

5. Results

The proposed converter is simulated with the PSIM software and prototype hardware implemented in the hardware. The firing pulse for the switches are generated with the help of dSpace 1104 real time hardware kit. The pulses are isolated with the help of opto-isolater circuit.

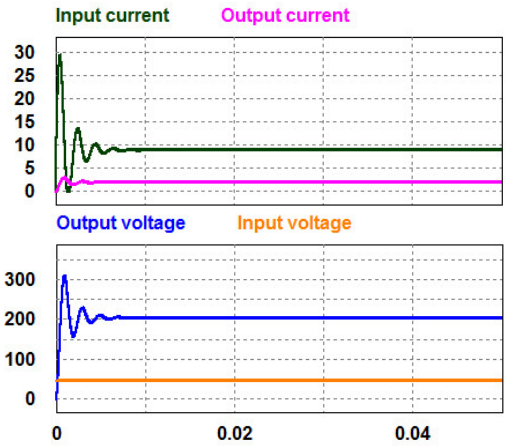

Figure 5(a). Simulation results of V_{in}, I_{in}, V_O, I_O

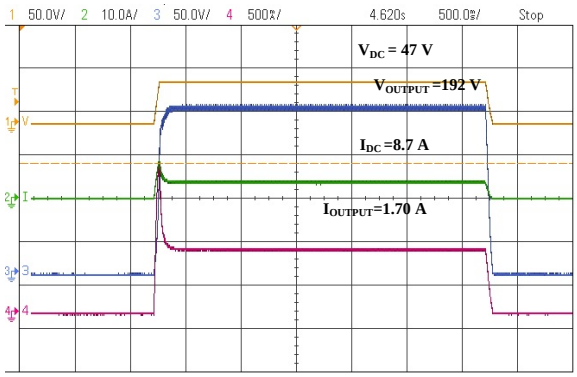

Figure 5(b). Hardware results of V_{in}, I_{in}, V_O, I_O

The detailed results obtained from the proposed converter is shown in Figure 5. The Figure 5(a) shows the simulation results obtained at input and output side. The Figure 5(b) depicts the hardware results taken at the input and output. The results are almost matching with minimum ripple in the input and output.

The Figure 6(a) shows the simulation results obtained at input side inductor currents. The Figure 6(b) depicts the hardware results taken in the input inductor currents.

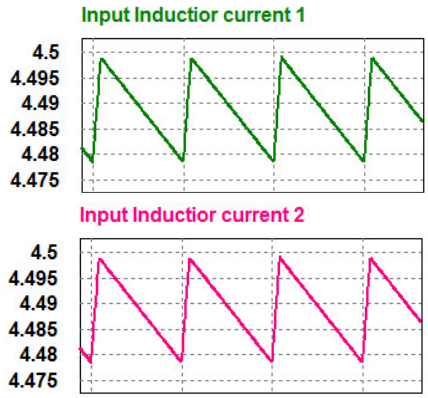

Figure 6(a). Simulation results of I_{input1}, I_{input2}

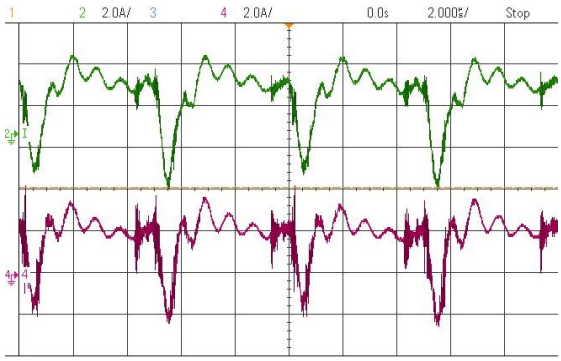

Figure 6(b). Hardware results of I_{input1}, I_{input2}

The Figure 7(a) shows the simulation results obtained at transformer 1 primary and secondary voltages. The turns ratio is 1:2, the 48 volts is supplied to the input side to the converter, output voltage at the secondary side becomes 96 V. The Figure 7(b) depicts the hardware voltage results taken at the transformer 1 input and output side.

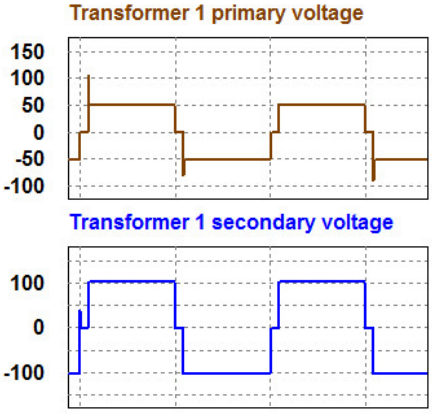

Figure 7(a). Simulation results of V_{pri1}, V_{sec1}

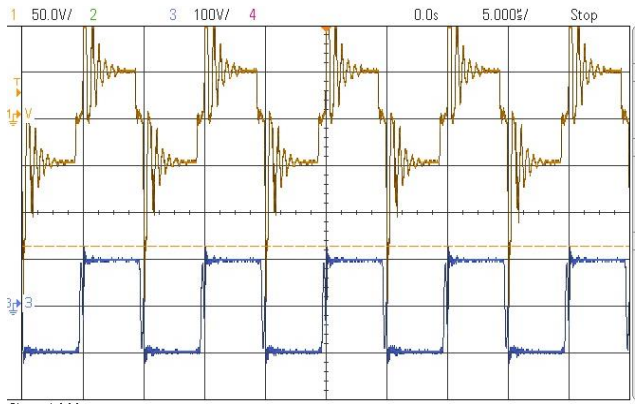

Figure 7(b). Hardware results of V_{pri1}, V_{sec1}

The Figure 8(a) shows the hardware results obtained at transformer 1 primary voltage and current. The Figure 8(b) depicts the hardware voltage results taken at the transformer 1 secondary voltage and current.

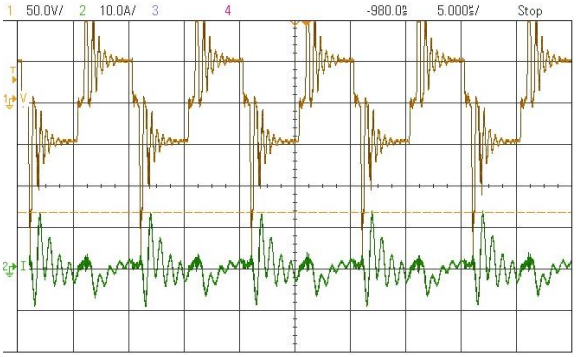

Figure 8(a). Hardware results of V_{pri1}, I_{pri1}

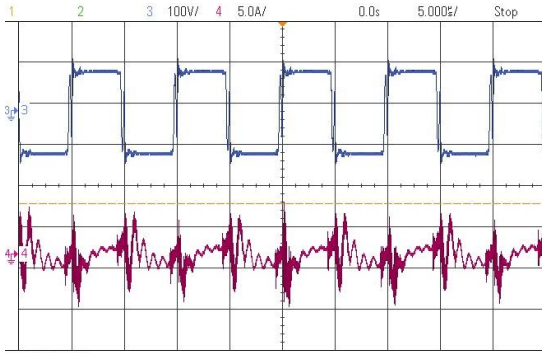

Figure 8(b). Hardware results of V_{sec1}, I_{sec2}

6. Conclusion

A modified interleaved DC to DC boost converter topology is been proposed in this paper. The model is designed for low voltage applications which need very steady mode of operation and high efficiency. In this topology, output Voltage gain is almost Four times the input voltage. The result is tested in both software and hardware. We found both the results have high efficiency, low input current ripple and low output side voltage ripple.

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