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Design and Implementation of Soft Switched High Gain Current Fed Full Bridge DC-DC Converter for Fuel Cell Applications

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Abstract

This paper proposes the analysis and design of new current fed full bridge high gain isolated dc-dc converter for fuel cell application. The proposed converter uses voltage multiplier cells on the secondary side. The objective of the proposed converter is to generate DC link voltage for three phase grid from fuel cell. Current fed Converter reduces the input current ripple at the fuel cell input. The converter utilizes the energy stored in the transformer leakage and parasitic capacitance to maintain zero-current-switching (ZCS) over wide range. Soft switching permits higher switching frequency operation, reducing the size, weight and cost of the magnetic components and improve the converter efficiency. A new design method of half-wave Cockcroft–Walton Voltage Multiplier (H-W C-W VM) that lays on the calculation of the optimal number of stages, which is necessary to produce the desired output voltage with the minimum total capacitance value, is also presented. The operating frequency of the converter is 100 kHz. The Analysis, simulation and experimental results of the proposed converter are presented. The proposed converter with three stage voltage multiplier is simulated for two different cases full load and half load conditions and the results were analysed. The hardware model for an input voltage of 30V and input current of 5 Amps was designed, the output from the inverter is 40 V and output from the voltage multiplier of three stages is 240 V and 0.6 Amps.

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Keywords: Fuel cells; Zero-Current switching; Current fed DC-DC converter; Half Wave Cockcroft- Walton

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1. Introduction

The astounding trends in power converters instigated analyzing the subject. A continuous current capacitance commutated mode boost CSI provides a continuous input current and regulated output current [1],[2],[8]. A voltage multiplier circuit with inbuilt protection provides voltage scaling with high gain [4]. Moreover, soft switching characteristics of proposed converter reduce switching loss of active power switches and rises conversion efficiency. The objective of this project is to design an intermediate converter block for current sources like fuel cells and load. The source current is high as compared with the source power and contains ripples [7]. Hence CCM- CSI is used to regulate the current and the output voltage gain is increased using HW- CW Voltage Multiplier [5]. Output Voltage can be multiplied to many stages without changing the turn ratio of the transformer hereby we reduce the number of turns of the transformer [5]. High frequency transformer acts as the electrical barrier between source and load [8]. The size of the power supply is reduced by increasing the frequency of operation thus boosting up the power density of the converter system [5],[9]. High frequency of operation reduces the number of turns of the transformer and there by cuts down on its size. The core losses are reduced considerably.

Environmental concerns about global warming, fossil fuel exhaustion and the need to reduce carbon dioxide emissions provided the stimulus to seek renewable energy sources. Fuel cells are one of the most promising technologies to solve the aforementioned environmental concerns [3]. Interest in fuel cell systems arises not only because of their essentially zero pollution emission, but also because of their energy conversion efficiency, which can be higher than that of a conventional power plant [3]. Additionally, thermal energy generated as the by-product of fuel cell operation can be used for heating. Since the power density of a fuel cell is higher than other renewable energies, it can be widely used for grid- connected generation, vehicles, and portable applications. Generally, the fuel cell stack has a low voltage and its current ripple should be small [6]. Therefore, a high step-up dc–dc converter with high voltage conversion ratio, low input-current ripple, and high efficiency is required. Voltage-fed converters are often used in the step-up dc–dc converter for fuel cells. However, these voltage-fed converters may not be optimal due to large input-current ripple. Reducing the input-current ripple in the voltage-fed converter requires an additional LC filter across the fuel cell stack, which lowers the power efficiency [11]. Also, a high turn's ratio between the primary and secondary sides of the high-frequency transformer is required. However, current-fed converters decrease the input-current ripple by using an inductor. Current-fed converters have advantages such as high voltage conversion ratio, low input-current ripple, and low conduction loss of switches. Several current-fed converters have been developed such as a current-fed push–pull converter a current- fed full bridge converter and a current-fed half-bridge converter. A conventional current-fed full-bridge converter has the inverter function [10].The objectives of this paper are to present the analysis and design of the current-fed full-bridge dc/dc converter with voltage multiplier cells for fuel cell applications. Fuel cell stack voltage is varying with load. Hence Fuel cell stacks should give wide variation in their output dc voltage and power transfer capacity by characteristics. The converter therefore, has to offer wide regulation range. The proposed converter is simulated for full load and half load condition. This paper presents the converter analysis for three possible operating conditions and discussed next. The paper is presented as follow: Steady-state operation and analysis of the converter are described in Section II. Converter design procedure and simulation results of the proposed converter are presented in Section III. The hardware results are illustrated in Section IV. The proposed converter is shown in Fig.1.

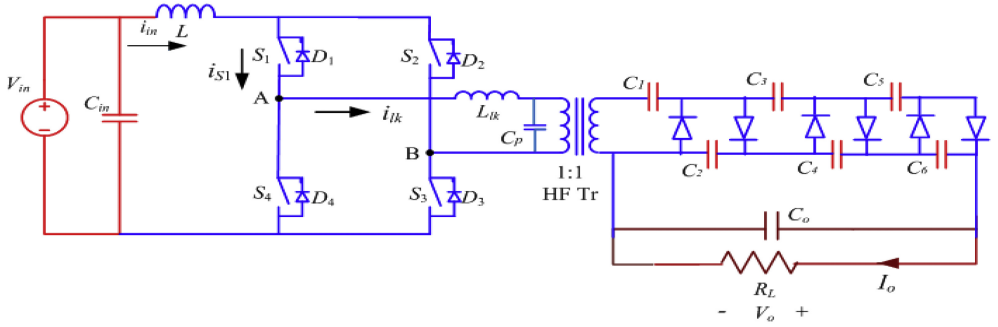

Fig.1. The proposed CSI fed converter with 3 stage voltage multiplier.

2. Operation and Steady State Analysis

In this section, steady-state operation and analysis of the proposed converter have been explained. Main focus is on the proposed front-end dc–dc converter. Since the secondary of the proposed converter is voltage multiplier, it will multiply the transformer secondary voltage. Hence in the analysis only input side is explained. The theoretical waveforms are shown in Fig.2

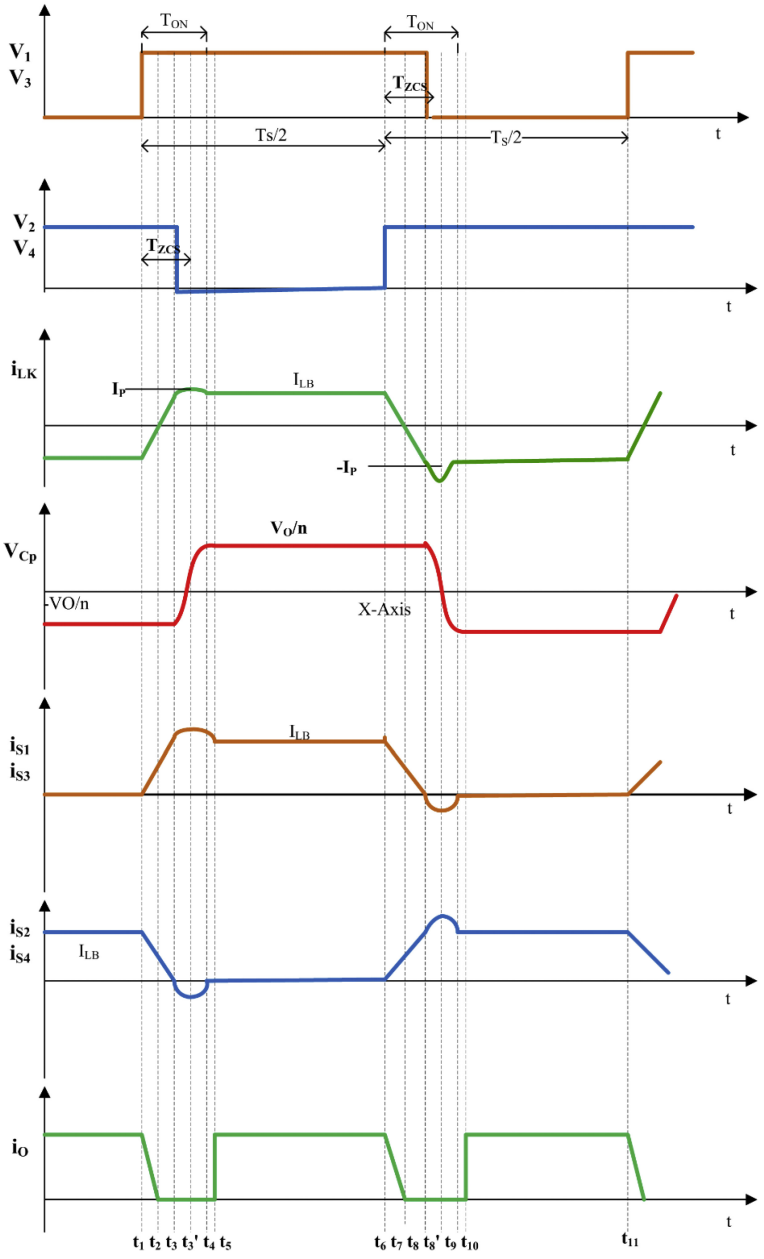

Fig. 2 Theoretical waveforms

Interval 1 ($t_1 < t < t_2$)

At t = t1, switches S1 and S3 are turned on. All four main switches S1-S4 are ON. The operation of this mode is shown in Fig. 3a. The energy stored in Lk is transferred to the output load and inductor current i_{Lk} is increased linearly with the slope of Vo/ L_k. There are two paths for $-i_{lk}$ to flow .The switches S_1 and S_3 turn on, current in them starts increasing and current in S_2 and S_4 decreases. The switches S1 and S3 are turned on with ZCS due to resonant inductor L_k. The corresponding equations are shown below. This mode ends as the current in $L_k$reaches zero. Current i_{lk} increases from $-I_{lk}$ to zero in time t_2-t_1.

$$i_{Lk} = \frac{V_p}{L_k}(t - t_1) - I_{Ls} \quad (1)$$

$$i_{s1} = i_{s3} = \frac{1}{2}(I_{Ls} - (-i_{Lk}(t))) \quad (2)$$

$$i_{s2} = i_{s4} = \frac{1}{2}(I_{Ls} + (-i_{Lk}(t))) \quad (3)$$

At $t=t_2$, $i_{Lk}=0$ and thus

$$(t_2 - t_1) = \frac{I_{Ls}L_k}{V_p} \quad (4)$$

Interval 2 ($t_2 < t < t_3$)

Now the load is disconnected from the source. The operation of this mode is shown in Fig. 3b.During this mode the capacitor C_p starts losing its energy through the inductor and thus charges the inductor. The polarity across inductor remains the same. Also, due to this resonance between the leakage inductance $L_k$and capacitor C_p, current through switches S_2 and S_4 decreases further whereas current increases in the switches S_1 and S_3. Mode 2 ends as the current in switches S_2 and S_4 reach zero and hence they are switched off with Zero Current Switching i.e. attaining zero current just before attaining the their blocking voltage. Let resonant frequency be ω_r and the characteristic impedance be Z_r. When $i_{s2} = i_{s4}=0$, $i_{Lk}= i_{Ls}$ and hence it becomes the boundary condition.

$$\omega_r = \frac{1}{\sqrt{L_k C_p}} \quad (5)$$

$$Z_r = \sqrt{\frac{L_k}{C_p}} \quad (6)$$

$$i_{s1} = i_{s3} = \frac{1}{2}(I_{Ls} + i_{Lk}(t)) \quad (7)$$

$$i_{s2} = i_{s4} = \frac{1}{2}(I_{Ls} - i_{Lk}(t)) \quad (8)$$

$$i_{Lk}(t) = \frac{V_p}{Z_r}(\sin(\omega_r(t - t_2))) \quad (9)$$

At $t=t_3$, $i_{Lk}(t)=I_{Ls}$

$$(t_3 - t_2) = \frac{1}{\omega_r}\sin^{-1}\left(\frac{I_{Ls}Z_r}{V_p}\right) \quad (10)$$

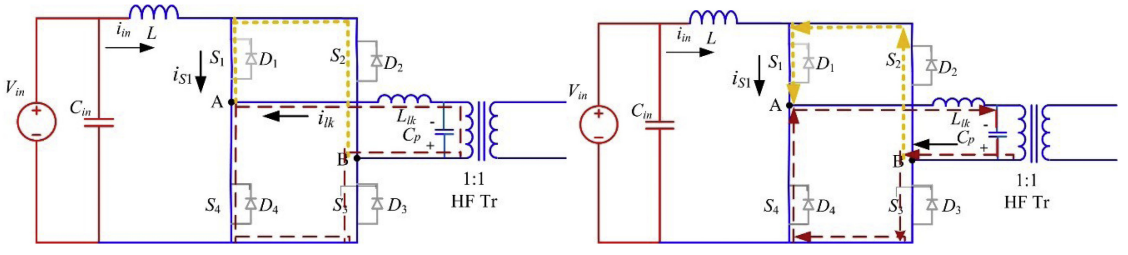

Fig. 3(a) Interval 1; Fig. 3(b) Interval 2

Interval 3($t_3 < t < t_4$)

Now, in mode 3 S_2 and S_4 are already off, but body diodes D_2 and D_4 are on and also S_1 and S_3 are on. The operation of this mode is shown in Fig. 3c.In this mode Capacitor $C_p$completely loses its energy to inductor $L_k$through the paths S_3 - D_4 and D_2 – S_1 respectively. A small increase in the value of i_{Lk}, i_{s1} and i_{s2} is observed and their value is greater than $+I_{Ls}$. Voltage across capacitor C_p becomes zero. To achieve ZCS this small increase in the value of current has to be observed. Let I_{Lk} reach I_P at $t=t_4$.

$$I_P = |i_{Lk}(t)|_{max} = \frac{V_P}{Z_r} \geq I_{Ls} \tag{11}$$

Load is still disconnected from source; no active power is transferred from the source to the load.

Interval 4($t_4 < t < t_5$)

The operation of this mode is shown in Fig. 3d.To maintain current across $L_k$continuous, $L_k$reverses its polarity and now starts discharging through the capacitor C_p. Mode 4 is similar to Mode 2 and Mode 3. Resonance still continues in this mode. Wheni_{Lk}becomes I_{Ls}, resonant period ends and body diodes D_2 and D_4 turn off.

$$\omega_r(t_5 - t_2) = \sin^{-1}\left(\frac{I_{Ls}Z_r}{V_P}\right)\left(\frac{\pi}{2} < \omega_r(t_5 - t_2) < \pi\right) \tag{12}$$

$$\omega_r(t_5 - t_2) + \omega_r(t_3 - t_2) = \pi \tag{13}$$

Interval 5 ($t_5 < t < t_6$)

The duration of this mode is very small. The operation of this mode is shown in Fig. 3e.In this S_1 and S_3 are on and I_{Lk} has settled to I_{Ls}. In this mode $C_p$is charged further by the input voltage and I_{Ls} to a value such that it starts floating again. $C_p$will again get connected and will dissipate energy now during the resonance period which will occur during the ZCS of S_1 and S_3.

$$i_{Lk}(t) = I_{Ls} \tag{14}$$

$$V_{Cp} = -V_p \cos\left(\omega_r(t_5 - t_2)\right) + \frac{I_{Ls}}{C_p}(t - t_5) \tag{15}$$

$$i_{s1}(t) = i_{s3}(t) = I_{Ls} \tag{16}$$

$$i_{s2}(t) = i_{s4}(t) = 0 \tag{17}$$

At $t=t_6$ V_{Cp} reaches V_p and the load is now connected to the source side.

Interval 6 ($t_6 < t < t_7$)

The operation of this mode is shown in Fig. 3f.S_1 and S_3 are in ON state during this mode of operation. Load is connected to the source and active power transfer from the source to load through the half wave Cockcroft Walton voltage multiplier circuit takes place. $V_{Cp}$is clamped to $V_p$and is in the floating state during this mode.

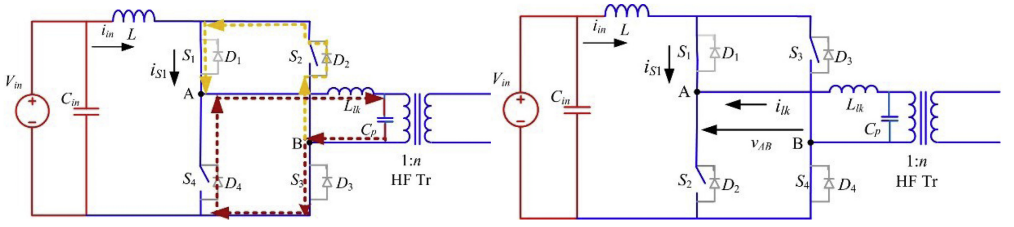

Fig. 3(c) Interval 3; Fig. 3(d) Interval 4

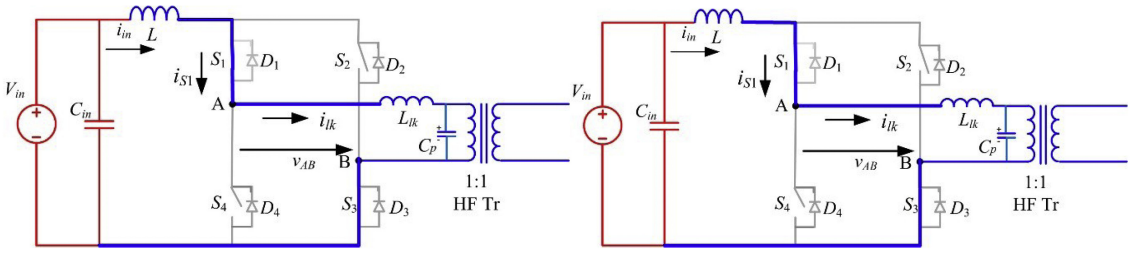

Fig. 3(e) Interval 5; Fig. 3(f) Interval 6.

3. Design & Simulation

Four different ways (cases) to design an H-W C-W VM can be considered [5], [12]:

Case 1:$C_{2i} = C_{2i-1} = C$ (the classical case where all capacitors are equal, analyzed by many authors).
Case 2:$C_1 = 2C$ and $C_{2i} = C_{2i-1} = C$ for i = 1 (case often found in the bibliography).
Case 3:$C_{2i} = C2_{i-1} = (n + 1 - i)C$.
Case 4:$C_{2i} = (n + 1 - i)C$ and $C_{2i-1} = (n + 1 - i)2C$.

Wherei is the number of every stage and C is the capacitance of the last stage, defined as base capacitance. C_{tot} is the sum of all capacitances, ΔVo is the voltage drop, δVo is the voltage ripple and X isthe voltage gain. Case 3 is identified as the optimal design for the multiplier and the design equations for case 3 are given below.

$$X = 2n - \frac{g}{2fCtot}[\, n^2(n+1)\,(2n+1)\,] \tag{18}$$

$$\frac{\Delta Vo}{Epk} = \frac{g}{fCtot}[\, n^3(n+1)\,] = \frac{g}{fCtot} A_{C3}(n) \tag{19}$$

$$\frac{\delta Vo}{Epk} = \frac{g}{fCtot}[\, n^2(n+1)\,] = \frac{g}{fCtot} B_{C3}(n) \tag{20}$$

$$C_{tot} = 2\sum_{i=1}^{n}[(n + 1 - i)C] = 2C\sum_{i=1}^{n}(i) = n(n+1)C \tag{21}$$

The proposed current-fed, full bridge isolated DC-DC converter is simulated in ORCAD 9.2 software and the results are interpreted in this section. Each case of the operation is simulated and simulated results for the both cases areanalysed individually. Fig 4 shows the proposed converter circuit simulated in ORCAD software for full load.

CASE-1:

This condition is observed for full load which is obtained at low voltage at V_{in}= 30V for 1000 Watts. The input voltage, switch pulses, voltage across the primary and secondary of the transformer, and the output voltage, the output current are given in Fig.5., Fig.6.,Fig.7,Fig.8,Fig.9respectively for duty 68 to 70%. The current through main switches is compared with switching pulse which shows Zero current switching is shown in Fig.10.Table1 gives the observation of the simulation parameters at full load.

Table 1. Simulation parameters for Case 1.

Simulation Parameters	Values
Duty ratio	0.68
Input Voltage	30
Output Current	1.38A
Output Voltage	724 V
Power Output	1000W
Load Resistance	520 ohms
Transformer turns ratio	1:3
Operating frequency	100 kHz

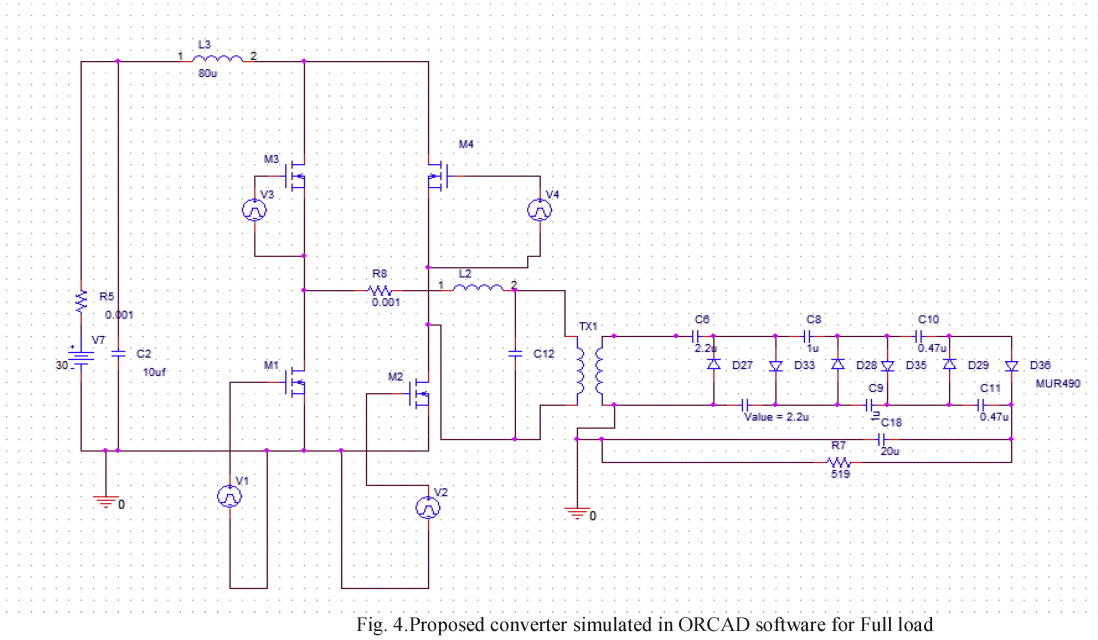

Fig. 4.Proposed converter simulated in ORCAD software for Full load

Fig.5 and Fig. 6 shows input voltage and switching pulses for S1 through S4 respectively. S1, S3 and S2, S4 switch pulses are identical. Fig.7 shows the transformer secondary voltage is three times higher than the primary. Fig.8 and Fig. 9 shows the output voltage and output current. For an input voltage of 30 V the output Voltage of 717 V with output voltage ripple of 0.7V and the output current of 1.382A are obtained.

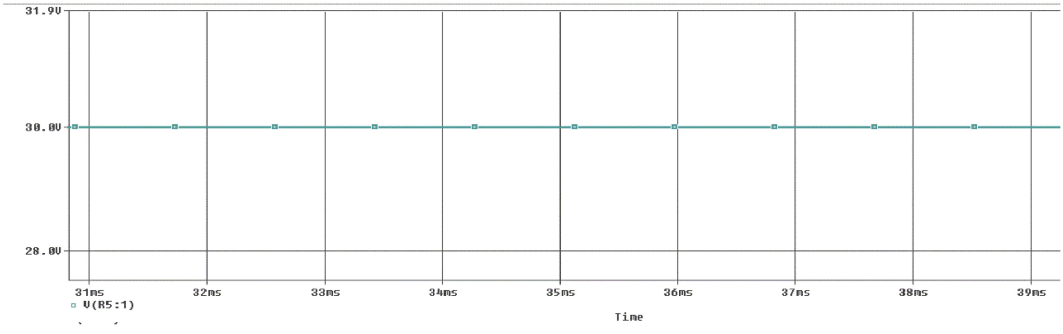

Fig.5. Input Voltage of the proposed converter for full load.

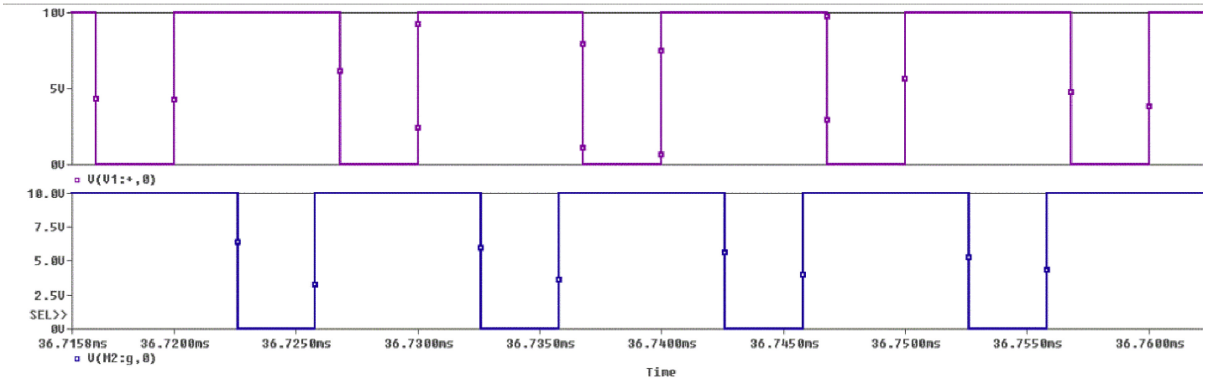

Fig. 6 Switching pulses at full load.

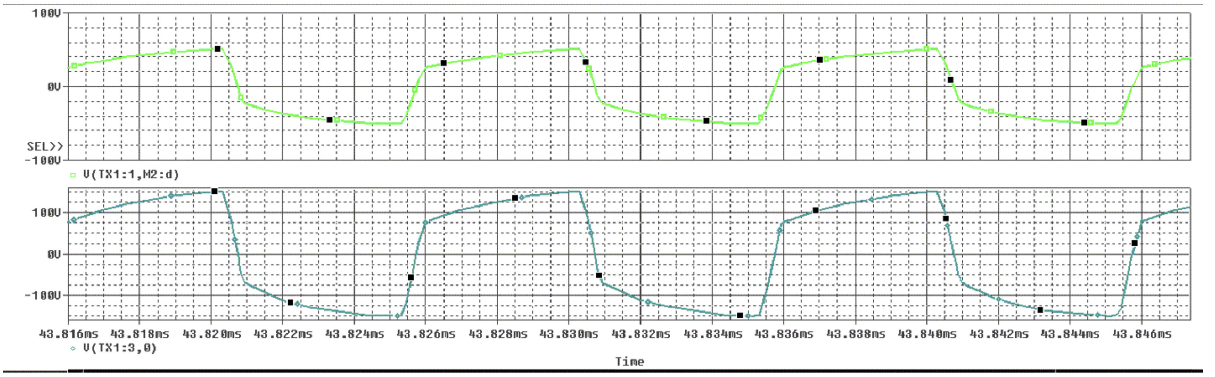

Fig.7. Transformer primary and secondary voltages.

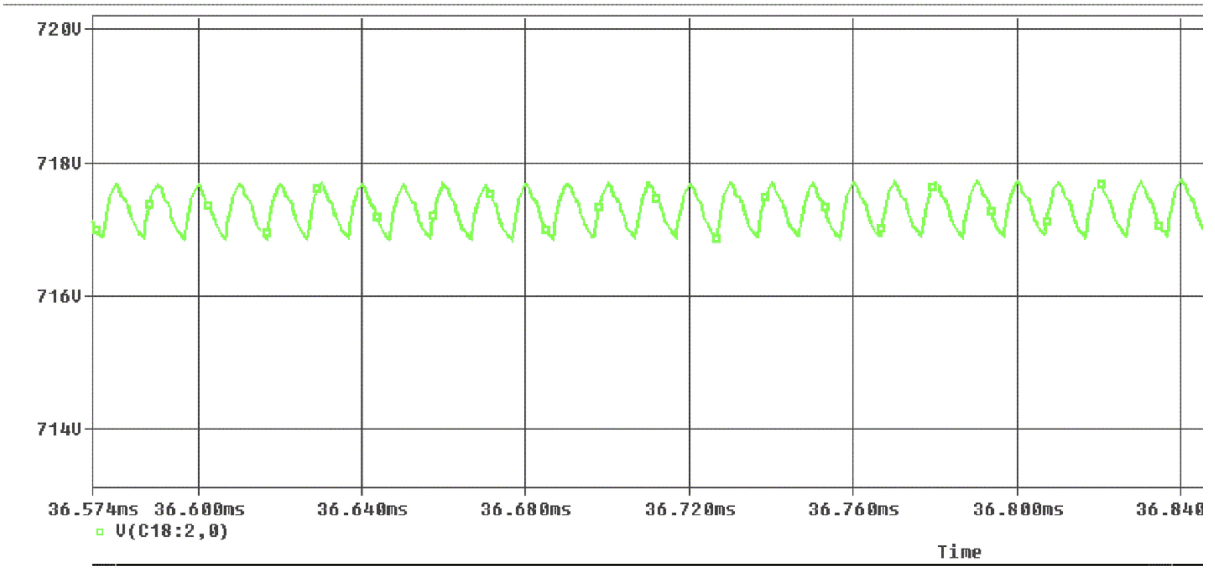

Fig. 8 Output Voltage.

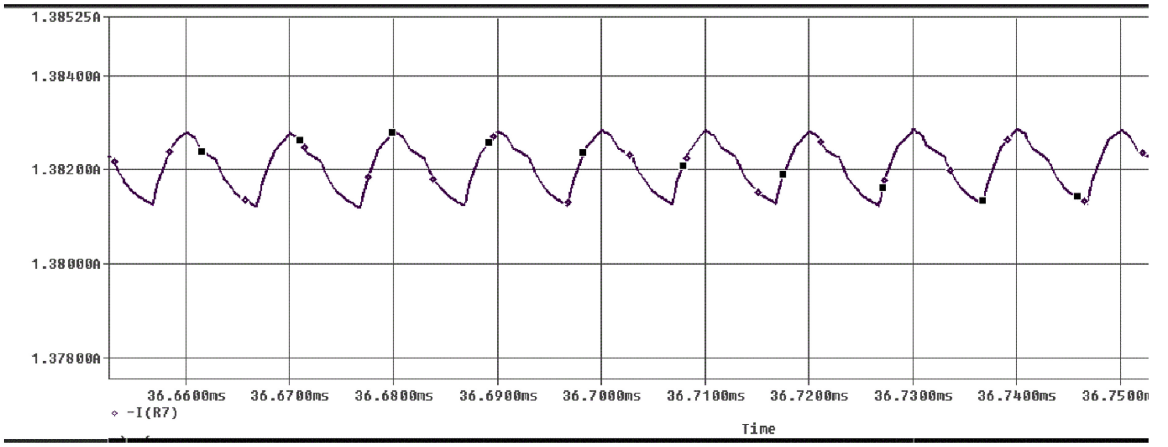

Fig. 9 Output current

Fig. 10.shows the switch pulse and drain current of main switch M1 and from figure it is clear that switch pulse is removed when switch current reaches to zero hence the main switch M1 is turned off by zero current switching (ZCS). The negative portion in switch current indicates body conduction of main switch M1.

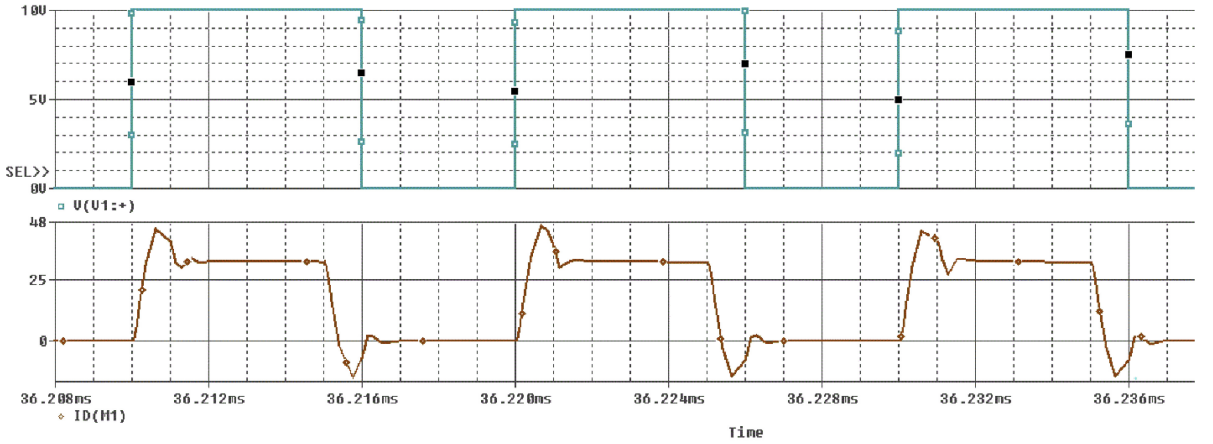

Fig. 10 Zero Current Switching of the proposed converter for full load.

CASE 2

This condition is observed for half load which is obtained at V_{in}= 34V for 500 watts. Fig.11. shows the proposed converter simulation using ORCAD Software for half Load. The input voltage, switch pulses, voltage across the primary and secondary of the transformer, and the output voltage, the output current are given in Fig.12, Fig.13.,Fig.14.,Fig.15.,Fig.16.respectively for duty 60 %. The current through main switches is compared with switching pulse which shows Zero current switching is shown in Fig.17.The Table.2 gives the observation of the simulation for case 2 at half load.

Fig.12 and Fig. 13 shows input voltage and switching pulses for S1 through S4 respectively. S1, S3 and S2, S4 switch pulses are identical. Fig.14 shows the transformer secondary voltage is three times higher than the primary. Fig.15 and Fig. 16 shows the output voltage and output current. For an input voltage of 34V the output Voltage of 730V with output voltage ripple of 0.3V and the output current of 704.56mA are obtained.

Table 2. Simulation parameters for Case 2.

Simulation Parameters	Values
Duty ratio	0.60
Input Voltage	34
Output Current	0.703
Output Voltage	730V
Power Output	500W
Load Resistance	1037 ohms
Transformer turns ratio	1:3
Operating frequency	100 kHz

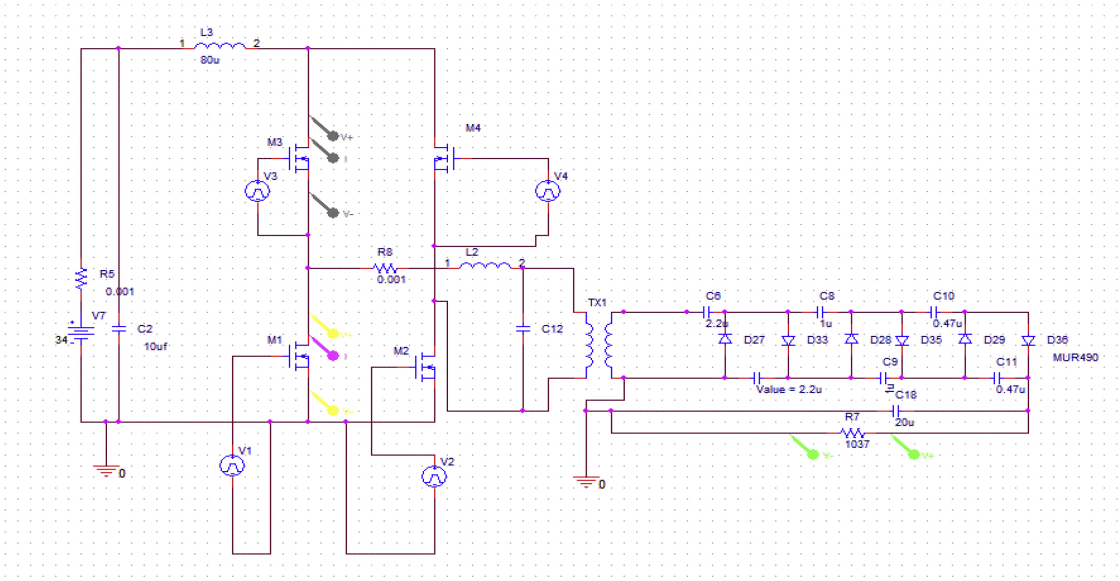

Fig.11. Proposed Converter simulated in ORCAD software for half Load

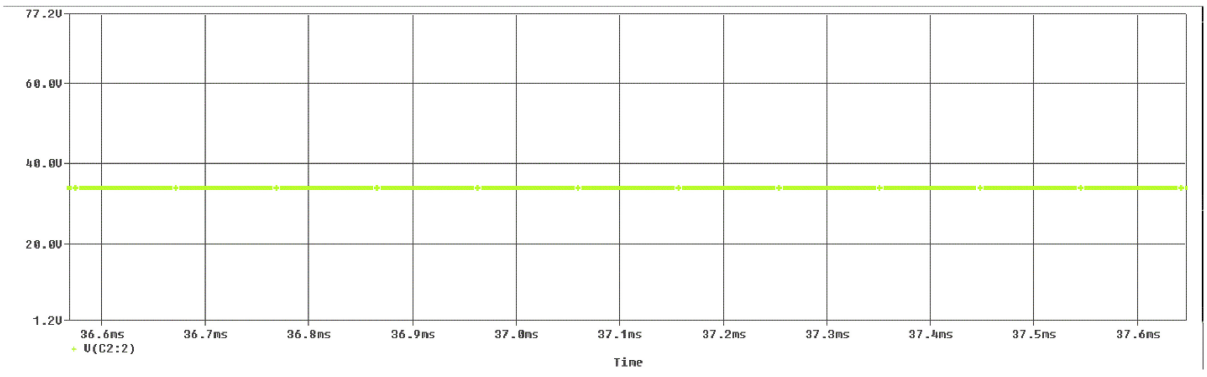

Fig.12. Input Voltage for half load.

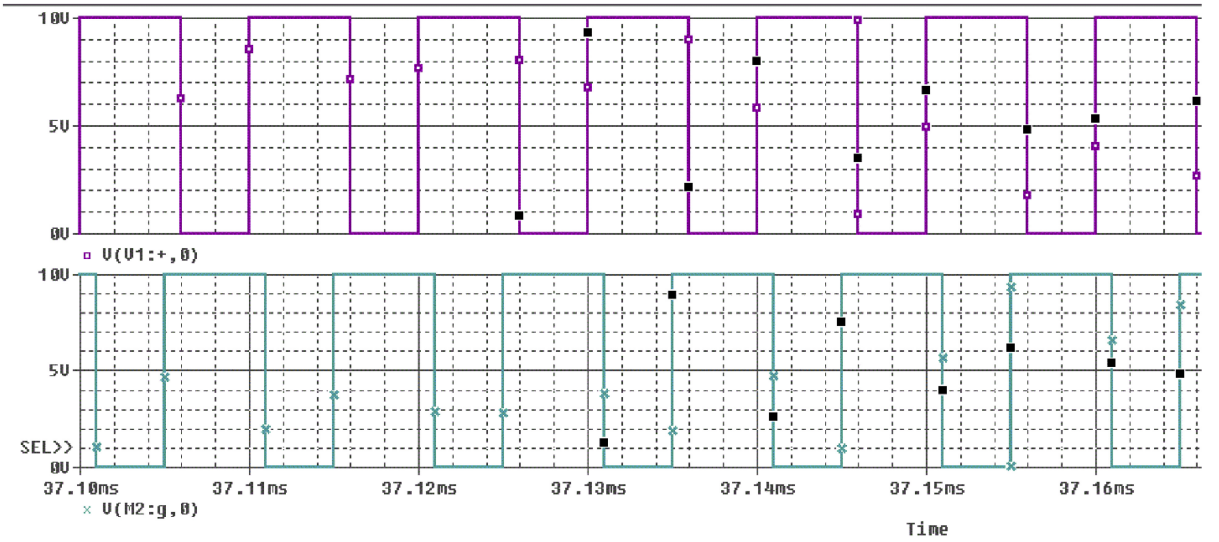

Fig.13. Switching pulses.

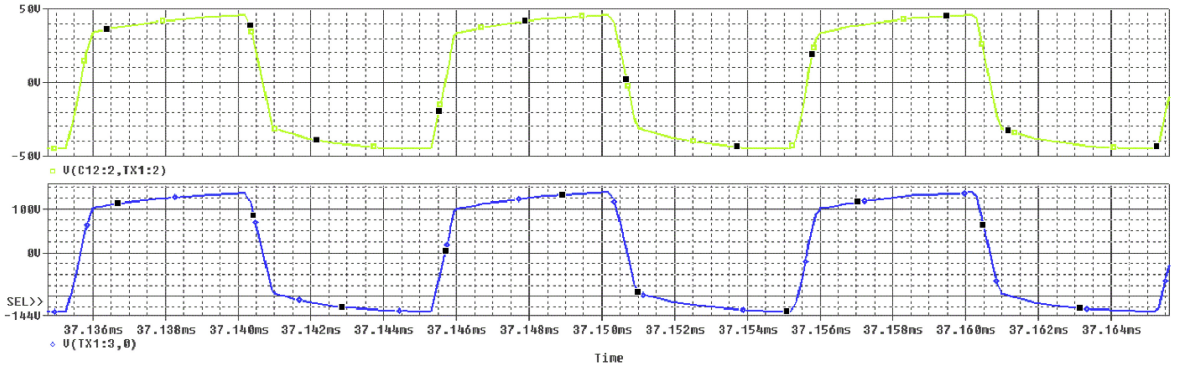

Fig. 14.Transformer primary and secondary voltage.

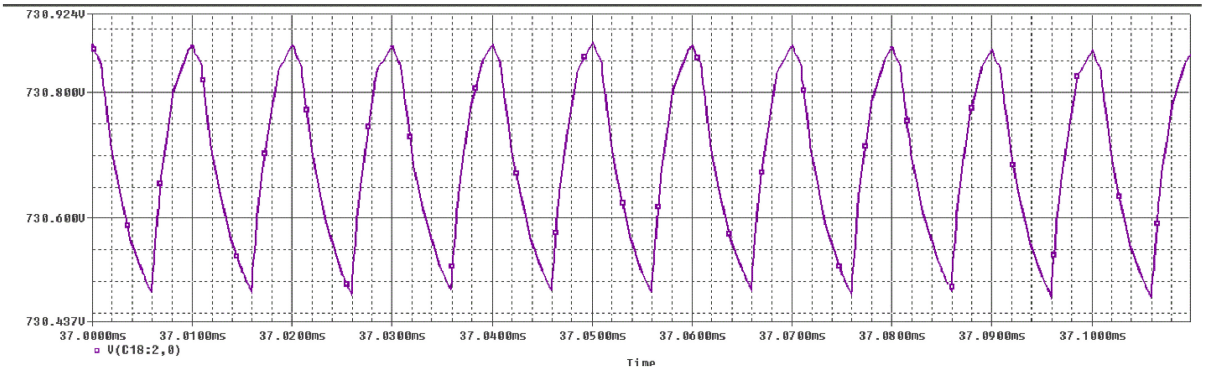

Fig. 15 Output Voltage.

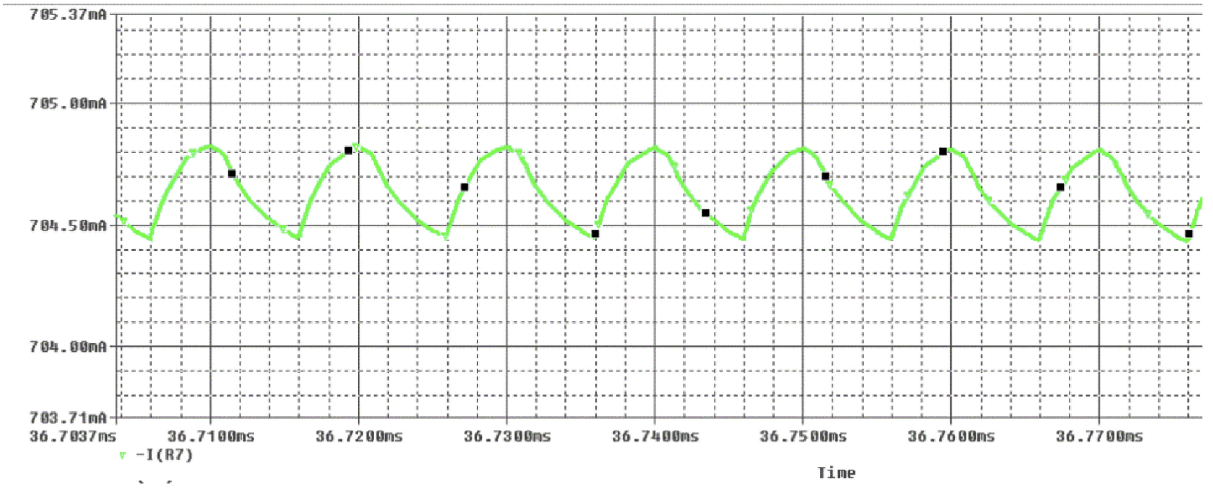

Fig. 16 Output current.

Fig.17. shows the switch pulse and drain current of main switch M1 and from figure it is clear that switch pulse is removed when switch current reaches to zero hence the main switch M1 is turned off by zero current switching (ZCS). The negative portion in switch current indicates body conduction of main switch M1.

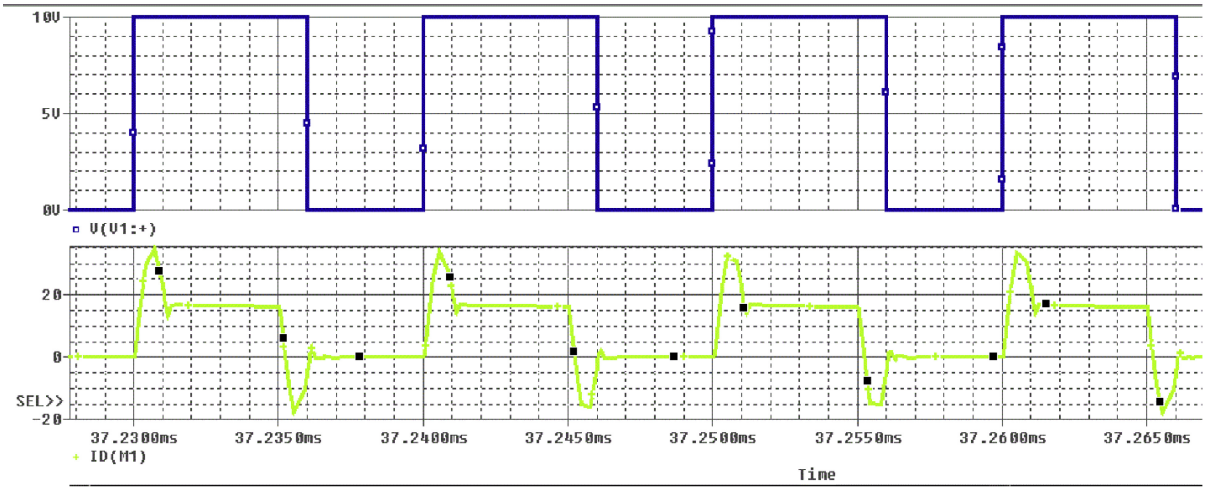

Fig.17. Zero Current Switching of the proposed converter for half load.

4. Hardwareimplementation

An experimental prototype for the proposed circuit with three stages of voltage multiplieras shown in Fig.18 was built for the reduced specifications as shown in the Table 3. The DSO output showing the input and output voltage and the microcontroller pulses are shown in Fig.19 (a)and Fig.19 (b).

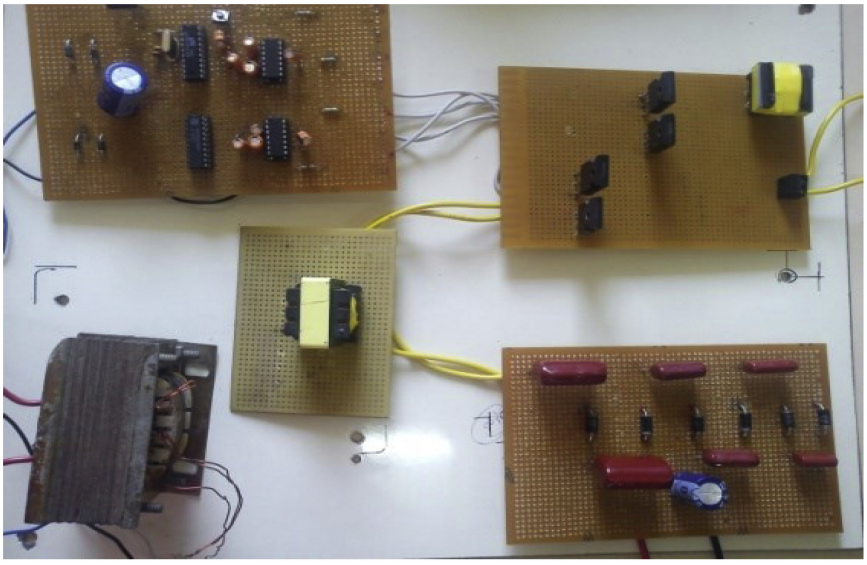

Fig.18. Experimental Prototype of the Proposed Converter for three stage Voltage Multiplier

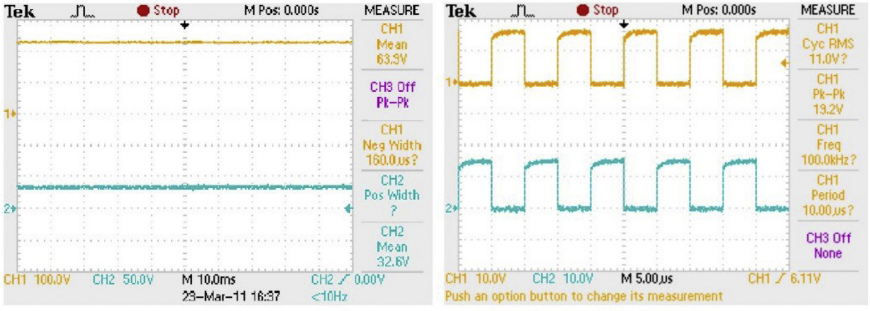

Fig. 19. DSO output and input voltage and Microcontroller pulses for the switches

Table 3. Hardware Specifications (for three stages)

Simulation Parameters	Values
Input Voltage	30V
Output Voltage	240V
Output Current	0.6A
Transformer turns ratio	1:1 (25turns)
Operating frequency	100 kHz

5. Conclusion

Summarizing the most important properties of the Current Source Inverter and Minimum Capacitance Voltage Multiplier as revealed by the circuit diagram, the description of operation and the different waveforms, the following conclusions can be drawn: The proposed converter analyses the converter operation with two cases and simulations were observed with variation in fuel cell stack voltage with Vin =30V (full load) and Vin=34V (half load). The dc link voltage of 720+/- 10% voltage is obtained as an output for three phase grid connected

applications. For both the cases Zero current switching was obtained. A reduced specification prototype was built. Transformer structure is simpler and less bulky. The number of turns on primary as well as secondary side is 25 turns and it can withstand current of 5 Amps. An output voltage of 240V is obtained from the voltage multiplier, for the same transformer size. The core losses are considerably reduced and the efficiency thus increases. On the other hand the advantages of minimum capacitance voltage multiplier are elimination of the need for implementing transformers with a large number of turns and reducing the cost of the multiplier circuit. This enhances the compactness of the circuit and improves the efficiency and performance considerably.

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