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DESIGN OF COMBINATIONAL LOGIC CIRCUIT PROBER

Mohanad ABDULHAMID
AL-Hikma University, Iraq
moh1hamid@yahoo.com

Okoth MASIMBA
University of Nairobi, Kenya
researcher12018@yahoo.com

ABSTRACT

The objective of this paper is to design and implement a logic circuit prober to display truth tables of a three input combinational logic circuit. The truth table is to be as "1" and "0" on an ordinary 60 MHz oscilloscope. This paper meets this objective by using Lissajous Patterns to plot a "0" or a "1" on the oscilloscope screen. To plot a "0" on the oscilloscope screen, two sinusoidal signals in quadrature are supplied to the two inputs of the oscilloscope with the scope set to X-Y mode. To plot a "1" on the oscilloscope, only the signal to the Y input is allowed to reach the oscilloscope screen. To display all the 32 patterns required to obtain a three input truth table, two staircase waveforms are employed. The staircase waveforms, one eight-step and the other four-step, are added to the two sinusoidal signals to shift the patterns along the X and Y directions to produce all the 32 patterns.

KEYWORDS: Logic circuit prober, truth table, Lissajous patterns

1. Introduction

The 21st century has been characterized by high speed data transmission. There has been an ever increasing need not only to transmit information at higher speeds but also to make the information more robust to noise while at the same time economically using the bandwidth. This need has been observed in the 3G and 4G revolution of the mobile industry as well as the introduction of high definition television (HDTV) in the broadcasting industry and the phasing out of analogue televisions in exchange for digital ones in the entertainment scene. To meet this need, digital signals and digital circuits to control the digital signals have been extensively employed. Digital signals and circuits have also been extensively used in the design of digital controllers in plants as well as in the design of logic for the control of more intelligent machines creating a digital revolution. With this digital revolution, there is need to be able to design the circuitry to support it (Mano & Celeti, 2006).

Various tools have been designed for application in the analysis and design of digital circuits. One of them is the logic analyzer. The logic analyzer is an electronic instrument that displays signals in a digital circuit that are too fast to be observed and presents it to a user in form of timing diagrams so that the user can more easily check the operation of the digital system with precision. They are typically used for capturing data in systems that have too many channels to be examined with an oscilloscope (Karambelkar & Shinde, 2012).

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Another tool that can be used in the design of logic circuits is the logic probe. It is a hand-held pen-like probe used for analyzing and troubleshooting the logical states of a digital circuit. The logic probe displays a different color for logic one and logic zero.

While the logic analyzer can be used in the design of a system with several inputs, it has the disadvantage in that the output is in the form of timing diagrams and thus assumes a prior knowledge of analysis of timing diagrams. The logic analyzer is also very expensive. The logic probe overcomes these shortcomings by being cheap and user friendly. It has the main disadvantage of being limited to only one input at a time and can therefore not be used in analyzing a digital circuit (Weiping & Huan, 2016). The combinational logic circuit prober overcomes the shortcomings of the logic analyzer and the logic probe. It displays its outputs in form of "0" and "1" on an oscilloscope screen therefore making it more user friendly in comparison to the logic analyzer. The combinational logic circuit prober can also display data from several channels making it useful in the analysis of digital circuits as compared to the logic probe (Bai & Chen, 2018).

2. Design Methodology

To meet the objective of the paper, the block diagram of Figure no. 1 is designed to be implemented. Each block in Figure no. 1 is explained in subsequent sections.

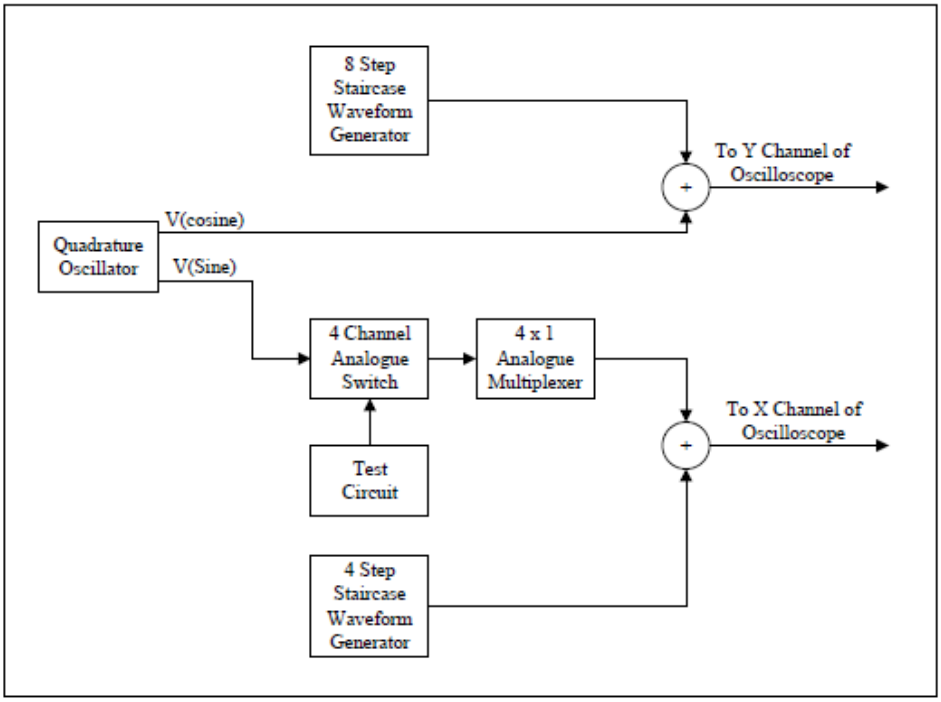

Figure no. 1: *Combinational logic circuit prober block diagram*

The block diagram design consists of the following modules:

a) Quadrature oscillator;
b) Timer circuits;
c) Staircase generator;
d) X-position controls;
e) Y-position controls;
f) Buffer.

2.1. Quadrature oscillator

The quadrature oscillator as shown in Figure no. 2 is a type of phase shift oscillator that provides both sine and cosine waveform outputs (the outputs are in quadrature). The two quadrature signals are required in plotting a zero on the oscilloscope. The quadrature oscillator, in

comparison to other Operational Amplifier (Op-Amp) oscillators, is the most suitable oscillator for the combinational logic circuit prober since it can economically produce two signals in quadrature.

The output of the quadrature oscillator increases in distortion as the frequency increases. At a frequency of 7 kHz, the designed quadrature oscillator could operate without significant distortion at the output. A frequency of 7 kHz is also enough to produce an adequate refresh rate on the oscilloscope screen. The quadrature oscillator is therefore set to operate at a frequency of 7 kHz.

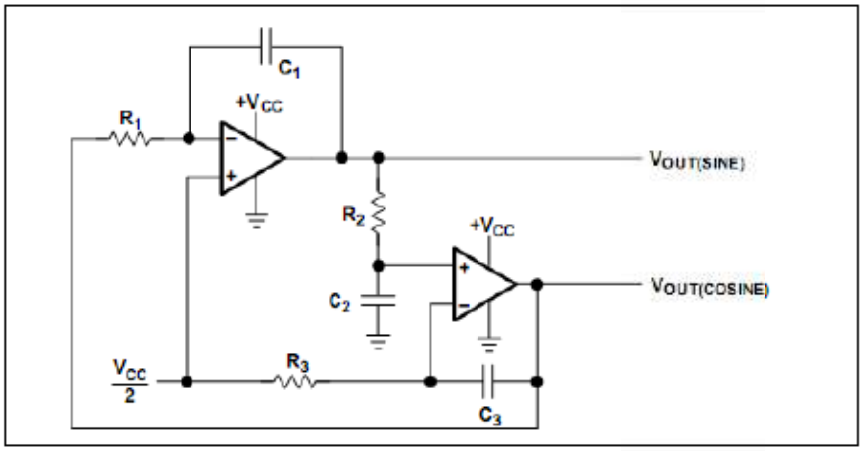

Figure no. 2: *Quadrature oscillator*

2.2. Timer circuits

Timer circuits are required to control the logic selection units (analogue switch and analogue multiplexer) as well as the staircase waveform generator. The timers are also needed to provide the required clock pulses to the counters that produce the logic levels used in the construction of the truth table. The 555 timer is used to achieve the required timings.

To give the sinusoidal signals ample time to draw a complete "0" or a complete "1" on the oscilloscope screen, the frequency of Timer 1 should be at least half that of the oscillator. The frequency of Timer 2 should allow all the first four patterns to be plotted on the scope before moving to the second level. Therefore, the frequency of Timer 1 should be four times that of Timer 2 at the very minimum. The timer circuit is shown in Figure no. 3. The timer circuit is included in the block of test circuit in Figure no. 1.

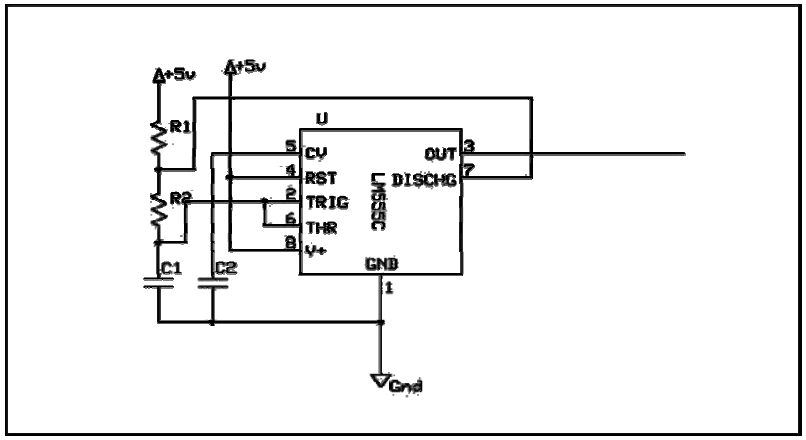

Figure no. 3: *Timer circuit implementation*

2.3. Staircase Waveform Generator

In order to display all the 32 patterns required for a three input combinational logic circuit, dc voltages of increasing amount are required to be added to the sinusoidal signals. A staircase waveform which appears as a set of discretely increasing dc values is used. The circuit used to generate the staircase waveforms is shown in Figure no. 4. This circuit is represented in Figure no. 1 by block of 8-step staircase waveform generator.

The eight-step staircase waveform generator is constructed using an 8x1 analogue multiplexer with the inputs being supplied by a potential divider circuit as shown in the Figure no. 4. The selection is implemented using the three Least Significant Bit (LSB) bits of a 4 bit counter.

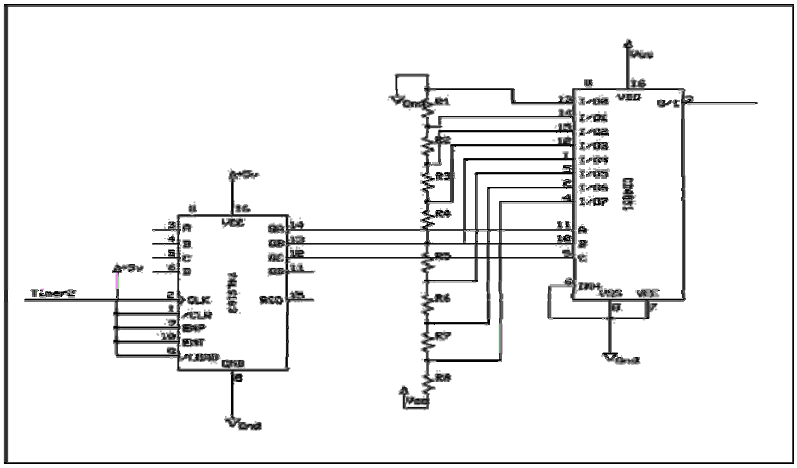

Figure no. 4: *Eight-step staircase waveform generator circuit*

The connection for the four-step staircase waveform generator is similar to that of the eight-step staircase waveform generator with the 8x1 analogue multiplexer being replaced with a 4x1 analogue multiplexer (CD4052). Only the four lower levels of the potential divider connection are used as the inputs to the multiplexer. The two LSBs of a second counter are used for the multiplexer switch selection. The two staircase waveform generator circuits are simulated in Proteus and also implemented in the laboratory and give the laboratory results shown in the Photographs in Figure no. 5 and Figure no. 6.

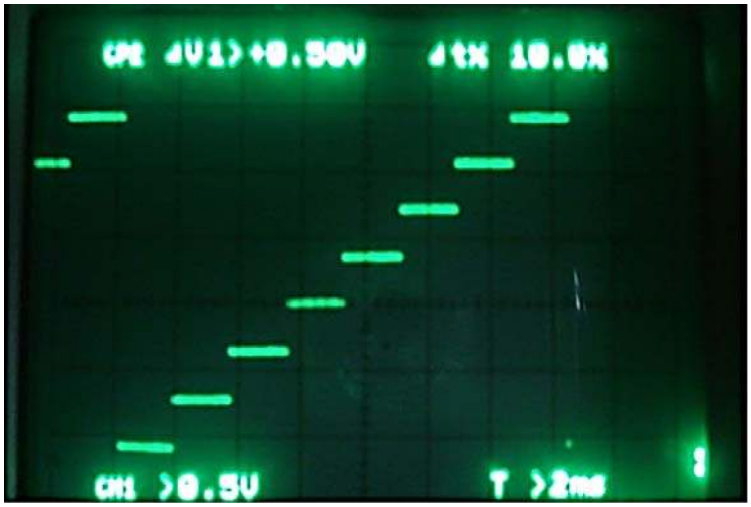

Figure no. 5: *Eight-step staircase waveform*

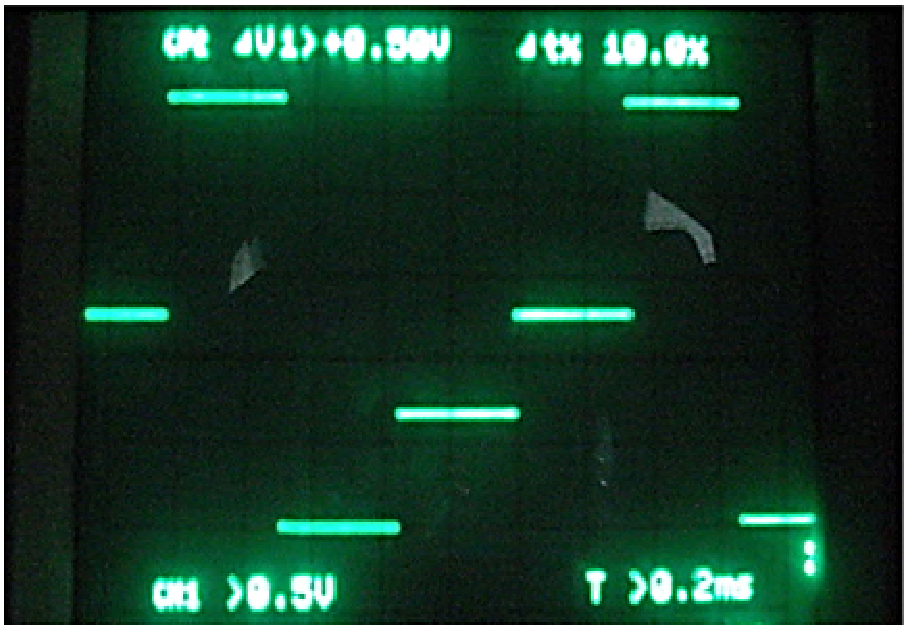

Figure no. 6: *Four-step staircase waveform*

2.4. X-Position controls

The X-Position control is to determine the logic levels to be displayed on the oscilloscope screen i.e. whether a "1" or a "0". It displays the inputs to the combinational logic circuit and the output on the scope. In addition to displaying the inputs and the output of the combinational logic circuit, the X-Position control is also employed to shift the patterns four steps along the X direction at Timer 1 frequency therefore displaying four patterns on the scope screen.

2.4.1. Selection of logic levels

To select the required logic levels to display on the scope, a combination of a four bit counter run by Timer 2 (Counter 2), a 4-channel analogue switch, a 4x1 analogue multiplexer, a four-bit counter run by Timer 1 (Counter 1) and four inverter gates are used.

Three of the LSB outputs of Counter 2 are used as the control bits of the analogue switch having been inverted as shown in Figure no. 7. The fourth analogue switch control bit is obtained from the inverted output of the combinational logic circuitry. The channel input to the analogue switch is one of the signals from the quadrature oscillator. This section of the X-Position controls simply provides a complete channel to the output if the counter bit or the combinational logic circuit output is a one, otherwise it blocked the channel. The next section of the X-Position controls used in the selection process involves a 4x1 analogue multiplexer with the selection switches being controlled by the two LSBs of Counter 1. The four channel outputs of the analogue switch provide the inputs to the multiplexer channel. At a speed four times that of Counter 1, the multiplexer moves through the four channels selecting and presenting the output of the signals at the channels.

2.4.2. Shifting of the logic levels

To display the four logic levels on one line, the output of the X-position controls is combined with the four-step staircase waveform. The circuit of the X-position controls is given in Figure no. 7. This circuit is connected to X channel of oscilloscope in Figure no. 1.

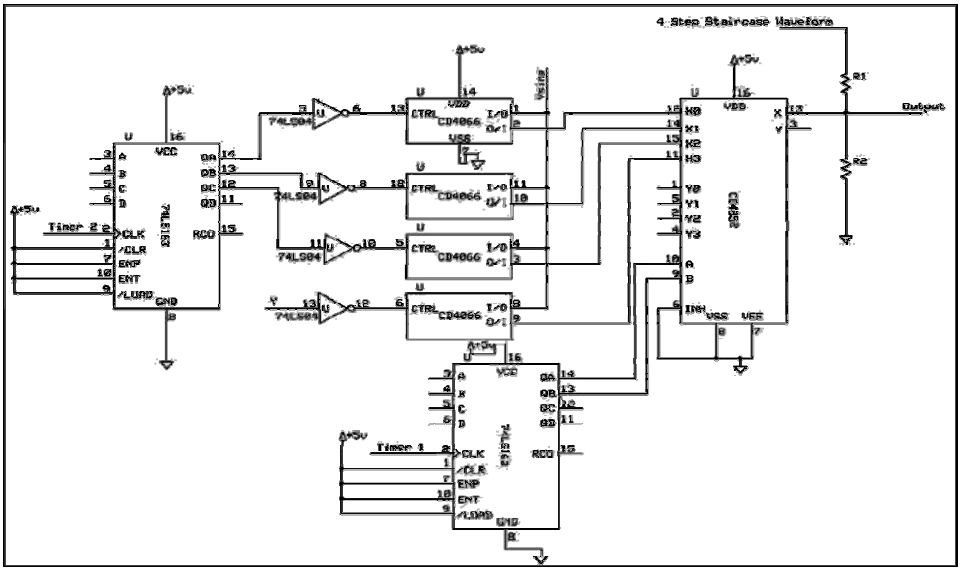

Figure no. 7: *X-Position controls circuit*

2.5. Y-Position Controls

The purpose of the Y-Position controls is to shift the already formed four patterns on the X-axis along the Y-axis thereby producing eight levels and hence 32 patterns on the oscilloscope screen. The function of the Y-Position controls is achieved by combining the eight-step staircase waveform with V_{cosine} signal from the quadrature oscillator.

2.6. Buffer Circuit

During the implementation of the staircase waveform generator circuit and the oscillator circuit, it is observed that when these circuits are connected to the rest of the circuitry, their outputs are loaded. This loading results in the distortion of both the staircase waveform and sinusoidal signals. To counter this effect, a circuit with a very high input impedance and very low output impedance is required and this requirement is met by the implementation of an Op Amp buffer circuit as shown in Figure no. 8. The buffer circuit is embedded in block of oscillator and block of staircase waveform generator in Figure no. 1.

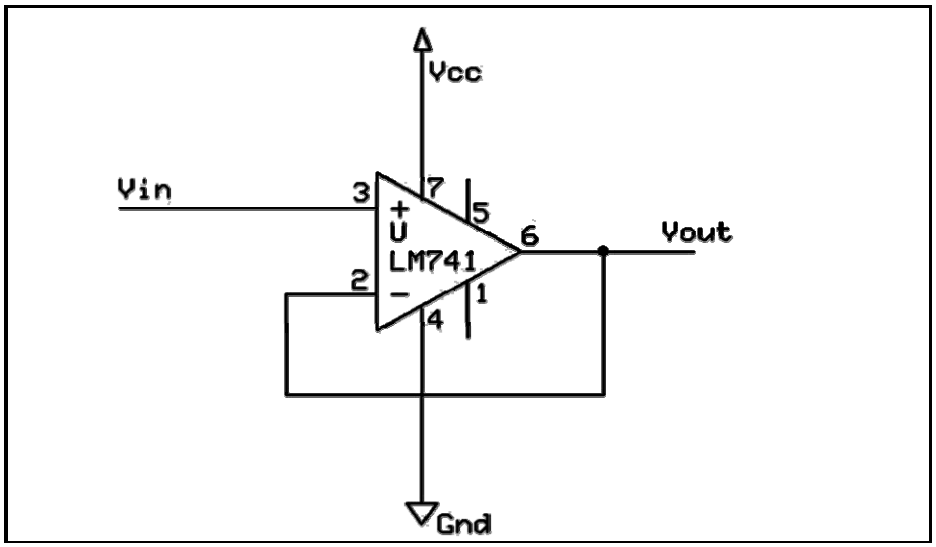

Figure no. 8: *Op-Amp buffer circuit*

3. Results

A simple three input AND gate, a simple even bit parity generator and a simple majority logic circuit are implemented as shown in Figure no. 9, Figure no. 10, and Figure no. 11 respectively. The truth tables for these combinational logic circuits as obtained by the combinational logic circuit prober are shown in Figure no. 12, Figure no. 13, and Figure no. 14 respectively.

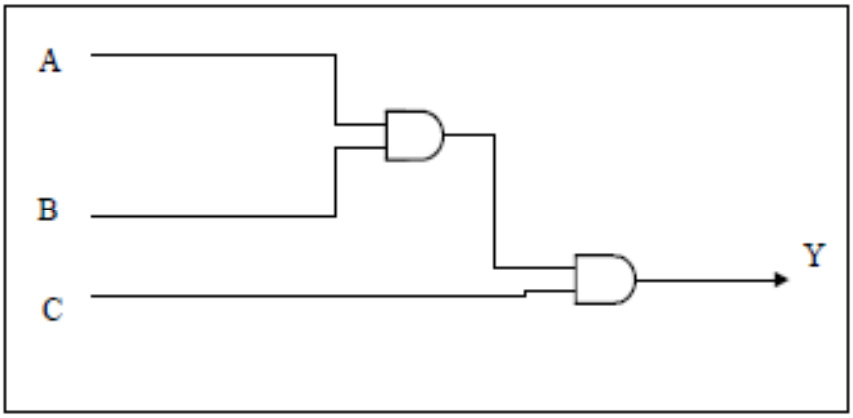

Figure no. 9: *A simple three input AND gate*

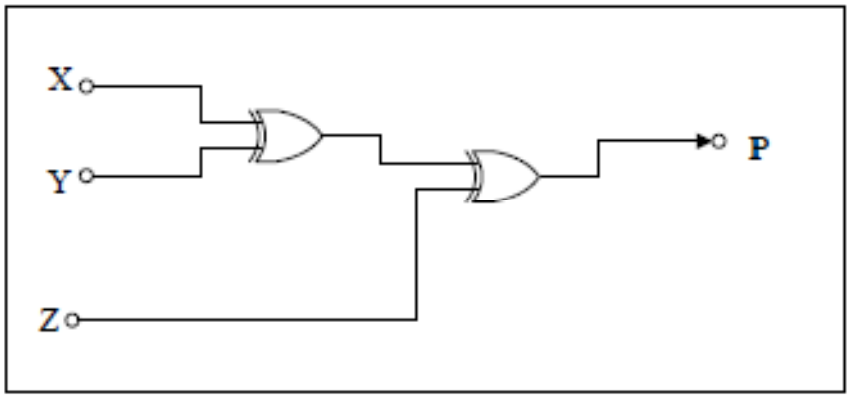

Figure no. 10: *A simple even bit parity generator circuit*

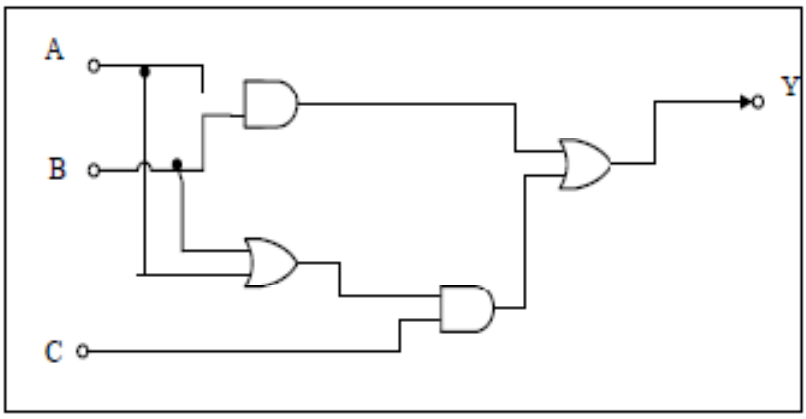

Figure no. 11: *A simple majority logic circuit*

Figure no. 12: *A three input AND gate truth table*

Figure no. 13: *A simple even bit parity generator truth table*

Figure no. 14: *A simple majority logic circuit truth table*

4. Conclusions

It was shown in this paper that a truth table for a combinational logic circuit can be displayed on an ordinary 60 MHz oscilloscope in form of "1"s and "0"s. Despite the few setbacks, the "0"s and "1"s obtained by the combinational logic circuit prober were clearly distinguishable. The combinational logic circuit prober was used to obtain the truth tables of a simple even bit parity generator circuit, a majority logic circuit and a three-input AND gate and the results verified to be accurate by comparison with the theory.

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