ISSN (Print) : 0974-6846
Indian Journal of Science and Technology, *Vol 8(32), DOI: 10.17485/ijst/2015/v8i32/87600, November 2015* ISSN (Online) : 0974-5645

Design of NIOS II Soft-Core based Partial Reconfiguration Controller in FPGA for MPSoC Design

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Abstract

Recent advancement and research in FPGA has led to the development of energy optimization techniques and runtime partial reconfiguration in FPGA. This work describes an effective approach for power reduction techniques in FPGA based Multiprocessor system-on-Chip (MPSoC) platform and it works on partial reconfiguration technique during runtime. Partial reconfiguration is implemented to reconfigure only a part of FPGA dynamically and other parts of the device continues there operation undisturbed. NIOS II soft-core processor is programmed as control processor to perform reconfiguration partially and also it manages the dynamic power optimization process. This control process is further configured for clock-gating which works on a FPGA logic element and cut down a substantial part of dynamic power dissolution in FPGA. Proposed power optimized low power MPSoC is implemented using ALTERA cyclone III FPGA and its power analysis is performed and summarized.

Keywords: Dynamic Power Optimization, Multiprocessor System-On-Chip, Partial Reconfiguration

1. Introduction

Partial reconfiguration during runtime is the capability to modify the designed hardware to perform certain function. This technology is named as partial reconfiguration dynamically, which is completely operational and now a day's provided by major FPGA manufacturers Altera and Xilinx. Reconfiguration during run time will reduce the use of area on silicon chip by sharing available space for multiple operations executed parallel. This will greatly reduce the FPGA usage by reconfiguration. To meet the increasing requirement for computing with less power and chip area has led to the Multiprocessor System on Chip (MPSoC). More functionality is accumulated in these systems and hence they require less power consumption for long battery life. In case of any application which utilizes many tasks with same hardware will require partial reconfiguration during runtime. There will be tradeoff between area utilized, power consumed and actual energy requirement. This dynamic reconfiguration is utilized in certain cases such as 1. Many software task for same hardware, 2. In case of mix in both hardware and software, 3. Dynamical hardware task.

MPSoC is an emergent area in embedded systems which is an on chip architecture formed by complex components integrated to communicate at high speed with each other. This single chip architecture is used in dedicated application system design with complex and parallel processing n capability[1]. MPSoC architecture comprise of many heterogeneous components like elements for processing, storage device and interfaces for communication. Selection of appropriate processing unit, power optimization for on chip, communicating via processor is challenging and considered as bottleneck in MPSoC based embedded system design[1,2]. Reconfiguration using FPGA is an important factor to design low power MPSoC platform dependent embedded applications. Due to the high performance per watt of

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reconfigurable logics they offer on–chip reconfigurable memory blocks[3,4]. Reconfigurable hardware support is provided by all leading soft core processors such as NIOS II, Pico Blaze, MicroBlaze, Xtensa LEON, etc.[5]. Run time partial reconfiguration reduces power consumption and chip-area gradually[6–10].

This work elaborates the partial reconfiguration implementation using NIOS II soft core processor with FPGA. Here FPGA is used for dynamically setting the embedded memory provided in on-chip and also for allocating PLL bandwidth for low power applications. The rest of the paper is organized as Section 2 discusses about the partial reconfiguration, Dynamic Frequency Scaling (DVFS), clock gating. Section 3 describes the integration of power minimization technique in NIOS II based MPSoC design. Experiment setup and data analysis is presented in section 4. Section 5 summarizes the paper.

2. Preliminary

2.1 Partial Reconfiguration

Partial Reconfiguration during runtime (PR) is a peculiar attribute given by FPGAs, which willprovide the user facilities to reconfigure only certain existing application while other process are running in the design. The above attribute makes the hardware to be adaptable for dynamic environment. Power optimization is performed by reducing the hardware implementation for computing and with proper utilization of chip area of different hardware blocks can be configured at runtime. Finally, leakage and clock dispersion power saving is obtained by load balancing the hardware which not active or utilized at that time. One of the crucial issues in partial reconfiguration is speed of reconfiguration between two reconfiguration processes, which in turns reduces the performance and increase power overhead. If the speed of configuration increases then overhead is minimized[12].

2.2 Clock Scaling

Clock scaling is one of the common approaches in ASIC based design or in case of microcontroller based system design. Clock scaling is required to adjust the varying power consumption dynamically. One of the important approaches is reconfiguration of Phase-Locked Loop (PLL) in real time scenario to realize the clock scaling in FPGA. This will allow sweeping frequencies from PLL output and adjusting clock phase for output dynamically. Some of the components in clock scaling are reconfigurable they are pre-scale counter, post-scale counter, feedback counter, Voltage-controlled oscillator and some of the other parameters can be changed. Frequency and phase of the cyclone III FPGA can be changed according to reconfiguration[13].

2.3 Clock Gating

Power consumption due to clock occupies an important portion in FPGA based design. Clock gating is a power optimization technique which will selectively utilize the clocking modules. Clocking modules are used when required by the active modules and making the remaining modules inactive. Power dissipation will be reduced greatly because of avoiding charging and discharging of the unused gates in the clocking circuit. Clock gating is performed by ANDing signal from clock with the control signal to constitute a gated clock. This is then given to the other components in the circuit. Control signal decides that upon which module this gated clock should be applied[11].

2.4 NIOS II based MPSoC Design

NIOS II is a soft core processor which is 32 bit works on RISC architecture. It is an embedded processor with pipelining stage of 5- pipelines with execution of 1 instruction per cycle. It consist of instruction cache memory, shifting operations for adding, multiply, dividing operations and to provide flexibility through reconfigurable architecture. The proposed MPSoC consist of three NIOS II processor, two soft core processors are executed for user application and one is used to control processor. Control processor is used in debugging and memory management. Every processor consists of a heterogeneous hardware block to connect other processors on the chip for communication.

Functional block diagram of proposed FPGA based low power MPSoC design shown in Figure 1 which is divided into static region and dynamic region[14].

FPGA consists of static region and dynamic region. Static part is a region in which the design made for input will be active for entire process. The static region is always kept active for whole time. NIOS II processors is used here as configuration controller, logic element for data interface and managing all the input/output interfaces according to application requirement. This region is provided additionally with architecture to load balancing at various parts of the design such as system scheduling, managing the data and interfacing attributes. Another part is dynamic region which is not dependent on any

input design and it will not be active for entire application. This part can be loaded or unloaded to a target device as per the system requirement. Scheduler will decide the request time and location allocation. These regions will be resided as steam of bits in the outside memory of FPGA. Dynamic region consist of clock manager, application based hardware design and M4K memory are configured.

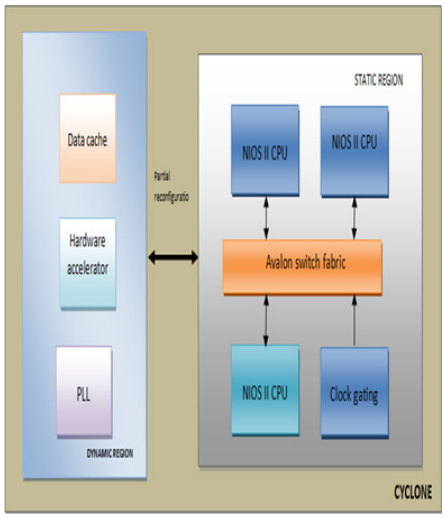

Figure 1. Functional block diagram.

3. Dynamic Power Manager

In this work NIOSII control processor is assigned for dynamic power manager.It consists of four jussive functions in order to optimize the power consumption due to dynamic and static regions. These four functions are partial reconfiguration, process remapped, clock manager and utilization observer. All the above functions are implemented to execute the control processor as software. Partial reconfiguration is used to control the modular devices such as PLL, embedded memory which is provided on chip. Dedicated hardware for dynamically varying regions is provided. Internal logics are used for processing and the reconfigurable bits are stored as bit stream in a 16 bit on chip memory such as MLABs or M20K blocks. The user should decide the number of applications to be active for the current operational state according to the amount of utilization of the active processor decision is made. Remapping algorithm is used for balancing the usage of each active region. Uncertainty in remapping decision is made because of this algorithm assumes that all process have equal workload and requires simple implementation. Here clock gating is managed and performed by the clock manager functionality which has a dedicated clock gate for every processor.RTL view of the circuit used in clock gating is shown in Figure 2. Clock gating circuit consists of LPM latch and LPM AND gate. Combination circuits consist of LPM latch and gate. They produce the glitches due to OR and AND base clock circuitry. Processor modules such as processing core, memories and caches are acquired by clock gate. After getting a clock all the components will start their preserved work and perform the operation assigned to them. The circuit size is very small, only 54 logic cells on FPGA[15].

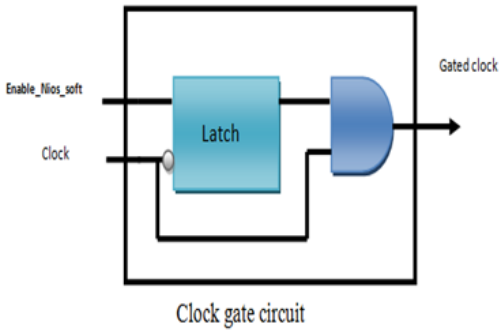

Figure 2. Clock gate circuit.

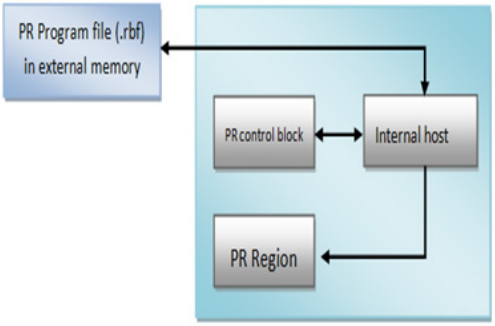

Figure 3. Partial reconfiguration with an internal H=host.

4. Result and Discussion

The proposed system is implemented using ALTERA QSYS and NIOS II IDE. Figure 4 shows the RTL view of MPSoC and the RTL view of PLL reconfiguration module is shown in Figure 5. The timing diagram in Figure 6 shows the timing analysis partial reconfiguration using NIOS II soft core processor.

Chip planner view of the proposed system in shown in Figure 7. Chip planner view displays the logic blocks and there placement, logic resources, route planning, clock region. Partial reconfiguration during runtime and area occupied by various components can be viewed from chip planner. The chip planner gives connection of recourses with other components such a logic cells, I/O elements, PLLs, etc. Figure 8 gives the partial reconfiguration of PLL.

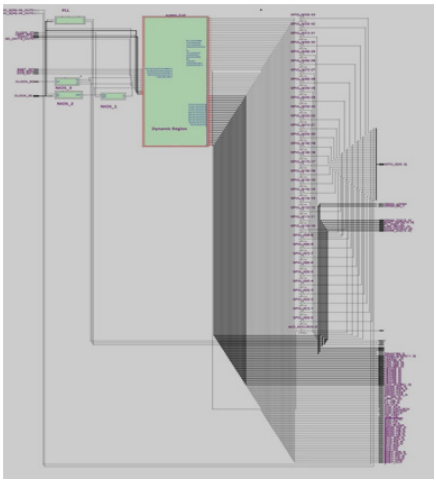

Figure 4. RTL view of NIOS II based MPSoC system.

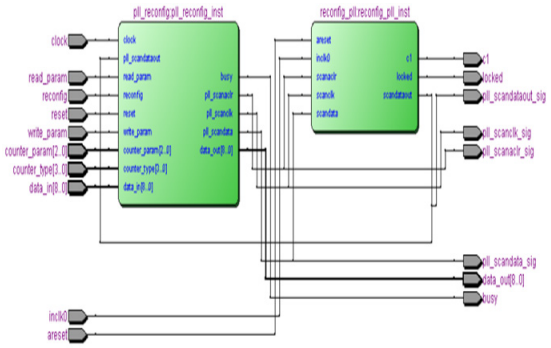

Figure 5. RRTL view of reconfigurable PLL model.

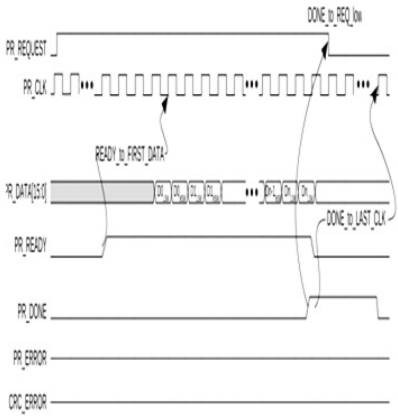

Figure 6. Partial reconfiguration timing diagram.

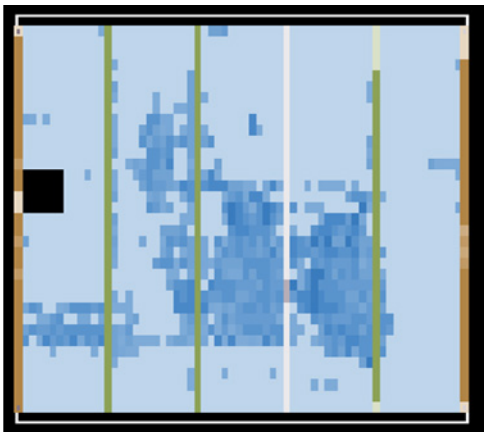

Figure 7. Chip planner view.

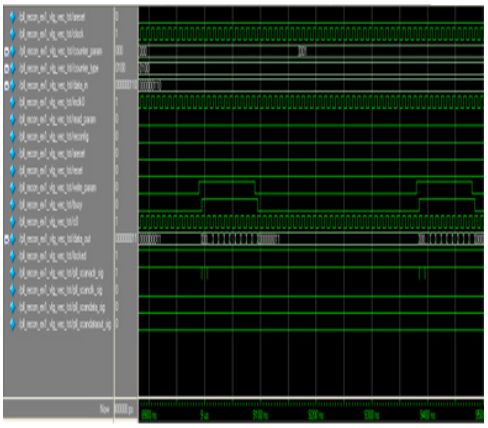

Figure 8. Partial reconfigurable PLL output.

Table 1 gives report on power dissipation and logic utilization based on different parameters such as partial reconfiguration with user logic and NIOS II. External host is also compared for power and utilization. Table 2 summaries the power dissipated depending upon varying clock frequencies at runtime.

Table 1.

Parameter	Total power dissipation in MW	Total logic utilization
Partial Reconfiguration with an Internal (user logic)	490.55	18611
Partial Reconfiguration with an Internal (NIOSS II)	356.23	16544
External Host	301.23	15700

Table 2.

Clock frequency	Total power dissipation in MW
50MHZ	490.55
100MHZ	598.00
200 MHZ	714.05

5. Conclusion

Partial reconfiguration controller is implemented in this paper using ALTERA cyclone III FPGA hardware and control processor is implemented by NIOS II soft-core processor. Here NIOS II processor is utilized for power management, logic utilization and analyzed using QUATRUS II IDE. The results are tabulated and reported. NIOS II processor has successfully performed the runtime partial reconfiguration and remapping using clock- gating. Power analyses is performed and proved that remapping the process and clock gating has optimized power greatly in FPGA.

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