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Effect of Underlap and Its Soft Error Performance in 30 nm Junctionless Based 6T- SRAM Cell

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Abstract

As CMOS device is scaling down significantly, the sensitivity of Integrated Circuits (ICs) to Single Event Upset (SEU) radiation increases. The Sensitivity of ICs to soft errors emerge as reliability threat which motivates significant interest in the development of various techniques both at the device and circuit level for SEU hardness in SRAM memories. To facilitate the scaling the concept of underlap Gate-Source/Drain (G-S/D) was suggested in the literature. L_{un} is one of the sensitive geometrical parameter considered to differ from 1 nm to 5 nm in a SEU radiating environment. The effect of Gate-Source/Drain underlap (L_{un}) on soft error performance in 30 nm Junctionless Transistor (JLT) based on 6T-SRAM cell has been examined through extensive mixed mode-device and circuit simulations using TCAD. The critical dose observed in JLT based 6T-SRAM with L_{un} ranging from 1 nm to 5 nm to flip the cell is given by Linear Energy Transfer (LET) between 0.05 to 0.06 pC/µm. The simulation result analyzes electrical and SEU radiation parameters to study its impact on JLT based 6T-SRAM cell.

Keywords*: Junctionless 6T-SRAM, Underlap, SEU Radiation, LET, HeavyIon, TCAD Simulation*

1. Introduction

Scaling of CMOS devices are mainly suffering from Short Channel Effect (SCEs) and Drain Induced Barrier Lowering (DIBL). The sensitivity of ICs to SEU radiation, coming from the natural space or present in the terrestrial environment is going up [1] i.e. the amount of minimum charge (known as critical charge) required to flip the memory cell (SRAM) decreases with scaling [2]. This event is known as soft error. Increasing design and fabrication complexities, smaller feature sizes, lower voltage and higher current levels, intrinsic parameter fluctuations, higher operating frequencies are also projected to cause an increase in the soft error failure rate in sub-90 nm ICs [3]. Soft error studies of deep sub-micron MOSFET-based 6T-SRAMs are dealt in detail [4],[5]. ITRS roadmap indicates that semiconductor memories will occupy major portion of chip area in the near future technologies [6]. SEUs have also been analyzed as an important reliability factor in the development of semiconductor memories [7]. Semiconductor memories such as SRAM is by far the dominant form of embedded memory found in today's ICs occupying as much as 60-70% of the total chip area and about 75%-85% of the transistor count in some IC products [8]. The most commonly used 6T-SRAM memory cell design uses six transistors to store a bit. The method to produce low power 6T-SRAM design was discussed in [9].

Device level characteristics of Double Gate Vertical (DGV) MOSFET with and without SOI structures are examined [10]. Since, the CMOS scaling technology brings in many unconventional devices especially FinFET, it is necessary to study the radiation effect on these devices and circuits. The transient response of planar Double-Gate and FinFET to heavy ion irradiation has been studied by 3-D numerical simulation in [11]. FinFET-based 6T-SRAM circuits are studied using TCAD simulations in [12],[13]. When these devices are scaled down to extreme dimensions, the formation of ultra-sharp junctions between source/drain and channel becomes complex since the doping concentration has to vary by several orders of magnitudes over a distance of a few nanometers. Therefore, highly accurate doping techniques and ultrafast dopant activation processes are required to avoid the lateral diffusion of source and drain impurities into the channel region.

Based on Lilienfeld's first transistor architecture a solution to this problem (Lilienfeld 1930) very recently, a Junctionless FinFET introduced by Colinge et. al. [14] has attracted device community. The SEU radiation analysis of a junctionless device is studied by Munteanu et. al [15]. Soft error study of Junctionless FinFET based SRAM is studied in [16]. To facilitate

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the scaling phenomena the concept of Gate-Source/Drain underlap (L_{un}) with low-doped channel was suggested [17]. L_{un} is one of the sensitive geometrical parameter considered to differ from 1 nm to 5 nm in a SEU radiating environment. In this paper, we have studied the Effect of L_{un} on SEU/soft error performance of tri-gate Jnless 6T-SRAM cell. L_{un} has been taken as a parameter under our control. Minimum radiation dose required to flip the cell is found out by doing the transient simulations using TCAD device simulator.

This paper is organized as follows: Section II discusses about Junctionless device construction and calibration. Section III talks about Junctionless 6T-SRAM structure simulation and SRAM operation. Section IV explains SEU radiation phenomena on Junctionless 6T-SRAM and provides the simulation results and discussions. Section V provides the conclusion.

2. Device Construction and Calibration

The various device parameters are shown in the schematic diagram of Figure 1. Sentaurus TCAD simulator from Synopsys is used in this work. The simulator has many features and modules used in our simulation are: Sentaurus Structure Editor (SDE) is used to create individual device structure. Common Triple-Gate-NMOS and PMOS JLT is created as shown in Figure 2 and Figure 3 prior to SRAM simulation. During device simulation, the mobility model includes doping dependency, high-field saturation and transverse field (i.e. gate field) dependency etc.

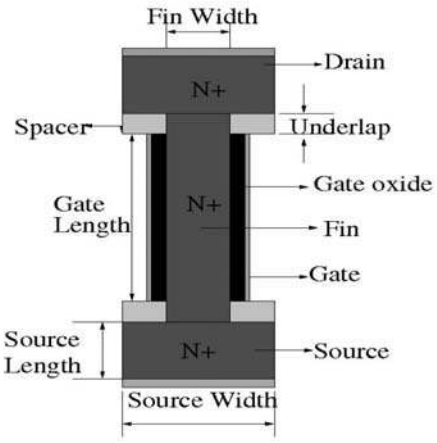

Figure 1. Schematic view of 2-D Junctionless FET

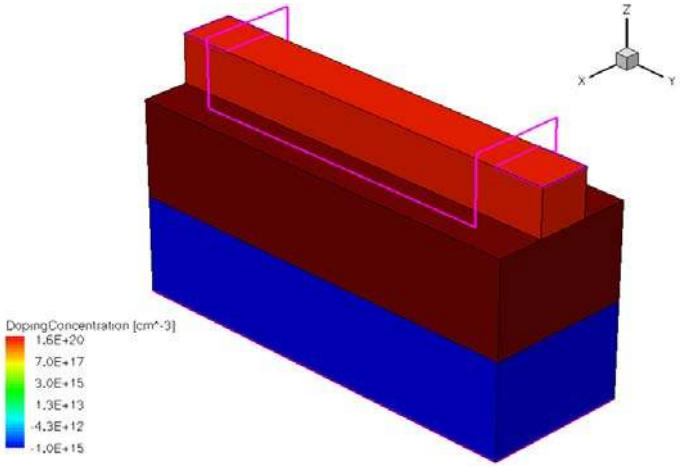

Figure 2. Common Tri-gate JLT NMOS Device Structure (Gate Oxide is removed)

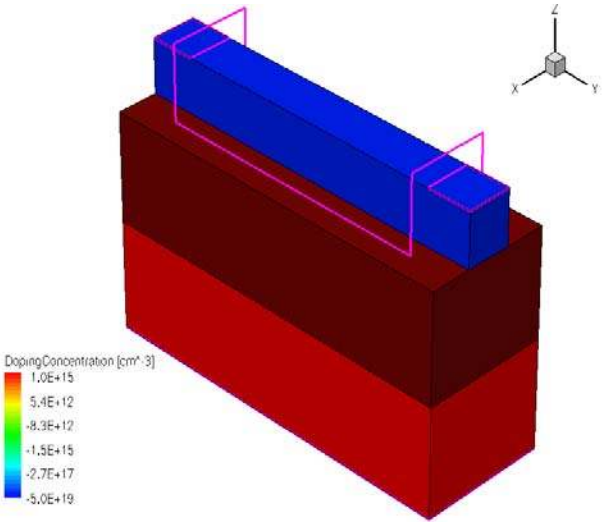

Figure 3. Common Tri-gate JLT PMOS Device Structure (Gate Oxide is removed)

Sentaurus Device (SDEVICE) Simulator is used to simulate transient curves; Inspect is used to view the results [18]. An I_D-V_G characteristic of NMOS device is shown in Figure 4. Supply Voltage (V_{dd}) used in this study is 1 V. Table 1 gives various device dimensions and doping values.

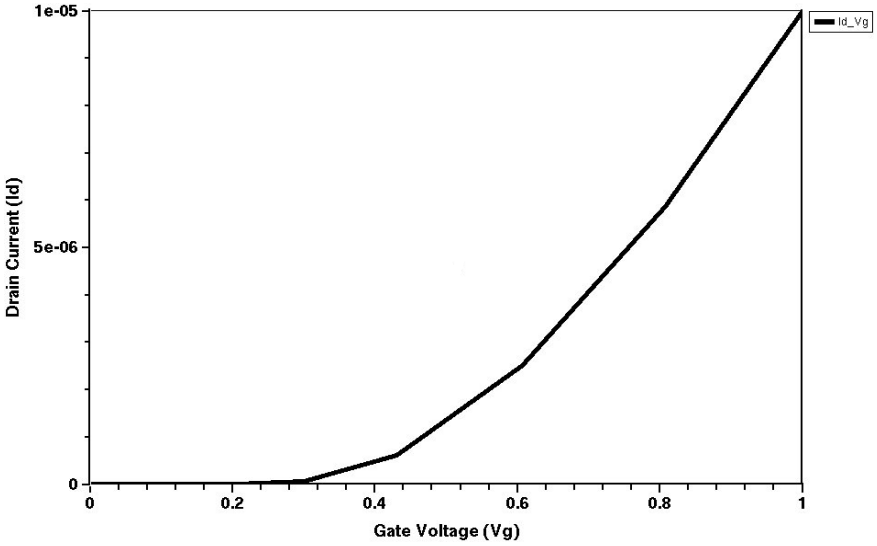

Figure 4. Common Tri-gate JLT NMOS Device I_D-V_G Simulation

Table 1. Device Dimensions

Parameter	Value
Gate Length(L_g)	30 nm
Gate-oxide thickness (T_{ox})	2 nm
Fin width (W)	5 nm
Fin height (H)	5 nm
Underlap ($_{Lun}$)	1 to 5 nm
Channel doping	8× 10^{19}/cm^3 (N transistor)
	2.5× 10^{19}/cm^3(P transistor)
Source-drain doping	8 × 10^{19}/cm^3 (N transistor)
	2.5 × 10^{19}/cm^3 (P transistor)

3. Junctionless 6T SRAM Structure

JLT is a multigate FET with neither N^+P nor P^+N junctions. Unlike a MOSFET, for a JLFET channel the doping concentration and type are equal to ($N^+N^+N^+$) in the source- channel-drain region. Since this device has no concentration gradient in the lateral direction of the conduction layer, it does not have any p–n junction. The doping concentration used in JLT is typically in the range of 10^{19} cm^{-3}, uniform, and homogenous across the source (S), channel, and drain (D) region.

A JLT 6T-SRAM cell is designed by replacing the conventional MOSFETs or SOI (silicon-On-Insulator) FinFET based multi-gate transistors with jnless transistors. The generated 6T-SRAM structure from SDE is shown in Figure 5. Meshing is shown on one-side of the device namely (N2, ACC2, P2 transistors) in Figure 5. In this new design approach, trigate jnless device provides gate controllability on three sides. Using a trigate device architecture it is possible to turn the device on and off to obtain MOSFET- like electrical characteristics.

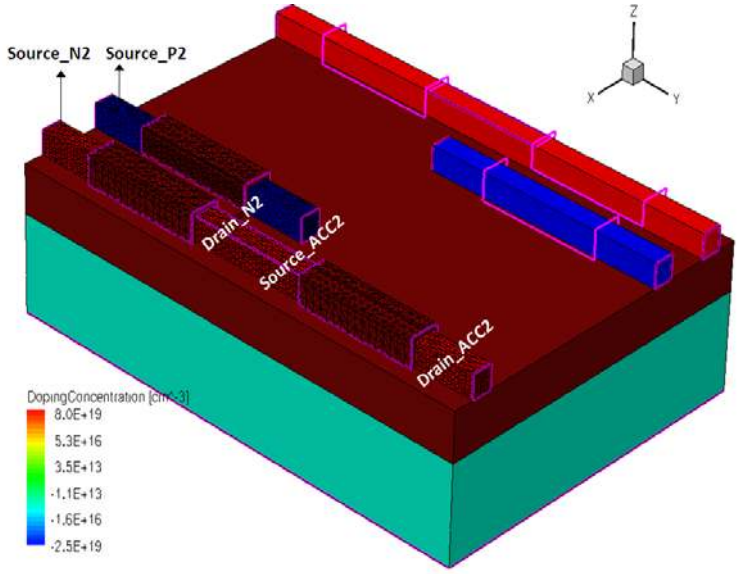

Figure 5. Common Tri-gate JLT 6T-SRAM Structure

In this work, JLT based 6T-SRAM is subjected to heavy ion based SEU radiation. Minimum radiation dose required to flip the cell is found out by doing the transient simulations with radiation models turned-on in TCAD device simulator. Figure 6 shows 6T-SRAM operation simulation curve before SEU radiation. Mixed mode simulation approach is used in SRAM simulation. In mixed mode simulation some portion of the circuit can be simulated at the device level and some part of the circuit can use compact models. In this study, interconnects are assumed to be perfect interconnects. The details of rise and fall time, pulse width of data and access pulses used in SRAM simulation are given in Table 2.

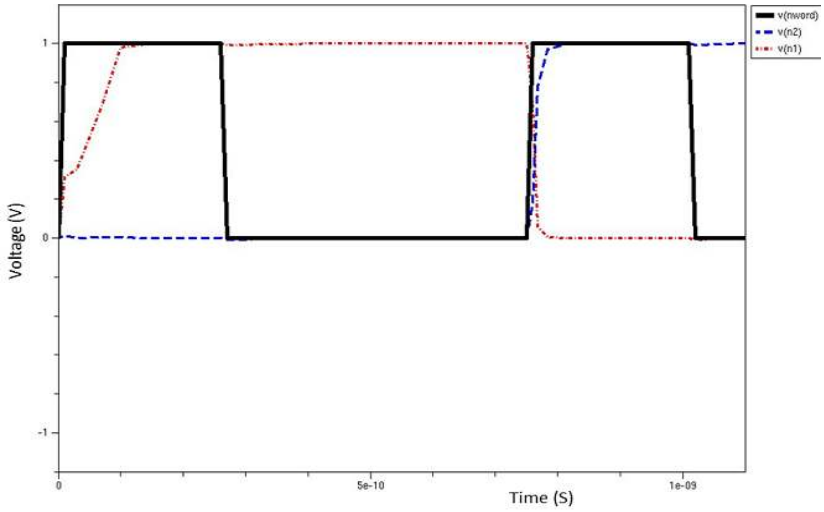

Figure 6. 6T-SRAM simulation

Table 2. Data and Access Pulse Timings

nbit(data)			n(word)		
Rise Time(pS)	Fall Time(pS)	Pulse Width(pS)	Rise Time(pS)	Fall Time(pS)	Pulse Width(pS)
10	10	500	10	10	250

4. SEU Radiation Effects and Results

The simulation of SEU caused by a heavy ion impact is activated by using the proper keyword ('HeavyIon') in the physics section of SDEVICE. The characteristics of the heavy ion like direction, characteristic radius, dose value or Linear Energy Transfer (LET in pC/μm) and strike location can be specified. The heavy ion strikes at location with direction of motion of ions from top to bottom along vertical axis. Length of the ion track is 0.035 μm, characteristic radius w_t = 0.01 μm. Heavy ion bombardment is initiated in the simulation during non-access period at the drain region which has logic value '1'.Figure 7 shows node voltages after heavy ion strike at t=275 ps for LET = 0.04 pC/ μm. By properly choosing LET value the state of the cell can be flipped as shown in Figure 8. The minimum required LET value to flip the cell is of our interest. In Table 3, the L_{un} Vs LET is shown for 1 to 5 nm. The LET value difference between L_{un} 1 to 5 nm is only one–fold magnitude difference due to less variation in the channel resistance [19].

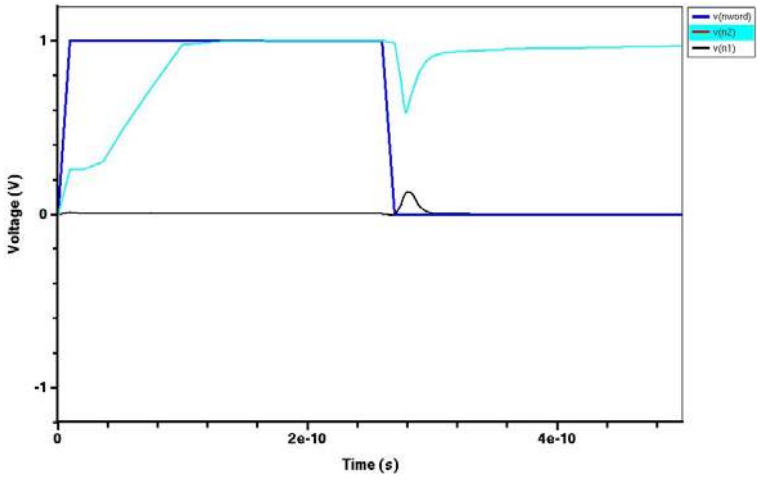

Figure 7. Node Voltages after Heavy Ion Strike at 275 ps for LET= 0.04 pC/μm

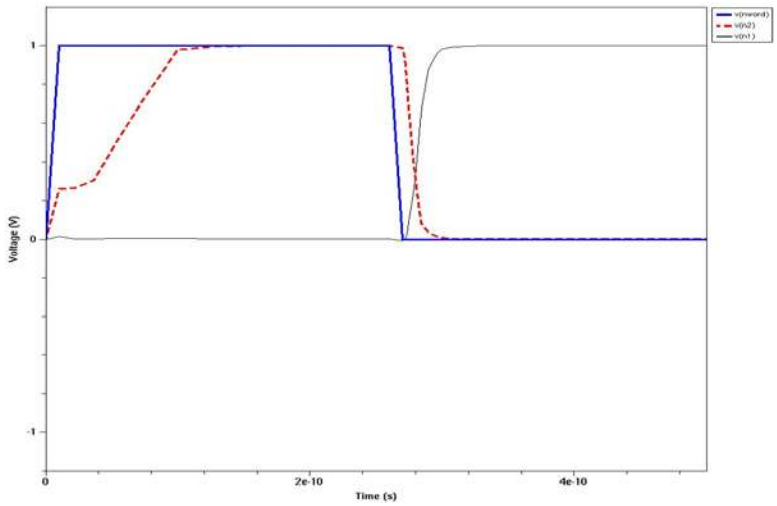

Figure 8. Node Voltages after Heavy Ion Strike at 275 ps (LET= 0.05pC/μm)

Figure 9 and 10 shows the heavy ion generation, heavy ion charge density and electro-static potential distribution across the tri-gate Jnless 6T-SRAM structure which switches its state at dose/LET value of 0.05 pC/μm for L_{un} = 1, 2 nm and 0.06 pC/μm for L_{un} = 3, 4, 5 nm. There are various parameters like electron and hole densities, electron and hole current densities, electro-static potential, SRH recombination rate etc. can be analyzed to study the SEU radiation effects. Figure 11 (L_{un} =1,2 nm) and Figure 12 (L_{un} = 3,4 & 5 nm) shows SRH recombination rate across the structure at three different time instants, i.e. @250 pS, @275 pS, and @330 pS. These time instants correspond to pre, peak and post radiations. It can be observed from Figure 11 and 12 that SRH recombination rate is very low for pre and post radiations.

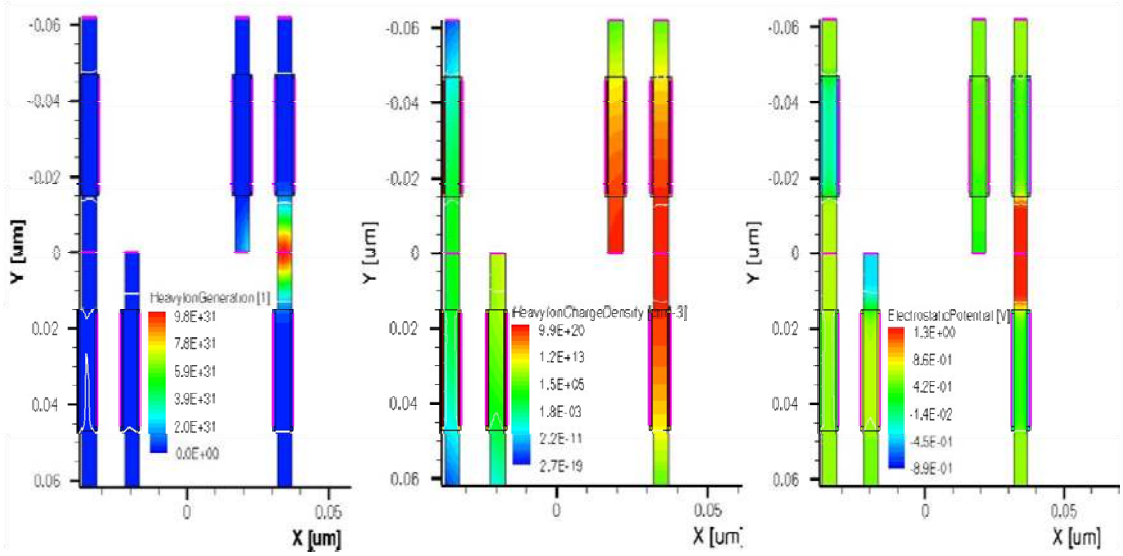

Figure 9. 2D profile of HeavyIonGeneration, HeavyIonChargeDensity, Electrostatic Potential of Tri-gate JLT 6T-SRAM structure at 275 pS (LET= 0.05 pC/μm for L_{UN} = 1 and 2 nm)

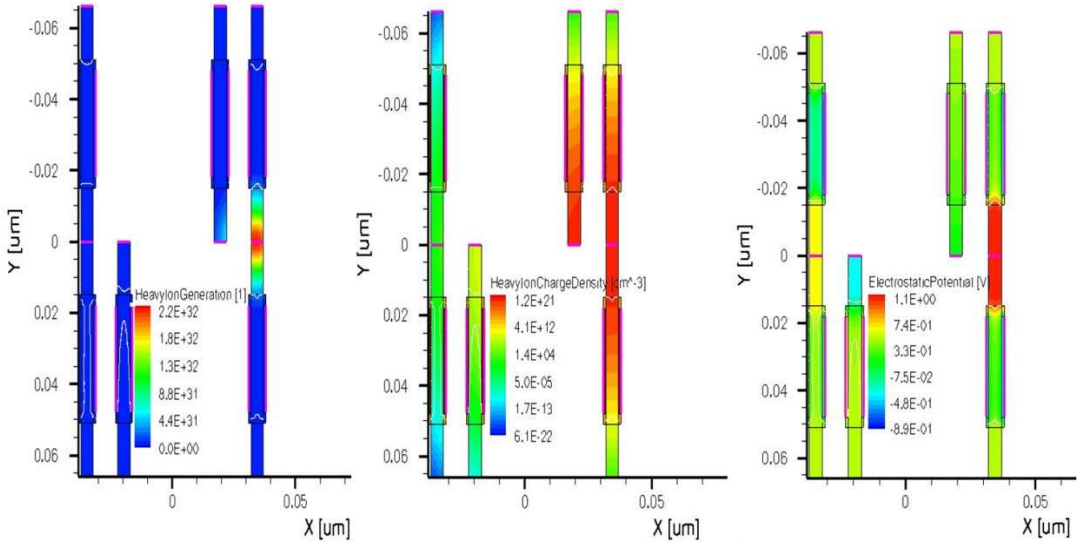

Figure 10. 2D profile of HeavyIonGeneration, HeavyIonChargeDensity, ElectrostaticPotential of Tri-gate JLT 6T-SRAM structure at 275 pS (LET= 0.06 pC/μm for L_{UN} = 3, 4 & 5 nm)

Table 3. Lun Vs LET value

L_{un} (nm)	LET (pC/μm)
1	0.05
2	0.05
3	0.06
4	0.06
5	0.06

As we increase the L_{un} from 1 to 5 nm the HeavyIonGeneration increases from 9.8e31 to 2.2e32 to flip the cell. This indicates higher LET is required for increasing L_{un}. In the similar way, the HeavyIonChargeDensity increases as L_{un} increases. It is also noted that HeavyIonChargeDensity increases from $9.9e^{20}$ to $1.2e^{21}$ $cm^{-1}s^{-1}$ to flip the cell. This also indicates higher LET is required. Electrostatic potential after the strike gets modified depending on the generated heavyion charge density. It is observed that it flips the node when it is close to 1V, otherwise critical charge is not sufficient to flip the node.

Figure 11 and 12 shows 2D spatial distribution of SRH recombination rate for Lun 1 to 5 nm. It can be observed from figure 11 the recombination rate is lower for Lun=1 and 2 nm compared to figure 12 for Lun =3,4 & 5 nm. At the strike location, SRH recombination values are given in Table 4. This makes node voltage disturbance is lower in Lun =3, 4 & 5 nm compared to Lun = 1, 2 nm. Hence it requires higher LET to flip the cell.

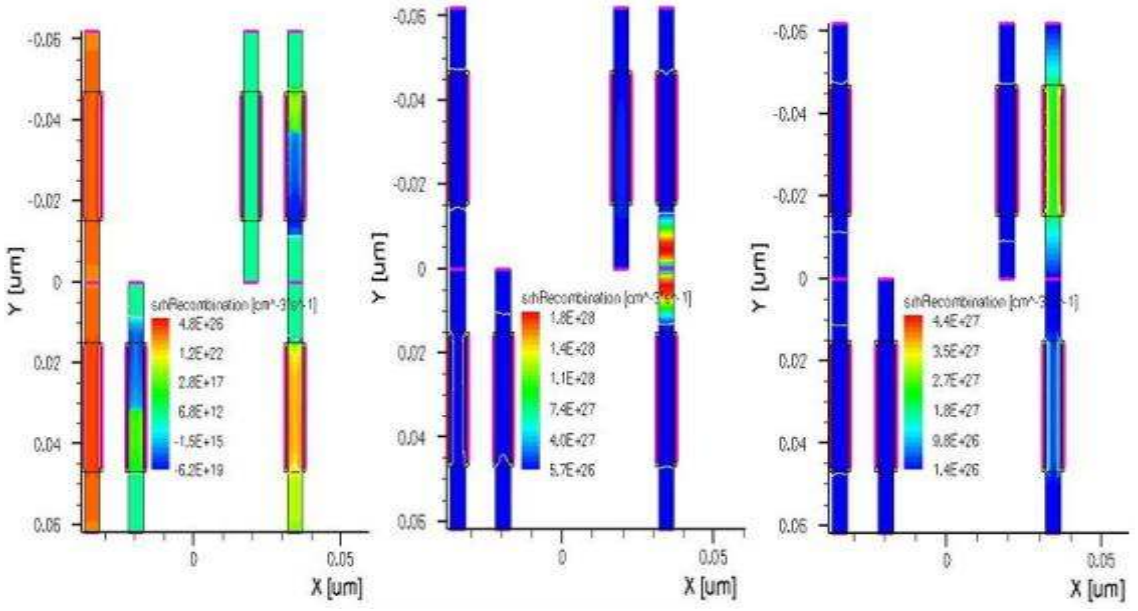

Figure 11. Tri-gate JLT 6T-SRAM SRH Recombination pre-peak-post radiation simulation (LET= 0.05 pC/μm L_{UN} =1 and 2 nm @250ps 275 ps 330 ps)

Table 4. Pre-Peak-Post time SRH Recombination for different Lun values

Pre-peak-post Time (ps)	SRH Recombination value for Lun = 1,2 nm	SRH Recombination value for Lun = 3,4 & 5 nm
250	4.8e+26	5.2e+26
275	1.8e+28	4.1e+28
330	4.4e+27	4.8e+27

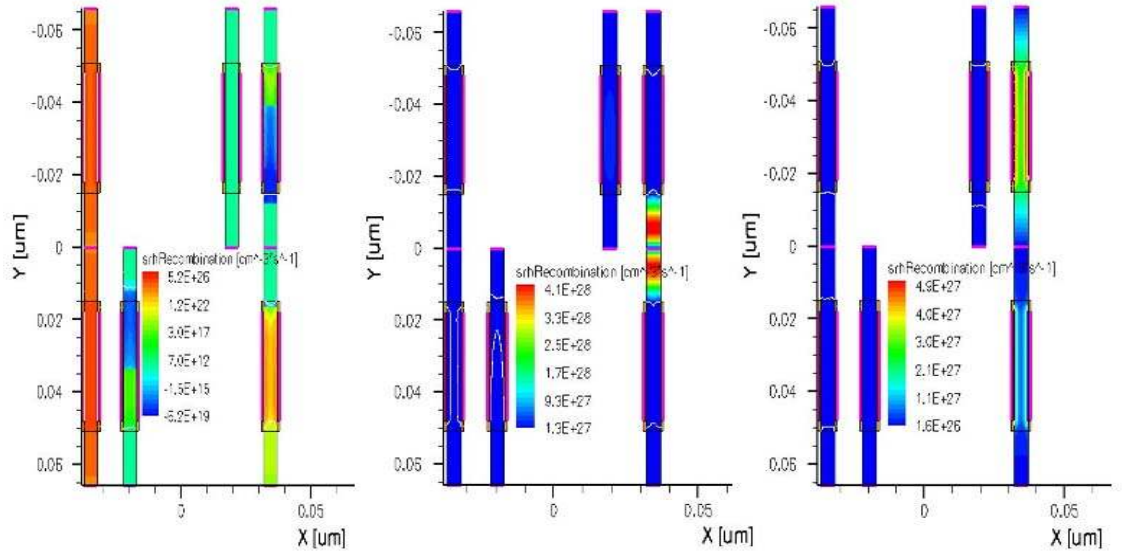

Figure 12. Tri-gate JLT 6T-SRAM SRH Recombination pre-peak-post radiation simulation (LET= 0.06 pC/μm L_{UN} =3, 4 & 5 nm @250ps 275 ps 330 ps)

5. Conclusion

Tri-gate Jnless 6T-SRAM is simulated to study the effect of L_{un} and investigated their SEU/soft error performance (the minimum LET value required to flip the cell) in TCAD. The LET required to flip the Jnless 6T-SRAM is observed and the value is found to be between 0.05 pC/ μm for L_{UN} = 1, 2 nm and 0.06 pC/μm for L_{UN} = 3, 4, 5 nm. The simulation result analyzes electrical and SEU radiation parameters to study its impact on JLT based 6T-SRAM memory circuit.

References

[1] Baumann RC. Radiation-Induced Soft Errors in Advanced Semiconductor Technologies. *IEEE Transactions on Device Material Reliability*. 2005; 5(3): 305- 316.
[2] Petersen EL, Shapiro P, Adams JH, Burke EA. *Calculation of Cosmic-Ray Induced Soft Upsets and Scaling in VLSI Device.* 1982; 29(6): 2055–2063.
[3] Kartik M. *Simulation of transients caused by single-event upsets in combinational logic*. International Test Conference, 2005; 37: 3.
[4] Lianlian Z, Beckett P. *Soft Error Rate Estimation in Deep Sub-Micron CMOS*. 13th Pacific Rim International Symposium on Dependable Computing. 2007*:* 210-216.
[5] Prashant KS, Navakanta B. SEU Reliability Improvement Due to Source-Side Charge Collection in the Deep-Submicron SRAM Cell. *IEEE Transactions on Device and Materials Reliability.* 2003; 3(1): 14-17.
[6] http://public.itrs.net.
[7] Palkesh J, Juzer V, Rakesh K. Lal. SEU Reliability Analysis of Advanced Deep-Submicron Transistors – Introduction. *IEEE Transactions on Device and Materials Reliability.* 2005; 5(2): 289-295.
[8] Hen C, Er E, Soh PN, Loh SK, Wang Q, Teong J. *Failure Analysis of 65nm Technology Node SRAM.* International Symposium on Physical and Failure Analysis of Integrated Circuits. 2008: 1-4.
[9] Labonnah FR, Mohammad FBA, Mamun BIR, Mohd. Marufuzzaman, Hafizah H. Advances on Low Power Designs for SRAM Cell. *TELKOMNIKA Indonesian Journal of Electrical Engineering*. 2014; 12(8): 6063-6082.
[10] Jatmiko ES, Razali I. Design of Double Gate Vertical MOSFET using Silicon On Insulator (SOI) Technology. *International Journal of Nano Devices, Sensors and Systems (IJ- Nano).* 1(1): 34-38.
[11] Munteanu D, Autran JL. 3-D simulation analysis of bipolar amplification in planar double- gate and FinFET with independent gates. *IEEE Trans. Nucl. Sci.* 2009; 56(4): 2083–2090.
[12] Ramakrishnan VN, Srinivasan R. Soft Error Study in Double gated FinFET-Based SRAM Cells with Simultaneous and Independent Driven Gate. *Microelectronics Journal.* 2012; 43(11):888-893.
[13] Ramakrishnan VN, Srinivasan R. Effect of underlap and soft error performance in 30 nm FinFET-based 6T-SRAM cells with simultaneous and independent driven gates. *Journal of Computational Electronics*. 2013; 12(3): 469-475.
[14] Lilienfeld JE. *Method and apparatus for controlling electric current,* 1930, U.S Patent 1 745 175.
[15] Munteanu D, Autran JL. *3D Numerical Simulation of Bipolar Amplification in Junctionless Double-Gate MOSFETs under heavy–ion irradiation.* 12th European conference on radiation and its effects on components and systems. 2011: 73-76.
[16] Ramakrishnan VN, Srinivasan R. *3D Simulation study of Soft Error on Juntionless 6T SRAM.* IEEE International Conference on Innovations in Engineering and Technology, 2014.
[17] Trivedi V, Fossum JG, Chowdhury MM. Nanoscale FinFETs with gate-source/drain Underlap. *IEEE Trans. Electron Devices*. 2005; 52(1): 56–62.
[18] Synopsys Sentaurus Device User Guide Version-A 2008.09
[19] Chi WL, Isabelle F, Aryan A, Ran Y, Nima DA, Pedram R, Jean PC. Performance estimation of junctionless multigate transistors. *Solid-State Electronics.* 2010; 54: 97–103.