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Efficient modeling of barrier resistance for an Improved Lumped Element Model of GaN-based MIS-HEMT gate stack

Narendra Rai, Ashutosh Mahajan, Dipankar Saha, and Swaroop Ganguly

***Abstract*—A methodology has been proposed to accurately model the gate stack of Gallium Nitride (GaN) based metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs). Small-signal analysis has been performed for the device biased in the spill-over region, where electrons accumulate at the insulator/III-Nitride 'critical' interface. Accounting for the barrier layer resistance with an accurate model yields a near but inexact match between simulation and measurement. It is found that the border trap admittance and the energy distribution of the interface trap capture cross section (σ) need to be included in order to achieve a very close one. It is concluded that the interface trap density, extracted using conventional small-signal admittance methods, can be significantly off if these non-ideal effects are not incorporated within the equivalent circuit models of GaN-based MIS-HEMTs.**

***Index Terms*—Aluminum Gallium Nitride, barrier layer resistance, border traps, GaN-based MIS-HEMTs, interface traps, power switching devices.**

I. Introduction

HIGH temperature resilience, high critical electric field, large two dimensional electron gas (2DEG) density and large input voltage swing make the gallium nitride (GaN) based metal-insulator-semiconductor high electron mobility transistor (MIS-HEMT) an attractive candidate for high power RF as well as power-switching applications [1], [2]. However, the lack of a high-quality insulator-semiconductor interface implies a large density of trap states within the gate stack in these devices [3]. This raises performance and reliability concerns, which could inhibit the commercialization and adoption of this technology. Therefore, it is essential to have efficient characterization of these devices, enabled by accurate modeling.

The conventional small-signal conductance (G) and capacitance (C) methods, primarily developed for SiO_2/Si MOS systems [4], are regularly used to extract trap density at insulator/III-nitride (III-N) 'critical' interface (D_{it}), in GaN-based MIS-HEMTs [5]–[8]. However, the MIS-HEMT gate stack has a few additional complexities, which must be correctly understood and modeled.

Firstly, in these buried channel devices, the critical interface is separated from the 2DEG channel by a polarized III-N barrier layer. The corresponding barrier resistance, R_B, can affect the movement of electrons between 2DEG and the critical interface, which will alter the response of interface traps to the applied signal. Thus interface trap information, extracted using the standard small-signal admittance methods, would be inaccurate.

Secondly, there is usually a 2DEG-confining AlN layer in the gate stack, which increases R_B and thereby significantly alters the measured frequency dispersion. The effect of R_B needs to be accurately modeled so as to be separated from the measured admittance for faithful extraction of D_{it}.

Thirdly, Border Traps (BT), also known as oxide states or slow states, can significantly affect frequency dispersion in MIS C-voltage (C-V) and G-V, and thus result in overestimation and distortion of the extracted D_{it}, if they are not included in the device model. These effects have been discussed in [9]–[11]. Through quantitative agreement with measurement, we have extracted a BT density of the order of D_{it}.

Lastly, the extracted D_{it} is profiled against trap energy (E_t) using the characteristic trap response time (τ) (see (1)), usually with a single value for the trap capture cross section (σ). However, in III-nitrides, σ can vary over orders of magnitude within the bandgap [12], [13]. Therefore, the energy distribution of D_{it}, profiled using a single σ, can be expected to be erroneous. This discrepancy could worsen if D_{it} varies rapidly within the bandgap, which is usually the case for III-N. The correct energy distribution of σ is crucial to get an accurate match between simulation and measurement.

Recently, we proposed an improved lumped element model (LEM) for GaN-based MIS-HEMT gate stack [14]. We showed that effective modeling demands both accurate models of component characteristics, e.g. non-linear dependence of intrinsic barrier layer capacitance (C_B) on gate voltage (V_G), and correct equivalent circuit topology. With a complex interplay between C_B, R_B and D_{it}, the proposed model produced a better, albeit still inexact, match with measurement compared to those previously reported [15]–[18]. In this paper, we build on the model proposed in [14], by re-calibrating the resistance of the different components of barrier layer and, more importantly, by incorporating other non-ideal effects, like BT, and the energy distribution of σ. The effect of the series resistance, R_S, is also included. This helps to achieve a near-perfect match. Along the way, we discuss the difficulty of matching using just D_{it} and R_B, and how these were eventually overcome through the incorporation of the aforementioned effects.

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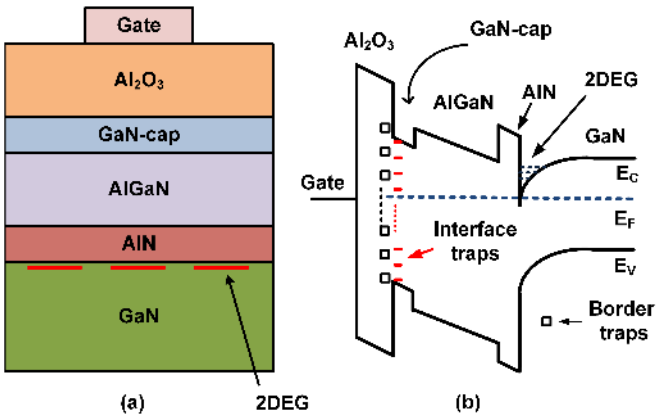

Fig. 1. (a) Schematic of the simulated Al_2O_3 (25 nm)/ GaN-cap (2 nm)/ $Al_{0.25}Ga_{0.75}N$ (17 nm)/ AlN (1 nm)/ GaN MIS diode capacitor [16]. GaN-cap/AlGaN/AlN form the barrier layer. (b) Schematic energy band diagram, showing 2DEG, interface traps and border traps (BT). (reprinted from [14] with the addition of BT in the energy band diagram)

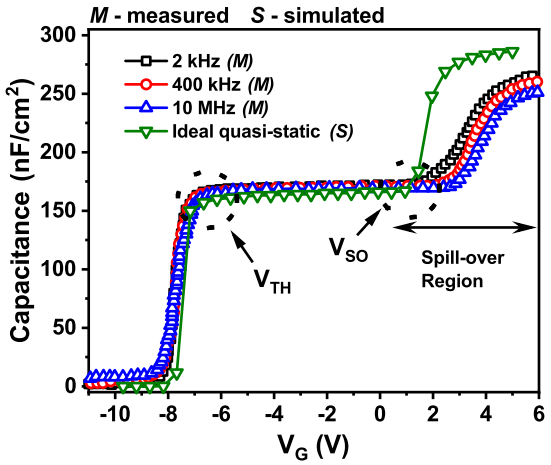

Fig. 2. Simulated ideal quasi-static C-V for the device in Fig. 1(a) along with the measured data at room temperature [16]. (Reprinted from [14])

This paper is organized in the following sections: Section II-A discusses the device structure and capacitance-voltage characteristics over the entire gate bias range. The simulation methodology is outlined in Section II-B. The simulation results with just D_{it} and R_B are given in Section III-A. The challenges faced therein, and their analysis to get an accurate match, are discussed in Section III-B. Section III-C presents the final match with the effects of D_{it}, R_B, σ, BT and R_S incorporated in the model, and is followed by concluding remarks in Section IV.

II. Device Structure, Measured C-V and Simulation Methodology

A. Device Structure and C-V over entire bias range

The schematic of the simulated Al_2O_3 (25 nm)/ GaN-cap (2 nm)/ $Al_{0.25}Ga_{0.75}N$ (17 nm)/ AlN (1 nm)/ GaN MIS diode structure is shown in Fig. 1(a) and the corresponding schematic energy band diagram is depicted in Fig. 1(b). The 2DEG at AlN/GaN and traps at Al_2O_3/GaN-cap interfaces, respectively, are marked, annotating the interface states and border traps. The simulated (S) ideal quasi-static C-V, along with the measured (M) data [16], is shown in Fig. 2. The measured data is at room temperature. It can be seen that the measured capacitance saturates in the accumulation region (i.e., for large V_G). This indicates that gate leakage is negligible, and thus the conductance losses associated with it can be neglected. V_G at which the 2DEG channel forms is the threshold voltage (V_{TH}), and the one at which there is an onset of the second rise in capacitance has been termed as the spill-over voltage (V_{SO}). V_{SO} marks the beginning of the spill-over region.

B. Simulation Methodology

The simulation steps II-B 1(a to d) follow those outlined in [14], with step 1d modified as per the changes introduced in this work. Simulations have been performed using an in-house self-consistent Schrödinger-Poisson simulator built using MATLAB. Material parameters used in the simulations are given in Table I. Mole fraction dependent parameters for AlGaN have been obtained using the expressions given in [23]. Since the aim is to extract insulator/III-N interface properties through small-signal analysis, the focus is only on the spill-over region. LEMs for the device biased in the spill-over region are shown in Fig. 3.

TABLE I
Parameter values used for the simulations (*partially reprinted from [14]*)

Parameter	value
GaN relative permittivity	8.9 [19]
GaN bandgap (eV)	3.4 [19], [20]
AlN relative permittivity	8.5 [19]
AlN bandgap (eV)	6.026 [21]
Al mole fraction in AlGaN (%)	25
Al_2O_3 relative permittivity	8.5
GaN conduction band density of states (N_c) (cm^{-3})	2.2 x 10^{18} [22]
Electron thermal velocity (v_{th}) (cm/sec)	2.6 x 10^7 [22]

We point out that the lumped elements in the model are frequency independent, while the admittance is frequency dependent in the usual way. Thus, the model is valid at all measurement frequencies, as long as the gate stack components can be represented as lumped elements. Here, we have chosen three frequencies, viz. 2 kHz, 400 kHz and 10 MHz, to illustrate the behavior of the proposed LEM at low, intermediate and high frequencies, respectively.

We have defined the D_{it} and BT energy profiles to start from the semiconductor conduction band edge (E_c). This is conventional for simulation studies [9], [10], [24], though measuring trap densities at energies closer to E_c is both difficult and unnecessary, since very shallow interface traps (i.e., traps close to E_c) are fast compared to the typical measurement frequencies, and hence do not contribute to frequency dependent dispersion of the admittance. On the other hand, BT lying close to E_c can contribute significantly to the measured admittance [11]. We find that the extracted interface trap time constant τ is in seconds at $E_c - E_t \sim 1$ eV (E_t is the trap energy at the critical interface). Therefore,

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these deep traps cannot respond to AC signals considered here, viz. 2kHz and higher. Hence, we have depicted the D_{it} and BT profiles only till $E_c - E_t$ = 1.2 eV. The D_{it} and BT profiles beyond these energies are irrelevant as far as room temperature small signal AC behavior of the device is concerned. Simulations have been performed in the following stages:

1) The peaks in C-V and G/ω -V, ω is the angular frequency, are tried to match using D_{it} and R_B for a single value of σ.
   a) Ideal quasi-static C-V (IQSCV) is simulated.
   b) Starting with some initial D_{it} profile, IQSCV is stretched to represent ideal high frequency C-V. D_{it} is then varied till the peak values of low frequency C-V and G/ω -V (2 kHz in this case) are matched. It is found that the amount of D_{it} required to stretch V_G is larger than the one needed to match the curves at low and intermediate frequencies. This is because stretch in V_G is due to all traps which can change their state in response to applied DC bias. R_B has been neglected during this step. Lower frequencies are least affected by R_B, and hence the error in the obtained D_{it} is minimum.
   c) R_B is introduced to obtain an approximate match for the highest frequency C-V and G/ω -V (10 MHz in this case).
   d) Conductance loss at the GaN-cap/AlGaN interface was neglected in [14]. The reasoning given was that the conduction band offset (CBO) at this interface is very small compared to that at AlN/GaN interface and becomes even smaller due to quantum confinement effects in the thin GaN-cap layer. Thus its contribution to the overall barrier layer conductance loss is relatively negligible. However, it seems that CBO at GaN-cap/AlGaN interface significantly contributes to R_B, and its effect has been assimilated in GaN-cap/AlGaN layer resistance, R_b.
2) R_b is increased, and AlN layer resistance, R_{AlN}, is decreased such that R_B remains the same. This removes the mismatch for 10 MHz G/ω -V in the depletion region (i.e., for small V_G).
3) R_B correction cannot simultaneously match the C-V and G/ω -V peaks at 400 kHz. Also, admittance values at lower frequencies are hugely mismatched towards the depletion region. These problems are solved as follows:
   a) D_{it} is lowered to approximately match the 400 kHz C-V.
   b) Energy distribution of σ is introduced to make deeper traps responsive. Profiles of D_{it} and σ are adjusted simultaneously to match the curves in the depletion region.
4) Mismatch over the remaining portions of the spill-over region is removed by the inclusion of Border traps. The effect of series resistance has been included to get the final match.

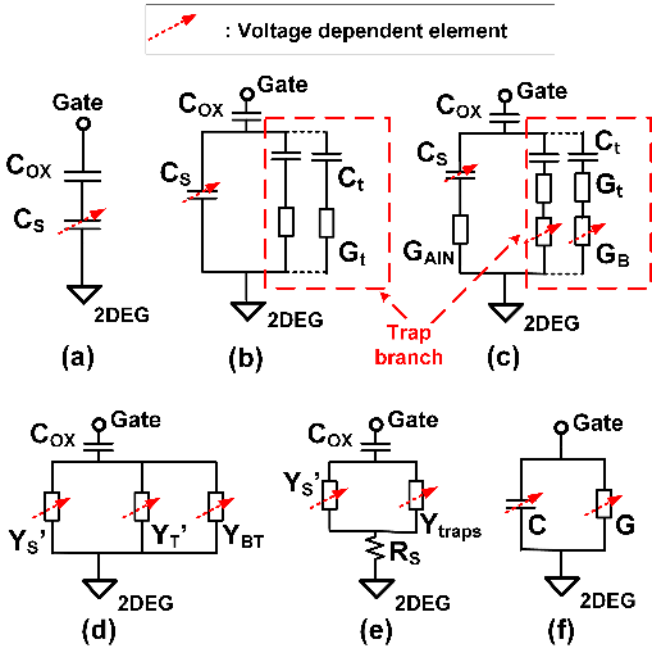

Fig. 3. Proposed LEM for the device in Fig. 1(a) biased in the spill-over region: (a) LEM under quasi-static condition and without traps. (b) LEM with interface traps, but barrier layer resistance, R_B, neglected. (c) Same as (b) with R_B included. (d) Same as (c) with border traps, BT, included. (e) Same as (d) with series resistance, R_S, included. (f) Equivalent LEM consisting parallel capacitance C and conductance G. Legend: C_S is bias dependent barrier layer ideal quasi-static capacitance, C_t and G_t are frequency independent trap capacitance and conductance, respectively, G_B = $1/R_B$ = $1/(R_b + R_{AlN})$ is the conductance of GaN-cap/AlGaN/AlN barrier layer with R_b being the resistance of GaN-cap/AlGaN stack and G_{AlN} = $1/R_{AlN}$ is AlN layer conductance, $Y_S{}'$ is series connection of C_S and G_{AlN}, $Y_T{}'$ is equivalent interface trap admittance in the presence of G_B, Y_{BT} is border trap admittance, Y_{traps}=$Y_T{}'$+Y_{BT}. (Fig. 3(a), (b) and (c) are reprinted from [14]. Note: GaN-cap/AlGaN/AlN and GaN-cap/AlGaN layer resistances were denoted by $R_{B,T}$ and R_B, respectively, in [14].)

III. Simulation Results

We start by reproducing here, in III-A, the results obtained from the "proposed model", given in [14]. Also, we present the matching of 10 MHz G/ω -V data in the depletion region, through the tuning of R_b and R_{AlN}. In the following section, viz. III-B, we discuss the challenges faced when seeking more accurate matching using just D_{it} and R_B. The role of σ is also discussed. Based on these analyses, the required non-ideal effects are incorporated in the model to finally achieve the highly accurate matching, as described in Section III-C.

A. Approximate match using $D_{it,1}$ and R_{B1}

Fig. 4(a) shows C-V curves for interface trap profile $D_{it,1}$ given in Fig. 6. The trap characteristic response time, τ, used in the simulation (see Fig. 6), is given by [4], [15], [25]

$$\tau = \frac{exp(\frac{E_c - E_t}{k_B T})}{\sigma v_{th} N_c} \quad (1)$$

where E_c is GaN-cap conduction band edge, E_t is the interface trap energy level, k_B is the Boltzmann constant, T is the temperature, σ is trap capture cross section, v_{th} is electron thermal velocity and N_c is the effective density of conduction

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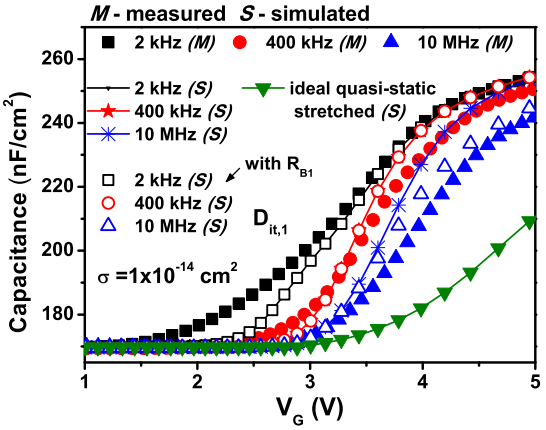
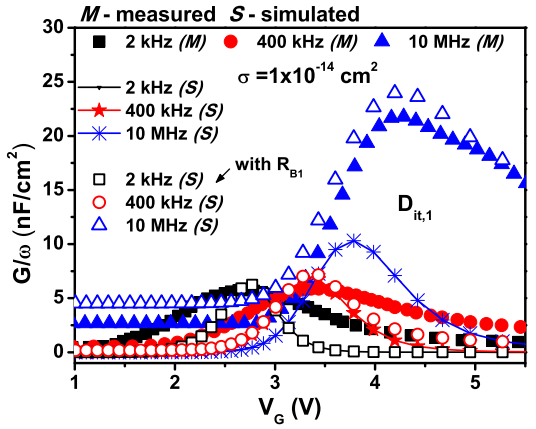


(a)



(b)

Fig. 4. (a) C-V and (b) G/ω -V in the presence of $D_{it,1}$. Note that the simulated 2 kHz C-V and G/ω -V curves, with and without R_{B1}, are lying on top of each other. The same is true for the simulated curves at 400 kHz. $D_{it,1}$, τ and R_{B1} profiles are shown in Fig. 6. R_{AlN}=2.5 mΩ·cm^2 gives the match at 10 MHz. (reprinted from [14])

band states in GaN. $D_{it,1}$ matches the peak values of C-V and G/ω -V at 2 kHz. In the absence of R_B, capacitances overlap in the deep accumulation region. Significant frequency dispersion is present in the depletion region. When R_{B1} is included, C-V for 10 MHz is approximately matched. No effect of R_{B1} is seen at the other two frequencies. Profile for R_{B1} is given in the inset of Fig. 6. The G/ω -V curves are shown in Fig. 4(b). Similar to C-V, only 10 MHz curve is appreciably affected by R_{B1}. Except for the C-V at 400 kHz, the admittance peaks are approximately matched by $D_{it,1}$ and R_{B1}.

The LEMs used to simulate the curves in Fig. 4 are given in Fig. 3(a), (b) and (c). A continuum of interface states is modeled as a parallel connection of defect branches. Each defect branch, which represents an interface trap located at energy E_t, is modeled as a series combination of frequency independent trap capacitance C_t and conductance G_t, which

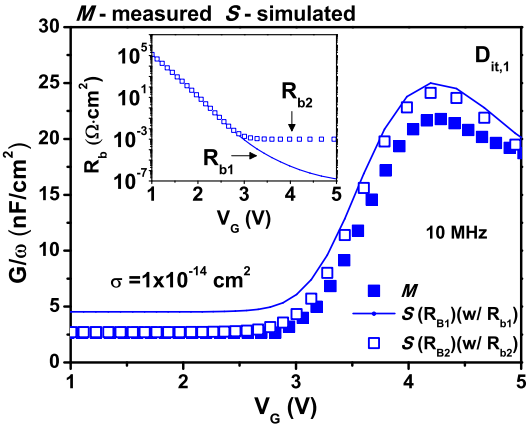


Fig. 5. G/ω -V at 10 MHz for two R_B profiles. R_{B1} contains R_{b1} and R_{AlN}=2.5 mΩ·cm^2 whereas R_{B2} contains R_{b2} and R_{AlN}=1.3 mΩ·cm^2. R_b is GaN-cap/AlGaN layer resistance. Profiles for R_{b1} and R_{b2} are given in the inset. Profiles for R_B are given in the inset of Fig. 6.

are given by

$$C_t = \beta q N_T f_0 (1 - f_0)$$
$$G_t = \beta q N_T c\, n_s (1 - f_0) \tag{2}$$

where $\beta = q/k_B T$, q is elementary charge, N_T is trap density (cm^{-2}), f_0 is Fermi-Dirac trap occupation probability, $c = \sigma v_{th}$ is trap capture co-efficient, n_s is free electron concentration at the insulator/III-N interface (cm^{-3}). The equivalent trap admittance (Y_T) is given by [4]

$$Y_T = j\omega \int_{E_v}^{E_c} \frac{C_t G_t}{j\omega C_t + G_t} \tag{3}$$

N_T is replaced by $D_{it}(E_t)\, dE_t$ in (3). In the presence of R_B, the trap admittance becomes

$$Y_T{}' = j\omega \int_{E_v}^{E_c} \frac{C_t G_{tb}}{j\omega C_t + G_{tb}} \tag{4}$$

where

$$G_{tb} = \frac{1}{R_{tb}} = \frac{1}{R_t + R_B} \tag{5}$$

with $R_t = 1/G_t$. The admittance of ideal branch, with R_B, is $Y_S{}' = j\omega C_S G_{AlN}/(j\omega C_S + G_{AlN})$.

It can be seen in Fig. 4(b) that the 10 MHz conductance curve is slightly mismatched in the depletion region. This is due to the overestimation of conductance loss in the ideal branch and has been resolved by decreasing R_{AlN}. R_b is increased correspondingly to keep R_B unchanged so that the conductance peak remains matched. The resulting conductance curves are shown in Fig. 5. The profiles for R_b are shown in the inset. The curve corresponding to R_{b1} is the same as in Fig. 4(b).

B. Challenges faced in exact matching

From the results shown in Fig. 4, we see that $D_{it,1}$ is able to match the C-V and G/ω -V peaks at 2 kHz, G/ω -V peak at 400 kHz but none at 10 MHz. The introduction of R_{B1}

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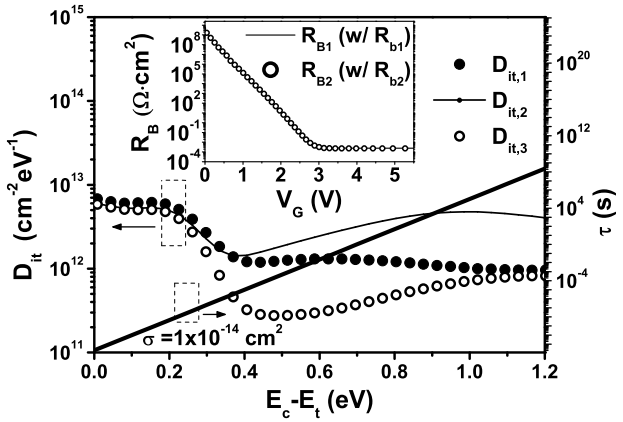
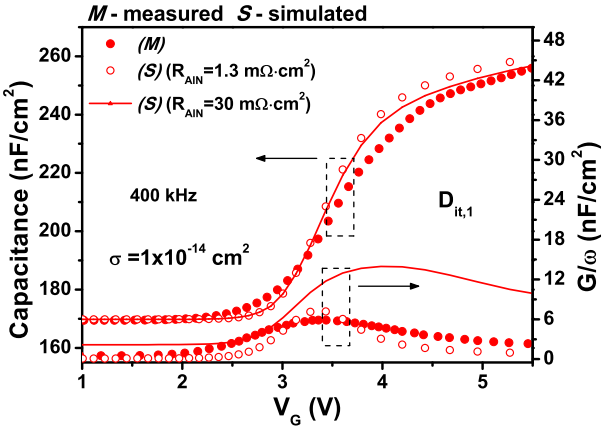
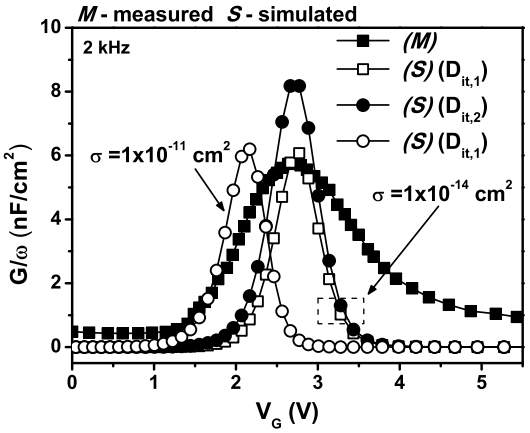


Fig. 6. Interface trap density, D_{it}, profiles used in the simulations. Trap characteristic response time, τ, profile for $\sigma = 1 \times 10^{-14}$ cm^2 is also shown. inset: Profiles for barrier layer resistance. R_{B1} contains R_{AlN}=2.5 mΩ·cm^2 and R_{b1}, whereas R_{B2} contains R_{AlN}=1.3 mΩ·cm^2 and R_{b2}. The profiles for R_b are given in the inset of Fig. 5. $D_{it,1}$, R_{B1} and τ profiles are reprinted from [14].



(a)



(b)

Fig. 7. (a) 400 kHz C-V and G/ω -V for two values of R_{AlN}. (b) 2 kHz G/ω -V for two profiles and values of D_{it} and σ, respectively. The profiles for D_{it} are shown in Fig. 6.

approximately matches the peaks at 10 MHz. The discrepancy in 10 MHz G/ω -V, in the depletion region, goes away when R_{B2} is used. However, no noticeable effect of R_{B2} is seen on 400 kHz admittance curves. We try to match the 400 kHz C-V using a larger value for R_{AlN}. The result is shown in Fig. 7(a). It can be seen that if the capacitance is reduced by increasing R_{AlN}, then conductance peak rises. Any further increase in R_{AlN} will only increase the mismatch.

Though the maximum values of 2 kHz curves are matched by $D_{it,1}$, discrepancy still remains on either side of G/ω -V peak. Fig. 7(b) shows 2 kHz conductance curves for two different profiles and values of D_{it} and σ, respectively. The D_{it} profiles are shown in Fig. 6. For σ=1x10^{-14} cm^2 and $D_{it,2}$, the peak increases, but there is not much effect on the breadth of the curve. For σ=1x10^{-11} cm^2 and $D_{it,1}$, the entire curve shifts to the left.

Following inferences can be made from the above observations:

1) If the peak value of 2 kHz C-V is matched using D_{it} alone, it overestimates 400 kHz C-V. In such a situation, C and G at 400 kHz cannot be simultaneously matched for any value of R_B. Thus, D_{it} has to be reduced, and contributions from other traps have to be considered.
2) Change in occupancy of traps, in response to the applied signal, is associated with energy loss, which is measured as conductance, G. Increase in D_{it} increases G, as shown in Fig. 7(b). Increase in σ decreases trap response time, τ, at all energies. This enables deeper traps to respond and add to conductance, whereas the shallower ones become too quick to cause any energy loss. This explains the leftward shift in 2 kHz G/ω -V curve in Fig. 7(b). Thus, D_{it} and σ have to be adjusted simultaneously to get the match in the depletion region.
3) It is obvious that in addition to correct profiles of D_{it} and σ, the contribution from other traps is still needed to get the match over remaining portions of the spill-over region.

C. Near-exact matching

Based on the analysis given in Section III-B, we start the simulations with a lower value of D_{it}, viz. $D_{it,3}$. The corresponding C-V is shown in Fig. 8(a), where the capacitances, without R_{B2}, can be seen overlapping at 400 kHz. With R_{B2}, 10 MHz C-V is matched. The $D_{it,3}$, R_{B2} and τ profiles are given in Fig. 6. Similarly, the 10 MHz conductance curve, see Fig. 8(b), is almost matched. No significant effect of R_{B2} is observed at 2 kHz and 400 kHz.

To obtain a match in the depletion region, at 2 kHz and 400 kHz, the adjusted σ profile, viz. 'fitted σ', is introduced in addition to $D_{it,3}$. The corresponding C-V and G/ω -V curves are shown in Fig. 9. Profile for 'fitted σ' is given in Fig. 11. The energy distributions of $D_{it,3}$ and 'fitted σ' have been obtained by matching the 2 kHz C-V and G/ω -V in the depletion region. The effect of R_B has been neglected during this step. The range of R_B values used in this work has not shown any effect at 2 kHz, and it is safe to say that the obtained 'fitted σ' profile contains minimum error.

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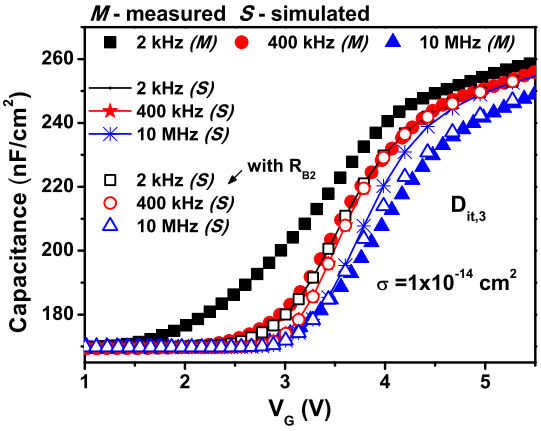
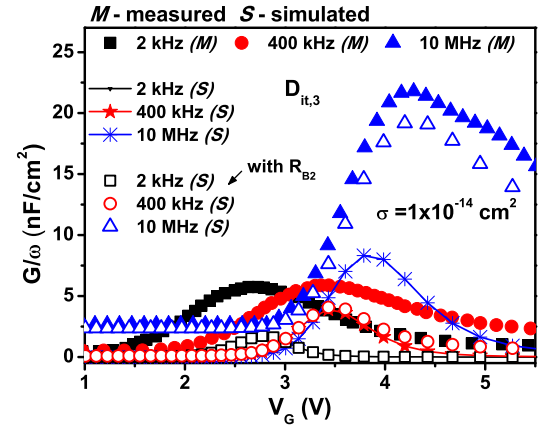
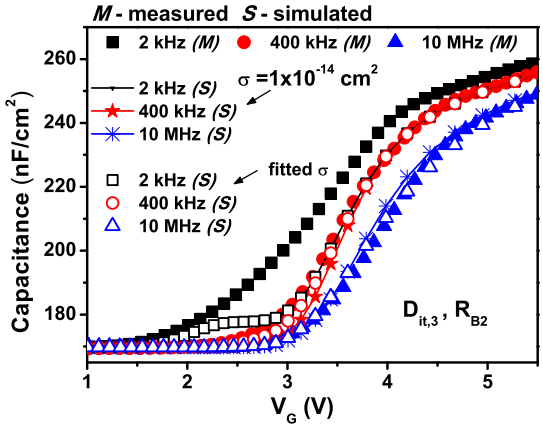


(a)

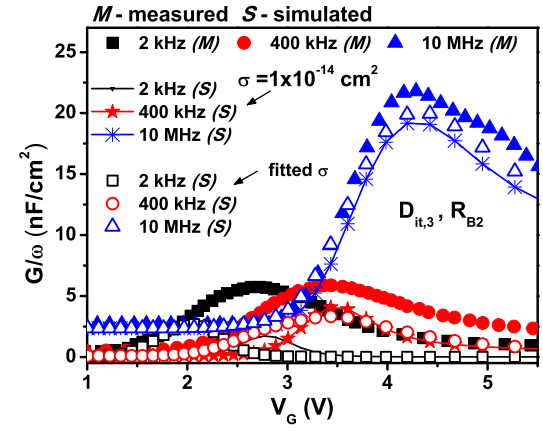


(b)

Fig. 8. (a) C-V and (b) G/ω -V for $D_{it,3}$. R_{B2} gives approximate match at 10 MHz. Profiles for $D_{it,3}$, τ and R_{B2} are shown in Fig. 6.



(a)



(b)

Fig. 9. (a) C-V and (b) G/ω -V for $D_{it,3}$ using σ=1x10^{-14} cm^2 and 'fitted σ' (see Fig. 11). R_{B2} gives approximate match at 10 MHz. Profiles for $D_{it,3}$ and R_{B2} are shown in Fig. 6.

We have compared the $D_{it,3}$ profile with other reported insulator/III-Nitride interface trap densities in Fig. 10. The D_{it} profiles labeled 'S. Yang' [16], 'S. Kim' [26] and 'Y. Irokawa' [27] are measured values, whereas 'B. Bakeroot' [24] is a model profile. $D_{it,3}$ is similar in order compared to others over the given energy range. To take a particular example: we applied our model to the measured admittance data from S. Yang et al. [16]. We find that, firstly, they have not considered the admittance contributions from BT while extracting D_{it}, resulting in a higher estimate for the interface trap density. Secondly, they have used a single σ (= 10^{-14} cm^2) to correlate τ to E_t, leading to a D_{it} profile that differs in magnitude and shape from our $D_{it,3}$. It may be useful to reiterate here that, the relevant energy range for interface traps is $E_c - E_t \leq 1.0$ eV, beyond which they are too slow to respond even to kHz AC signals.

It can be seen from Fig. 9 that large discrepancy persists at 2 kHz and 400 kHz. This has been resolved by incorporating admittance contributions from border traps, BT. We have used a model for BT as given in [10]. The LEM with BT is shown in Fig. 3(d), where BT admittance, Y_{BT}, is given by [10]

$$Y_{BT} = j\omega C_{OX} \frac{dV_{SS}}{d\psi_S} \tag{6}$$

where,

$$\frac{dV_{SS}}{d\psi_S} = \frac{q^2}{C_{OX}} \int_0^{w_{OX}} \int_{E_v}^{E_c} K_t(x, E_t) g(x, E_t) \times [1 + j\omega\tau_c(x, E_t)]^{-1} \frac{\partial f}{\partial E_t} \, dE_t \, dx \tag{7}$$

For meanings of the symbols and derivations, one is referred to [9]. $K_t(x, E_t)$ is space and energy distribution of border traps. $g(x, E_t)$ gives the probability that a trap located at energy E_t and depth x will retain its thermal equilibrium occupancy at the time of impedance measurement. x is the distance into oxide from the oxide/semiconductor interface. Based on the arguments made in [10], $g(x, E_t)$ has been taken as '1' for the important terms in (7). w_{OX} is the oxide thickness. The time constant τ_c is given by [11]

$$\tau_c = \tau_{eff} e^{2\kappa_0 x} \tag{8}$$

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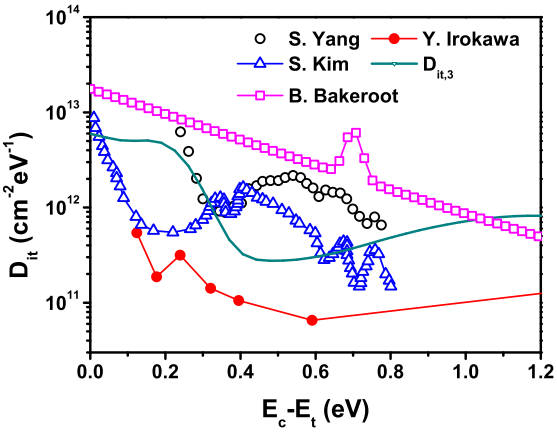


Fig. 10. The $D_{it,3}$ profile used in this work, compared to other insulator/III-Nitride interface trap profiles reported in the literature. D_{it} deeper than 1 eV from E_c is irrelevant for room temperature small signal AC analysis at measurement frequencies of interest.

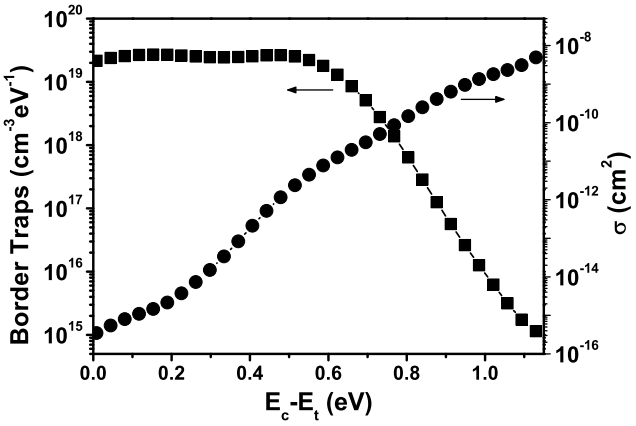


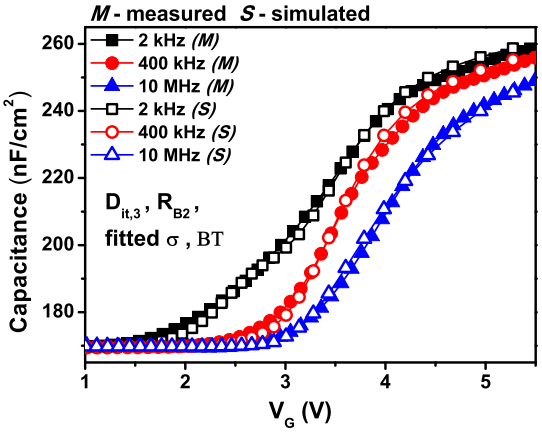
Fig. 11. The profile for Al_2O_3/GaN-cap interface trap capture cross section (fitted σ). The border traps (BT) profile is also shown. E_c is the GaN-cap conduction band edge. A spatially uniform profile has been considered for BT.

where,

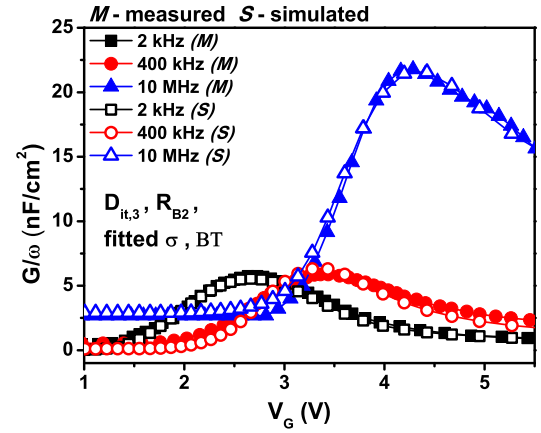
$$\tau_{eff} = \tau + \tau_B$$
$$\tau_B = \frac{C_t}{G_B} \quad (9)$$

$$\kappa_0 = \sqrt{2m^*(E_c^{OX} - E_t)}/\hbar \quad (10)$$

τ_B is the delay introduced by R_B. τ_{eff} is the effective response time of traps at the critical interface. κ_0 is the attenuation coefficient of an electron wave function, at energy E_t, decaying within the oxide. m^* is the electron effective mass in the oxide, E_c^{OX} is the oxide conduction band edge at the oxide/semiconductor interface, and $\hbar$ is the reduced Plank's constant. A range of values has been reported for the Al_2O_3/GaN conduction band offset [20], [28]. A value of 3.3 eV has been used in this work along with m^*= 0.5m_0 [11] to calculate κ_0. The incorporation of BT, in conjunction with $D_{it,3}$, 'fitted σ' and R_{B2}, finally matches the capacitance



(a)



(b)

Fig. 12. (a) C-V and (b) G/ω -V simulated using $D_{it,3}$, R_{B2}, 'fitted σ' and BT. Series resistance, R_S=3×10^{-4} Ω·cm^2, is also included.

and conductance curves as can be seen in Fig. 12. A series resistance, $R_S = 3 \times 10^{-4}$ Ω·cm^2, has been included to get the final match. The corresponding LEM is given in Fig. 3(e). The energy distribution of BT is shown in Fig. 11. We have considered a uniform spatial distribution for BT, up to 2 nm into the oxide. It may be imagined that the measured spatial profile of BT, obtained from the AC transconductance (AC-g$_m$) method [29] say, would also yield a more accurate energy profile for BT. However, such a BT profile may also have some error, since the impact of interface states is not considered in the AC-g$_m$ method [30]. In any case, the bias dependent admittance contribution from BT required to match the measured data remains the same irrespective of the energy and space dependence of their distribution. We assume the simplest spatial distribution and then derive the requisite energy distribution. From the values used in the simulation, it can be seen that BT density $> 10^{12}$ cm^{-2}eV^{-1} is contributing to the device admittance which is otherwise ascribed to D_{it} when extracted using small-signal conductance and capacitance methods. Such order-of-magnitude estimates of BT density, through a reasonable agreement with experimental

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data, have been reported in [10], [31], [32].

IV. Conclusion

We have developed a lumped element model, LEM, of GaN-based MIS-HEMT gate stack by performing small-signal analysis of the device biased in the spill-over region and effectively distinguished the admittance contributions coming from different components of the stack. We observed that the barrier layer resistance, R_B, causes significant conduction loss and appreciably affects the frequency dispersion of the admittance. For the Al_2O_3/GaN-cap/AlGaN/AlN/GaN MIS structure, simulated in this work, portions of the barrier layer, apart from AlN, also contributed significantly to the overall R_B. Thus, directly applying the small-signal admittance methods which had been developed to extract the interface trap density, D_{it}, for SiO_2/Si MOS capacitors, would lead to substantial error in the case of GaN-based MIS-HEMTs.

We find that just D_{it} and R_B are not enough to get an exact match; the correct profile for interface trap capture cross section, σ, is equally important. Approximate profiles for D_{it} and σ can be obtained simultaneously by matching the lowest frequency curves in the depletion region. Low frequency minimizes the effect of R_B, and depletion bias minimizes the contributions from traps other than interface traps.

Along with the interface traps, the contributions from border traps, BT, should also be considered. BT of the order 10^{12} $cm^{-2}eV^{-1}$ has been extracted in this work. This is usually ascribed to D_{it} when extracted using conventional small-signal admittance methods. Thus, it is imperative that the model correctly resolves these two contributions so that the technological root causes can be effectively addressed in experiments.

The model developed in this work effectively highlights the roles played by different components of the gate stack in the overall device admittance. In the process, we have highlighted different ranges of frequency and bias over which particular components are dominant. A near-exact match between simulation and experimental measurement data was finally obtained. This work can guide the development of experimental process techniques to achieve higher quality insulator/semiconductor interfaces for future GaN-based MIS-HEMTs; and aid the development of better techniques to characterize them.

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