Estimation of Lifetime and Reliability of Input Rectifier in Variable Frequency Drives

Estimation of Lifetime and Reliability of Input Rectifier in Variable Frequency Drives

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Abstract. This research paper investigates the causes of power module failures in front-end rectifier of variable frequency drive (VFD) and their lifetime estimation. The front-end rectifier plays an important role in the electrical system for energy conversion. However, from the industrial survey it is found that they are sensitive to harsh operating conditions and are prone to damage. Hence, it becomes inevitable to analyse the causes of their failure and lifetime. Due to prolonged usage, sudden variations in supply and load, the power modules will be subjected to stresses such as overvoltage, voltage variations due to sag, phase unbalance, over current, temperature, harmonics and pre-distortions. The major causes of failure are due to several stresses such as solder joint break, bond wire lift-off, cracks in power modules are discussed. In this paper, the lifetime of the power module is estimated for a given mission profile data. The junction temperature profile is obtained from the VFD Front-end rectifier simulation model. The number of temperature cycles from the temperature profile is estimated using cycle counting methods. Lifetime estimation and damage modelling is done using Coffin-Manson rule and Palmgren Miner rules. All these modelling and simulations are done for a specific VFD power size using MATLAB and PLECS.

Keywords**:** Lifetime estimation, reliability, Power modules, Cycle counting algorithm, VFD, Coffin-Manson rule, Palmgren Miner rule.

1. Introduction

Power converters contributes significant role in energy conversion systems which are widely used in various industrial applications. Reliability of Power semiconductor devices used in these converters is an important criterion for determination of their lifetime. Power converters are deployed in severe operating environment which are prone to various power quality disturbances such as voltage sag and swell, voltage unbalance, harmonic distortion, transients, rapidly changing temperature cycles and grid impedance variations. Power semiconductor devices reliability are mainly dependent on junction temperature variations subjected to thermal stresses due its operating environment, thereby reducing their lifetime. VFD lifetime is recommended based on the reliability of the DC filter capacitors and the Power modules. Front-end rectifiers were not given high priority for reliability in the past. However, in modern day scenario, the failures in the Front-end diodes and SCRs in VFD are getting increased. Input rectifier diodes/SCRs are subjected to various such disturbances and hence electrical, mechanical and thermal stresses vary considerably. Very few research works have been done in these areas.

In small power VFDs, there used to be an integrated Power module which consists of both rectifier and inverter sections designed in the same package. Sometimes, these modules will also have brake chopper built in. So, in this case, compared to the reliability of the front-end components, the IGBT inverters will be poor. However in drives rated beyond certain power range, this structure is not feasible.

The Front-end rectifier/Diode rectifiers will be kept in separate packages. In such case, it is important to know the reliability of this diode/SCR bridge also.

To understand in detail the major causes of concerns during power module usage, both dynamic power and standalone thermal tests are required to be done. Detached thermal cycling tests cause stress within the interconnection between base plate and substrate. Amid dynamic power cycles, there will be stress on bond wires resulting in concerns over solder joints in between the substrate and chip. Amid brief cycles, stress is observed on bonding wires and during long cycles, the chip-solder layer encounters increased stress. Investigations are carried out to understand issues due to stress in temperature such as average temperature, swing in temperature, junction temperature, temperature cycle duration and its impact on power module reliability and lifetime. Many investigations are carried out in bonding technology improvements and lifetime expectation models for checking the unwavering quality of the power module. The unwavering quality and lifetime of the power module is vital concern because it decides the reliability of the whole system [1]. The lifetime of the modules depends on the field of application. Power converter operates in extreme conditions subjected to longer duration of high currents, voltages and temperature swings.

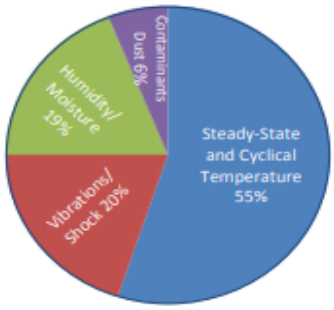

Figure. 1. Stress distribution sources

Analysis of failure mechanism is important criterion to estimate lifetime of power modules. Fig. 1 shows the source of stress distribution in power module. Major contribution of power module failure is random in nature, resulting in thermal stress caused due to increased junction temperature during passive thermal and active power cycling. Solder joints and bonding wires are the weakest interconnections within power module prone to frequent damage. These failures are mainly attributed to various thermal expansion coefficients of different adjacent layers within power module. Fig. 2 shows the failure mode distribution in power module.

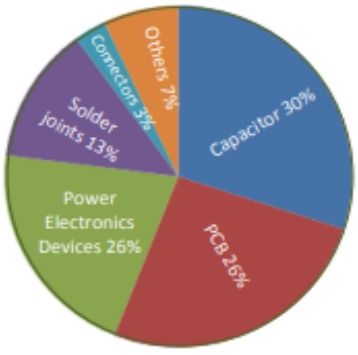

Figure. 2. Failure mode distribution

Lifetime prediction and failure mechanisms of power converters are well understood by creating various electrical and thermal cyclic models, subjected to accelerated life cycle tests carried over entire operating cycles. Analytical models are most suited to estimate lifetime over several cycles until failure, subjected to various factors such as current through bond wires, swing in temperature and the average value of

temperature. Cycle counting algorithms are used to determine the number of cycles and lifetime prediction is suitably modelled.
Three phase front-end rectifier, analysis of failure mechanisms, power modules failure modes, lifetime estimation through various simulation models and analytical methods are detailed in various sections of this investigation. Front-end rectifier in modelled using MATLAB® and PLECS® and the simulation results are discussed in detail.

2. Three phase Front-end rectifier

Three phase rectifiers are commonly used front-end topology in six pulse Variable Frequency Drives. The major parts of VFD are three phase front-end rectifier, control and regulation section, intermediate dc link and inverter as shown in Fig. 3. Front-end rectifiers are the most vulnerable part of VFD in the overall electrical system. Rectifiers must deal with high power and power quality disturbances. Hence, they are subjected to severe damages, stresses due to overvoltage, current and thermal effects. Thus, the reliability of VFD mainly depends on the rectifier reliability. The system reliability can be increased by replacing rectifier components before the components fail. In order to replace at the right moment, the lifetime of the device must be estimated. The estimation involves various testing. The tests must be carried out under different loading conditions considering the harsh environment in which rectifier is in operation.

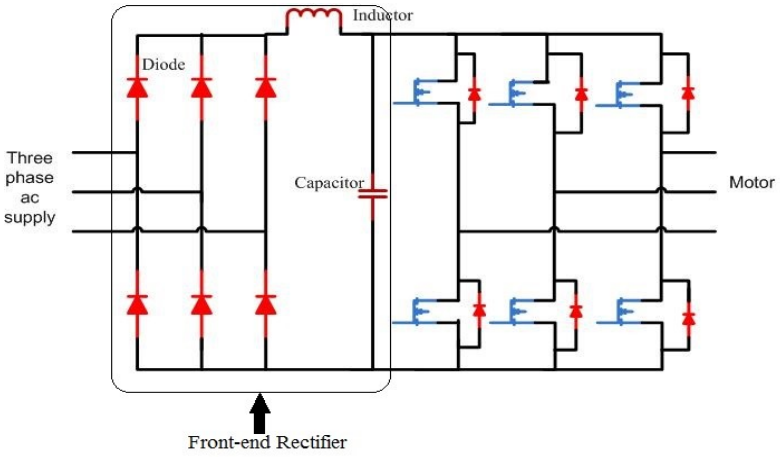

Figure. 3. Front-end rectifier components in VFD

3. Power modules

The foremost dependable operation of front-end rectifiers can be accomplished by the unwavering quality of diode and SCR power modules. Power module as shown in Fig. 4 comprises of distinctive layers each made of diverse materials. Silicon is the main constituent of the device chip and is soldered onto coordinate copper fortified ceramic substrate. This substrate serves as an insulation separator to chip from the metal base plate and scatters heat onto the cooling system framework. For giving electrical contact to the outside circuit, the chip is connected to aluminium bond wires. Chip top is joined with aluminium bond wire. All these materials have diverse CTEs (Coefficients of Warm Development) [1, 2, 3, 5]. The foremost untrustworthy parts in power module are the bonding wires and solder joints. At different loading conditions, power module is subjected to stresses due to increased temperature and variations in voltage and current, thereby resulting in junction temperature increase.

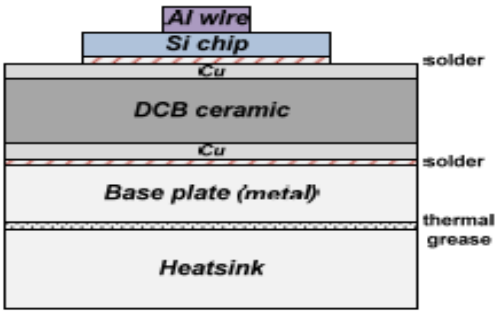

Figure. 4. Layers of Power Module

Dissipation of heat along with change in CTE, tends to lift-off distinct layers within the module thereby accelerating failure of the power module. Various accelerated life tests are conducted to ascertain the reliability of the module under several stress factors. Thereby, module is subjected to uneven temperature distribution and variations. Lifetime of module with its inherent design components can be assessed by subjecting to different tests thereby obtaining the junction temperature and examining the observations through different algorithms. Table.1 shows the co-efficient of thermal expansion of different materials used within the power module.

Table. 1. Coefficient of thermal expansion of different materials in Power module

S No.	**Coefficient of Thermal Expansion**	
	Material	***Value***
1	Al	$23.5*10^{-6}K^{-1}$
2	Al2O3	$6.8*10^{-6}K^{-1}$
3	AlN	$4.7*10^{-6}K^{-1}$
4	Cu	$17.5*10^{-6}K^{-1}$
5	Si	$2.6*10^{-6}K^{-1}$

4. Mission Profile

The temperature swing on the module is the important factor which has significant effect on the lifetime. From several research analysis it is understood that for every 10 °C temperature rise of the module, the failure probability is almost doubled [2, 3, 9, 12]. Hence monitoring temperature of the module gives good insight on the reliability enhancement. Mission profile variations impacts further temperature swings on the module.

Mission profile is the representative voltage pattern applied to the input of on the power module which has significant impact on device performance and junction temperature, thereby module lifetime [17]. Mission profile variations impacts loading stress of the module. Device strength depends on their physical properties. Stress on the device is directly related to device strength, which attributes device failure. These factors directly impact rectifier reliability and lifetime. Mission profile of the module in real time application ensures good lifetime estimation and reliability. The module ought to have way better electro-thermal characteristics. Mission profile transformation to thermal loading of rectifier level ensures reasonable lifetime estimation.

Power quality disturbances in the system has significant contribution in mission profile creation [17]. Mission profile consists of several input parameters such as power supply and environmental conditions including their variations. Various types of voltage sags have been accounted in Mission profile modelling. Voltage sag and types, their classification, occurrence reasons and effects on the system are discussed as below.

4.1. *Voltage Sag*

Voltage sag is the foremost critical power quality issue because it causes antagonistic impacts on the connected equipment's in the utility side [11, 16]. Voltage sag could be a diminish in RMS voltage for brief period caused by different occasions – power system framework faults, sudden energization of the transformer, connected load variations and high-power motor starts. Voltage sag basically happens due to fault current streaming through the power system onto the fault location. Voltage list is well defined by its magnitude, recurrence period and frequency. System impedance of the power system determines sag magnitude.

As per IEEE standard 1159-1995, voltage sag is characterized as a diminish between 0.1 and 0.9 p.u. in root mean square (RMS) voltage at the power frequency for duration length of 0.5 cycles to 1 minute [16].

4.1.1. Voltage sag classification

Voltage sags are classified depending upon the combination of above factors. Table. 2 provides information about the classification of sags.

Table. 2. Classification of voltage sag

Classification of sag	**Factors**		
	Fault type	***Transformer connection***	***Load connection***
Sag A	Three-phase to ground	Δ/Y_g	Y_g connection
Sag B	Single-phase to ground	Y/Y	Y_g connection
Sag C	Single-phase to ground	Δ/Y	Y_g connection
Sag D	Phase to phase	Δ/Y	Y_g connection
Sag E	Two-phase to ground	Y/Y	Y_g connection
Sag F	Two-phase to ground	Δ/Y	Y_g connection
Sag G	Two-phase to ground	Δ/Δ	Y_g connection

Type Sag A incorporates equal voltage drop in all three phases and there's equal 120° phase displacement as this happens due to symmetrical fault. Type Sag B has no voltage drops in Y and B phase wherein there's a drop-in phase R with 120° displacement in phase. Type Sag C sort incorporates voltage drop in R and B phases with no voltage drop in phase Y. As there is no symmetrical fault, the phase displacement between the phases isn't 120°. In type Sag D, the voltage drop is more in R phase compared to Y and B phases. Fault is unsymmetrical and phase displacement isn't 120°. In type Sag E, there's voltage drop in R and Y phases with no voltage drop in B phase, also there's 120° phase displacement among the phases.

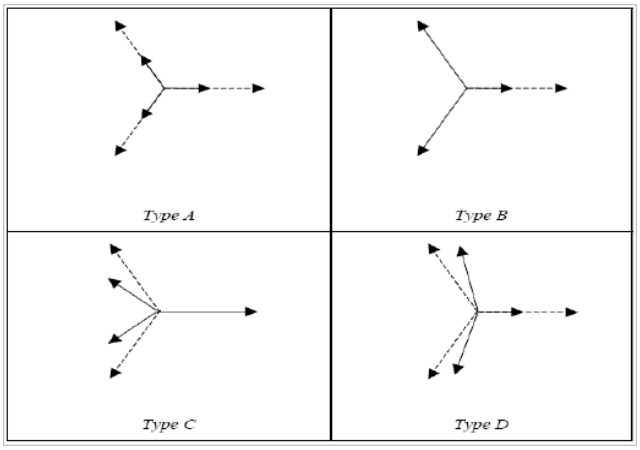

Figure. 5. Voltage sag types and one or three phase faults

Type Sag F has more voltage drop in R phase as compared with Y and B phase, resulting in the phase displacement not as 120°. Less voltage in phases Y and B as compared to phase R and displacement in phase is not 120° [16] (Fig. 5, 6).

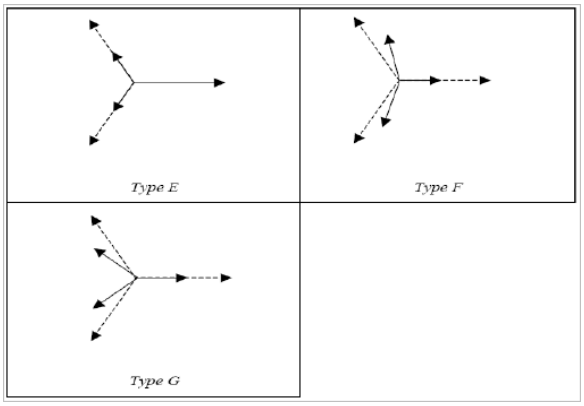

Figure. 6. Voltage sag types and two-phase faults

5. Lifetime estimation

VFD Front - end rectifier module and its lifetime are estimated [15] through proper methodology. Right models provide more accurate results. In this investigation, the following steps are followed.

1. System modelling
2. Thermal modelling
3. Lifetime modelling
4. Damage modelling

Fig.7 shows the flow chart of the lifetime estimation model and interconnecting information between different blocks.

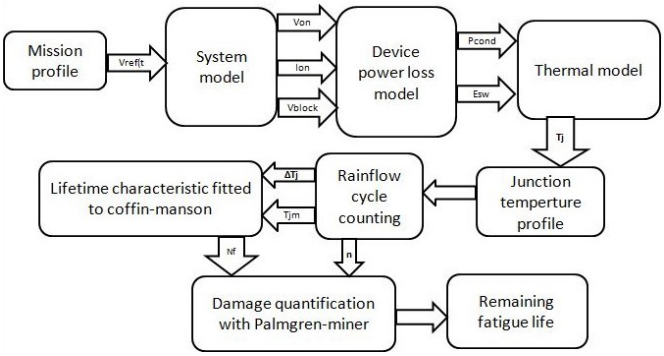

Figure.7. Power module lifetime estimation flow chart

5.1. System modelling

Prior to analyzing the characteristics of the module, circuit is first modelled, its working and characteristics are studied in detail, information are recorded. The system model will be made through use of reliable simulation tool or a mathematical model. The model should provide the resultant electrical data of the Power module based on the operating conditions. The input to the system model is the mission profile data. The loss contributing electrical parameters will be extracted from the system model. A repetitive voltage profile pattern is applied as the mission profile input to the circuit and variations in the module are observed and recorded.

5.2. Thermal modelling

Electro-thermal model is generally designed for establishing junction temperature of the module, switching power losses and conduction losses. Thermal characteristics of the module components can be portrayed by RC models [6, 14,16]. Thermal resistance defines the device ability to resist the heat flow and thermal capacitance defines the capability of the device to absorb or store heat. RC networks like Foster or Cauer (Fig. 8) are being used. Device mathematical modelling through Foster network does not give enough information on the internal structure. However, Cauer model provides physical meaning and needs more information on power module internal structure which is difficult to obtain. Hence the thermal modelling is designed using Foster RC network (Fig.9).

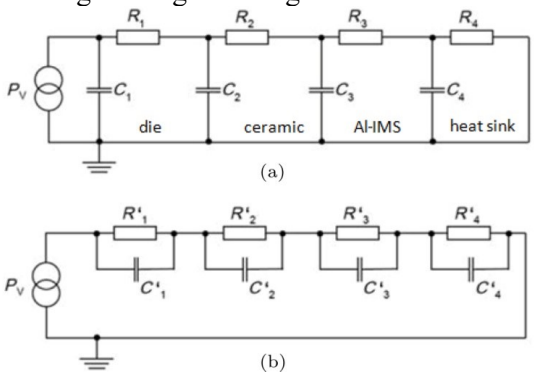

Figure 8. Thermal equivalent of RC Networks (a) Foster network (b) Cauer network

Thermal modelling hence deploys RC network equivalent and thermal coefficients available in the manufacturer's datasheet. Thermal resistances R_{thi} is available in the datasheet and hence thermal capacitance is derived from known thermal time constants τ_i and using the formula as below in equation (1),

$$C_{thi} = \frac{\tau_i}{R_{thi}} \tag{1}$$

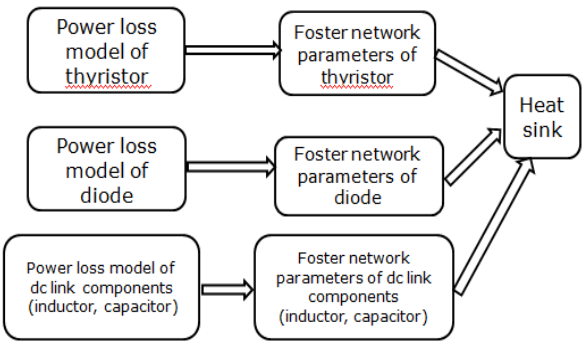

Figure.9. Thermal modelling

5.3. Lifetime modelling

Junction temperature is the most critical criteria in lifetime estimation of the power device. Junction temperature profile is derived from the thermal modelling and is generally irregular. Hence lifetime estimation is done by using suitable cycle counting method along with simulation models which determines fatigue of solders and bonding wires. The extent of damage on the device due to temperature stress is well measured using Palmgren miner rule. Several lifetime models are discussed as below [15].

Various counting methods such as level crossing, simple range, peak and rain flow are in general use. Amongst the popular counting algorithms, rain flow counting is the most commonly used method [7, 8, 15]. Rain flow counting has the unique advantage of reducing irregular temperature profile to simple and regular temperature intervals.

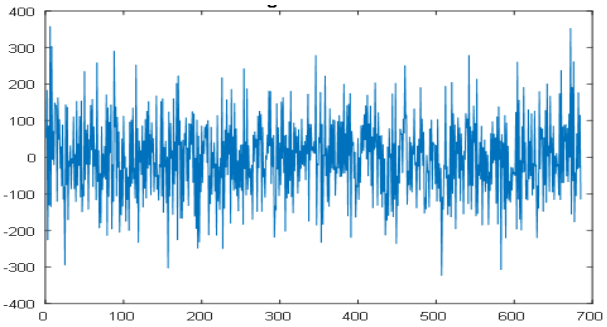

Figure 10. Irregular waveform

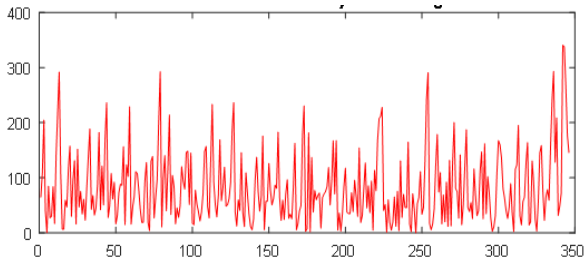

Figure 11. Simplified waveform - Rain flow cycle counting method

5.3.1. Rain flow cycle counting

Among the different counting techniques inside Rainflow method, three-point counting algorithm is being used. This algorithm thus eliminates shorter patterns through regular profile pattern checking (Fig 10, 11). Three consecutive points are being checked to determine completion of cycle [8, 13, 14, 17]. The amplitude and mean value of thermal cycle is calculated by equation (2) and equation (3) respectively.

$$T_{ja} = \frac{|T_{jmax} - T_{jmin}|}{2} \tag{2}$$

$$T_{jm} = \frac{T_{jmax} + T_{jmin}}{2} \tag{3}$$

By knowing the maximum junction temperature T_{jmax} and minimum junction temperature T_{jmin}, the temperature rise can be estimated as shown in equation (4).

$$\Delta T_j = |T_{jmax} - T_{jmin}| \tag{4}$$

5.3.2. Different Lifetime models

Lifetime models [1, 8, 15] are designed in general based on the module thermal characteristics. Various Lifetime models are discussed as below:

- *Coffin Manson model:* Coffin-Manson is used in general to estimate the fatigue caused by solder joints and bonding wires due to temperature changes in every cycle, expressed by equations (5, 6).

$$N_f = A * \Delta T_j^{\alpha} * \exp\left(\frac{E_a}{k_b * T_{jm}}\right) \quad (5)$$

wherein,

N_f – number of cycles due before failure
α – Expression Constant [$K^{-\alpha}$]
ΔT_j – range of temperature [K]
A – general constant
k_b – Boltzmann constant [J/K]
E_a – Activation energy [J]
T_{jm} – Average temperature[K] calculated by expression

$$T_{jm} = T_{jmin} + \frac{\Delta T_j}{2} \quad (6)$$

- *Norris-Landzberg model:* Norris-Landsberg model estimates number of cycles to failure taking into consideration temperature swing and the frequency by equation (7).

$$N_f = A * f^{-n_2}(\Delta T_j^{-n_1}) * \exp\left(\frac{E_a}{k_b * T_{jm}}\right) \quad (7)$$

- *Bayerer model:* Bayerer model is multi-parametric which considers temperature swing ΔT_j, heating time t_{on}, applied DC current I, diameter of the bond D, blocking voltage V and junction temperature T_j to determine number of cycles to failure by equation (8).

$$N_f = K(\Delta T_j^{-\beta_1}) * \exp\left(\frac{\beta_2}{T_j * 273K}\right) {t_{on}}^{\beta_3} * I^{\beta_4} * V^{\beta_5} * D^{\beta_6} \quad (8)$$

K and β are the constants derived through reliability test experiments. Among the above models, the simplest and commonly used model is Coffin-Manson model.

5.4. Damage modelling

Damage modelling is calculated through estimation of accumulated stress on the device. Palmgren miner rule is used to evaluate extent of damage in each cycle and thus calculated as in equation (9).

$$D = \frac{n[i]}{N_f[i]} \quad (9)$$

n_i - the number of identified temperature cycles
j - the number of cycles and half-cycles distinguished from the history
N_{fi} - the number of cycles to failure computed with Coffin-Manson law

However total damage is expressed as sum of damage caused every cycle as shown in equation (10). The device is expected to be failed [1, 8, 17] whenever total sum equals to 1.

$$D = \sum_{i=1}^{j} D[i] \quad (10)$$

5.5. Lifetime Estimation

Device lifetime can be estimated by understanding in detail the interval and total damage over the duration of entire cycle as shown in equation (11).

$$L = \frac{T_0}{D} \tag{11}$$

T_0 – cycle interval
D – Total damage over the entire cycle

Hence, the lifetime of VFD front-end rectifier is estimated through suitable design of system and electro-thermal model. These models are subjected to various mission profiles to analyse various device parameters mainly junction temperature. From the junction temperature profile lifetime is established by using Rain flow counting strategy, Coffin-Manson law and Palmgren miner rule.

6. Simulation results

VFD front-end rectifier is suitably modelled using MATLAB and PLECS software (Fig. 12). Thermal model of the front-end rectifier in specific is done using PLECS (Fig.13). PLECS software has built-in options for entering device data obtained from the manufacturer datasheets within the framework of multi-dimensional lookup tables and thereby losses are estimated.

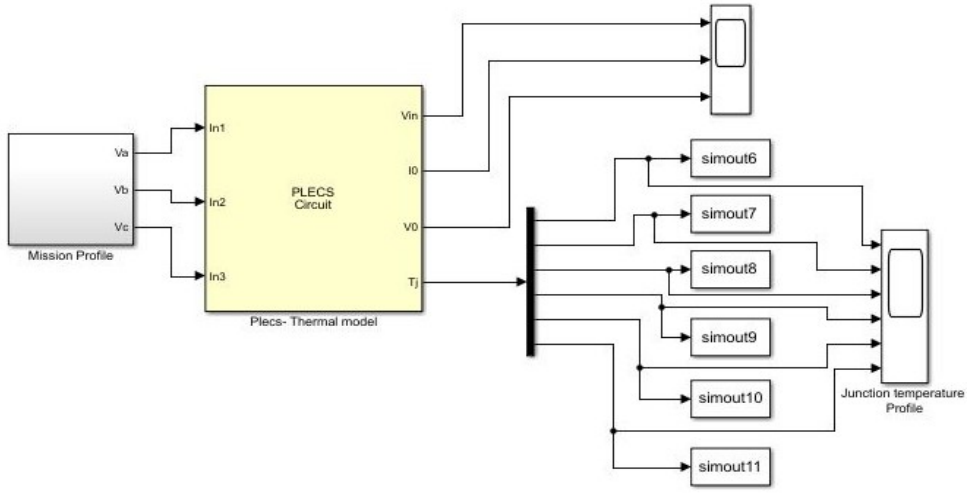

Figure. 12. Front-end rectifier MATLAB-PLECS model for lifetime estimation

Table 3. Specifications of the components used in the circuit

S.No	Component	Specification
1	Front-end Diode	MCD 162-16io1
2	VFD DC inductor (L)	181µH
3	VFD DC capacitor (C)	4700µF

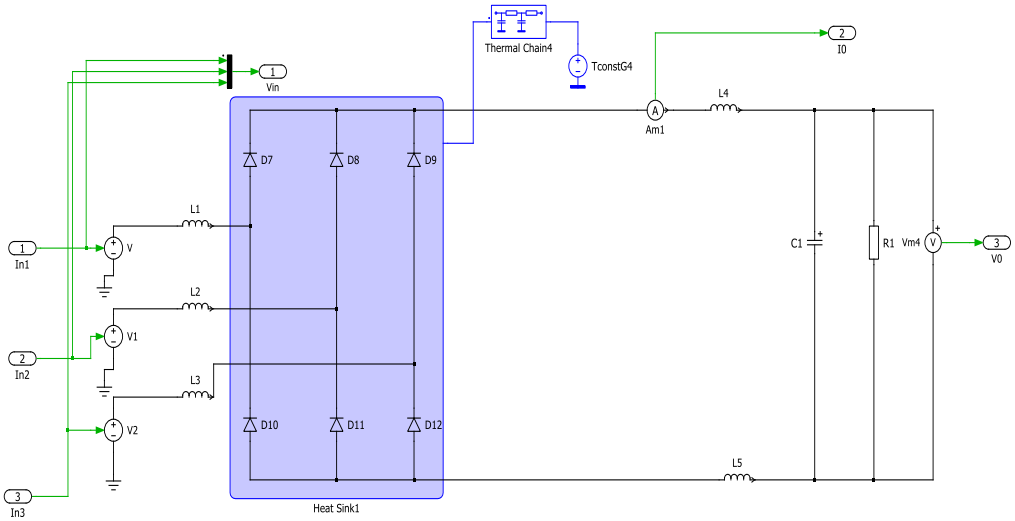

Figure. 13. Front-end rectifier Electro-thermal modelling: PLECS

The simulation is run for T_0 = 1000 s to analyse the damage accumulated for a considerable period and to analyse the model on the occurrence of voltage sag for few cycles at various instants of time. The specifications of the VFD and its components used in the simulation circuit are mentioned in Table. 3.

7. Mission profile

Three phase 415V, 50 Hz is fed as input supply to the system under investigation. Grid impedance plays significant role in establishing the stability and lifetime of the system. Grid impedance can be established from the short circuit ratio of the system. Short circuit ratio (SCR) is defined as the ratio of RMS current produced in the system to the nominal current of the system.

Short circuit ratio determines the voltage distortion and the stability of the grid. Short circuit ratio is taken into consideration to determine the distortion in the voltage. Higher impedance at the input minimizes the distortion in the supply. Lower the SCR, source impedance will be high. The test is done on front-end rectifier of a VFD. The nominal current of the drive for 415 V, 50 Hz input supply is found to be 37.56 A.

The source inductance is calculated for two different short circuit ratios. The source impedance is calculated and with available data system is modelled, simulation is carried out with mission profile as input supply without any disturbance (Fig. 14) and with voltage sag (Fig.15) for SCR as 20 and 120.

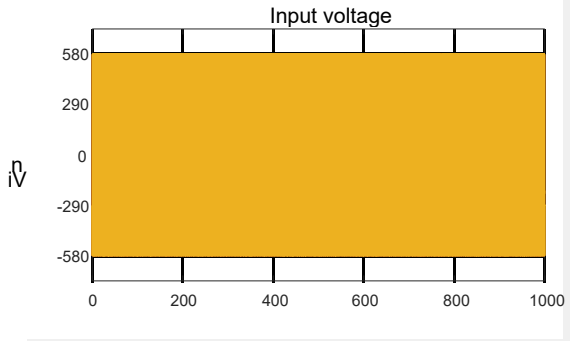

Figure. 14. Input supply without any disturbance

The voltage sag is generated at various instants throughout the loading profile to the system. Amplitude of the voltage sag is about 0.1 to 0.9 p.u. of the nominal voltage for a duration of few cycles to few minutes during its occurrence. During the simulation, voltage sag is generated at few instants for a

duration of 60s, 50s, 40s, 20s and 40s with reduction in the nominal voltage wherein the voltages are 0.5 p.u., 0.2 p.u., 0.7 p.u., 0.4 p.u. and 0.8 p.u. of the nominal voltage respectively.

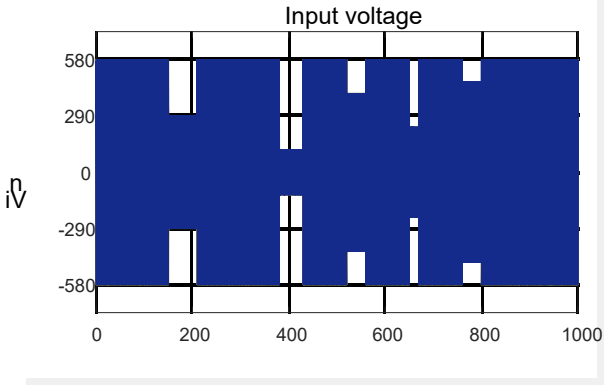

Figure. 15. Input supply with voltage sag

8. System model results

VFD front-end rectifier is suitably modelled using MATLAB and PLECS software. Front-end rectifier diode electrical parameters are updated in the lookup table of PLECS. This data corresponds to diode MCD 162-16io1 considered in this investigation.

9. Thermal model results

Thermal modelling of the device is developed using Foster RC network. However, thermal resistance values are obtained from diode manufacturer datasheet (Table.4). Thermal capacitance values are

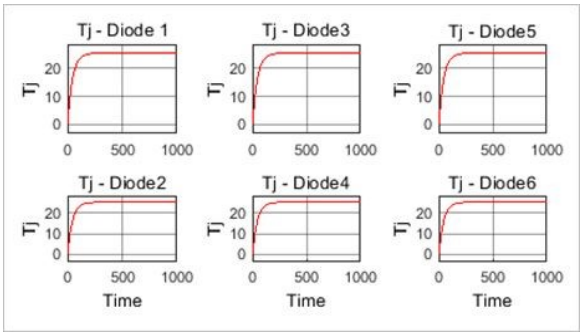

Fig.16 Thermal results for Rsce=20 without Sag

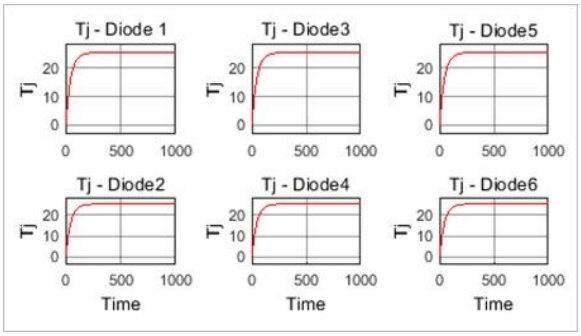

Fig.17 Thermal results for Rsce=120 without Sag

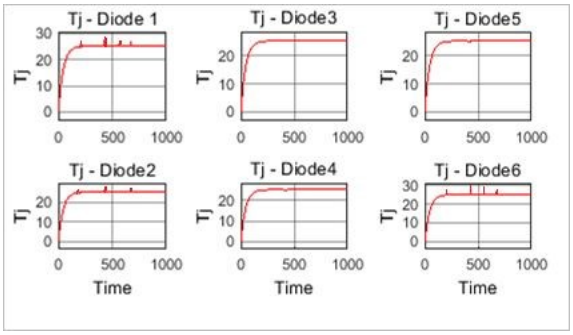

Fig.18 Thermal results for Rsce=20 with Sag

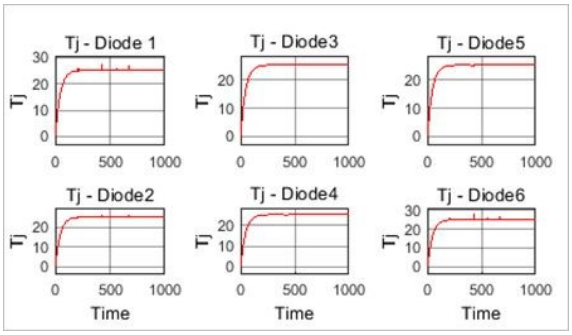

Fig.19 Thermal results for Rsce=120 with Sag

obtained from the thermal time constant values τ_i using the equation (12) as below,

$$C_{thi} = \frac{\tau_i}{R_{thi}} \quad (12)$$

C_{thi} – *thermal capacitance*
R_{thi} – *thermal resistance*
τ_i – *thermal constant*

The associated thermal and electrical parameters of semiconductor devices considered in this investigation are interconnected through means of heat sink. Heat sink is further associated to foster RC network and ambient (Table. 5). Ambient is considered to be maintained at 25°C and equivalent thermal parameters of the diode and heatsink are obtained from the datasheet.

Table 4. Thermal parameters for diode : Foster RC network

Thermal resistance R_{th} (K/W)	**Thermal constant τ_i (s)**
0.0072	0.001
0.0188	0.080
0.1290	0.200
0.07	14.29

Table 5. Thermal parameters for Heat sink: Foster RC network

Thermal resistance R_{th} (K/W)	**Thermal constant τ_i (s)**
0.0045	0.0045
0.0013	0.39
0.0057	7.1649

Additionally, thermal capacitance is calculated using equation (12) and entered in PLECS lookup table.

10. Lifetime and Damage Modelling results

Three phase 415V, 50 Hz is fed as input supply to the system and is simulated for time period of T_0 = 1000s with *SCR* = 20 and 120 respectively , with and without the event of voltage sag. VFD front-end diode junction temperature profile is determined for all cases (Fig 16, 17, 18, 19). It is observed from the graphs that there is considerable stress on diodes due to the occurrence of voltage sag and maximum short circuit ratio.

Outcome of the simulation and modelling is the irregular temperature profile which is subjected to rainflow counting algorithm for extracting optimized regular profile, determining the number of cycles and mean temperature. These values are then applied to Coffin-Manson lifetime model for obtaining the intensity of damage occurred and thereby determining lifetime of the device as shown in equation (5), where T_{jm} is calculated using equation (6). Damage is evaluated for the entire test cycle duration. Total damage of the system is estimated by the summation of individual damages in each cycle as shown in equation (10).

Simulation is carried out with the mission profile as input voltage supply without any disturbance and with the input supply with voltage sag and for short circuit ratio = 20 and 120. Damage on all diodes is obtained and the results are plotted in a graph (Fig 20, 21). The results show that the diodes experience more stress and damage on the occurrence of voltage sag which is more during higher short circuit ratio.

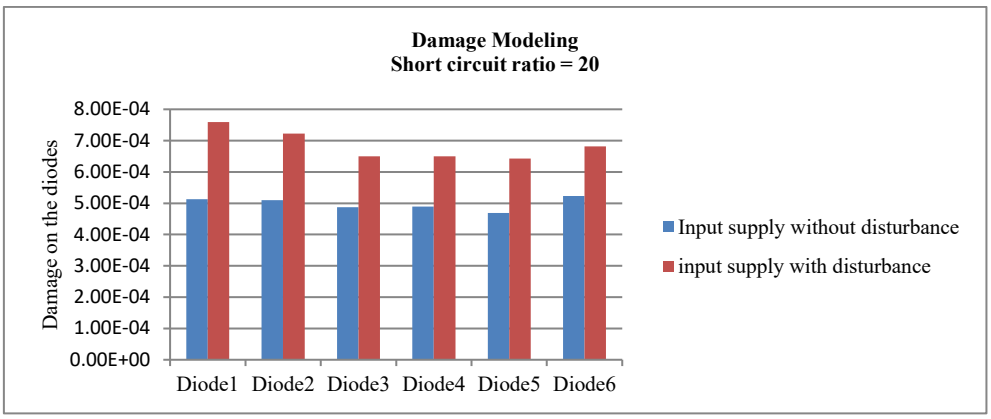

Figure. 20. Graph showing the damage occurred on the diodes of front-end rectifier at SCR=20

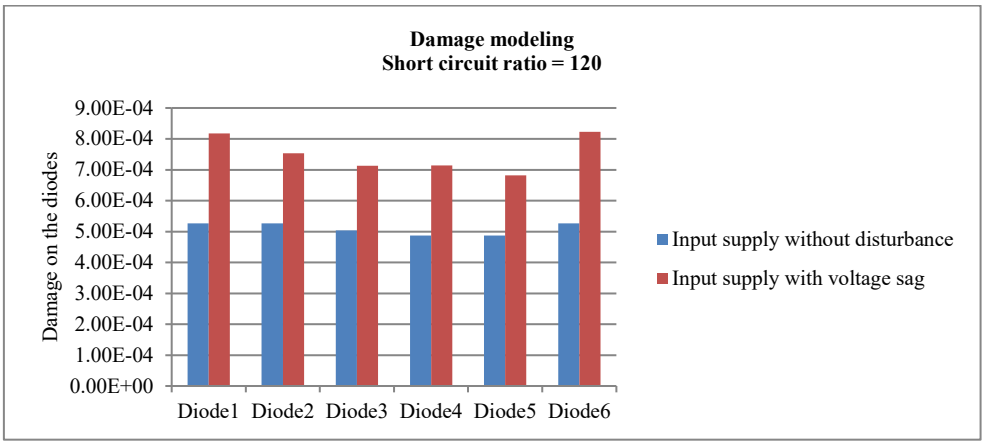

Figure. 21. Graph showing the damage occurred on the diodes of front-end rectifier at SCR=120

From the data from simulation, the lifetime of the diodes is plotted in graph for comparing the lifetime in case of input supply without any disturbance and input supply with occurrence of sag (Fig. 22,23)

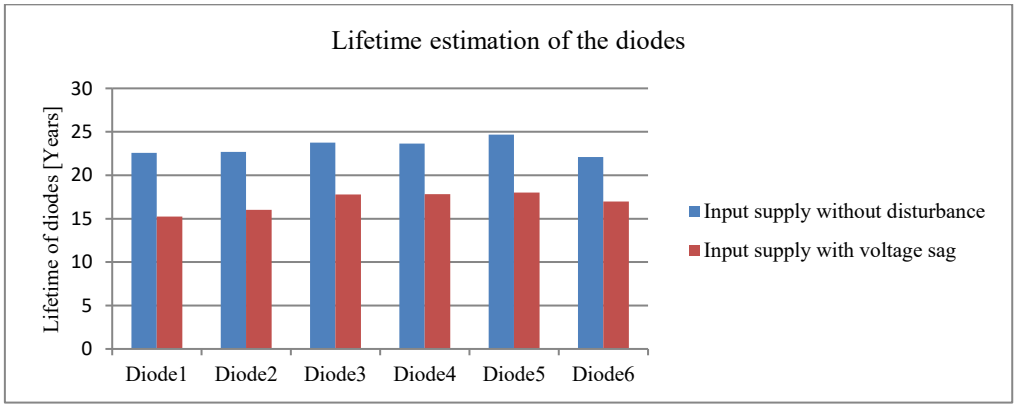

Figure. 22. Graph showing the lifetime of the diodes for short circuit ratio = 20

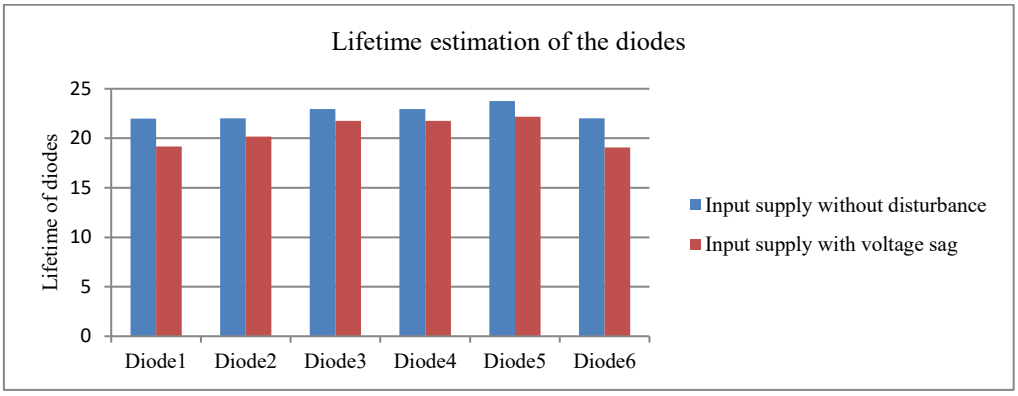

Figure. 23. Graph showing the lifetime of the diodes for short circuit ratio = 120

Thus, lifetime of the diodes in the front-end rectifier is calculated and as seen from the data and graphs, the lifetime of the device is reduced during the occurrence of voltage sag. And in case of minimum short circuit ratio, the impedance at the source is high which reduces the ripple in the supply. But in case of maximum short circuit ratio, the impedance at the source is less and the ripples in the supply are more and this too becomes a reason for the reduction in lifetime of the diodes.

11. Conclusion

VFD Front-end rectifier failure modes and causes are discussed in this investigation. Appropriate system modelling and simulation are carried out. Results are thus obtained through suitable simulation and analytical models. Device junction temperature profile evaluated is then considered for lifetime estimation as thermal stress contributes significant cause of failure. Lifetime estimation is calculated by suitable application of device junction temperature waveform through rain flow counting method, Coffin Manson model and Palmgren miner rule. Thus, with these three algorithms, the lifetime of the device is calculated. With this estimation it is possible to recommend an appropriate replacement time of the front- end rectifier. Lifetime of the device under voltage sag and at different short circuit ratio are also analysed. These effects also have additional impact on the device lifetime. Poor power quality and high short circuit ratio reduces the lifetime of device. Thus, the device can be tested with worst case scenario and the lifetime can be obtained while operating under real time harsh conditions.

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