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FIELD PROGRAMMABLE GATE ARRAY IMPLEMENTATION OF A VARIABLE LEAKY LEAST MEAN SQUARE ADAPTIVE ALGORITHM

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ABSTRACT

Adaptive noise cancellation is an extensively researched area of signal processing. Many algorithms had been studied such as least mean square algorithm (LMS), recursive least square algorithm, and normalized LMS algorithm. The statistical characteristics of noise are fast in nature and the algorithms for noise cancellation should converge fast. Since LMS algorithm has slow convergence; in this paper, a variable leaky LMS (VLLMS) algorithm is explored. VLLMS is implemented using the concept of hardware-software cosimulation using Xilinx System Generator. The design is implemented on Virtex-6 ML605 field programmable gate array board. The implemented design is tested for sinusoidal signal added with an additive white Gaussian noise. The design summary and the utilization summary are presented.

Keywords: Field programmable gate array, Noise cancellation, Adaptive filter, Variable leaky least mean square algorithm, System generator.

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INTRODUCTION

Adaptive algorithms are widely used for acoustic noise cancellation, system identification, controller design, and echo cancellation. This is one of the niche areas, in which still research continues. Implementation of these adaptive algorithms could be done either using analog components or digital processors depending on the application. Over the past few decades, digital processors such as programmable digital signal processing (DSP) [1] processors and field programmable gate array (FPGA) are explored. This research work focus in implementing adaptive algorithms in FPGA for noise cancellation.

Noise cancellation finds its applications in speech signal processing, cockpit control, and auditoriums. Typically to remove the noise from the desired signal, the noisy signal is passed through a filter that removes the noise. Filter is a system that removes the unwanted signal in the input signal to generate the desired signal as output [2]. Sometimes, the unwanted source information is not known prior [2]. Noise cancellation is a deviation of optimal filtering that involves producing an estimate of the noise by filtering the reference input and then subtracting this estimated noise from the input signal which contains both signal and noise. This requires an estimate of noise and an exact replica of signal. However, the characteristics of noise are unpredictable, filtering is done through an adaptive method. This means, the parameters of the filter are adjusted to minimize the error. In such cases, the filter has to be adaptive. That means, the weights of the adaptive filter parameters can be changed or adjusted using incoming input data and the desired signal output.

Various adaptive filters are discussed such as least mean square algorithm (LMS), recursive least square algorithm, and normalized LMS (NLMS) algorithm [3]. Adaptive filter finds its applications in noise cancellation of car environment [4], electrocardiography signal noise cancellation [5], signal processing applications [6], and to suppress intersymbol interference in digital communication system [7].

The LMS algorithm is one of the popular methods for adaptive filters. This algorithm aims to minimize the error by changing the weights of the filter in every iteration. LMS algorithm which is developed by Widrow and Hoff in 1960, utilizes the gradient of instantaneous error function, for the search of least square filter coefficients [8].

Various implementation of the adaptive filter using LMS algorithm is done in FPGA [4,6,9-11]. LMS algorithm is implemented in VLSI using various architectures [6]. The basic filter in LMS is finite impulse response (FIR) filter. Instead of direct form FIR filter, transposed form FIR filter is studied for fast convergence. Furthermore, a parallel FIR filter is used in LMS algorithm implementation for fast convergence [7]. Even though many architectures of LMS algorithm being researched to obtain a fast convergence, theoretically it has been proved that variable leaky LMS (VLLMS) algorithm has fast convergence compared to LMS [12]. Hence, VLLMS is chosen for implementation in this research using FPGA. Section 2 explains how LMS algorithm is modified as VLLMS algorithm. Section 3 talks about the design and implementation. Section 4 presents the results, and finally, Section 5 gives conclusions.

VLLMS ALGORITHM

The diagram of the generic adaptive filter is shown in Fig. 1. LMS algorithm [13] which is developed by Widrow and Hoff in 1960, utilizes the gradient of instantaneous error function, for the search of least square filter coefficients [14]. The LMS adaptation method is defined as

$$w(k+1) = w(k) + \mu\left(\frac{\partial e^2(k)}{\partial w(k)}\right) \quad (1)$$

Where the error e(k) in above equation is the difference between the output of the adaptive filter and the desired signal d(k), and it is given by equation (2),

$$e(k)=w^T(k)\, y(k) \quad (2)$$

and the gradient,

$$\frac{\partial e^2(k)}{\partial w(k)} = \frac{\partial}{\partial w(k)}\left[d(k) - w^T(k)y(k)\right]^2 \quad (3)$$

$$=-2(k)[d(k)-w^T\, y(k)]$$
$$=2y(k)e(k)$$

Where μ is the converging factor, which decides the stability of the filter and the speed of convergence. For an adaptive filter, it takes values

between 0 and 1/(N) (signal power), where N is the number of filter taps [12,15]. The LLMS algorithm was designed to alleviate the drifting problem of the LMS algorithm.

Max Kamenetsky and Bernard Widrow introduced new algorithm named VLLMS algorithm [12] to give fast convergence compared to LLMS. The weight update coefficient for the algorithm is given by the equation (4),

$$w_{k+1} = (1 - 2\mu_k\gamma_k)w_k + 2\mu_k \epsilon_k \widehat{Y_k} \quad (4)$$

Where, $\epsilon_k = Y_k - \widehat{Y_k}$ (5)

Step size μ_k is varied for better convergence of the VLLMS algorithm in the presence of noise and γ_k is the leak factor which is a time-varying parameter.

$$\mu_{k+1} = \mu_k + \gamma R_k^2 \quad (6)$$

Where, R_k is the autocorrelation of ϵ_k and ϵ_{k-1} and it is calculated as given by equation (7).

$$R_k = \rho R_{k-1} + (1-\rho)\epsilon_k \epsilon_{k-1} \quad (7)$$

Where, ρ the weighting parameter and it takes values between 0 and 1. γ_k takes value between 0 and 1 and it controls the convergence time [15] and it can be adjusted as given by the equation (8),

$$\gamma_{k+1} = \gamma_k - 2\mu_k \rho \epsilon_k Y_k w_{k-1} \quad (8)$$

After updating the leakage factor, an error signal is calculated and filter weights are adjusted accordingly.

DESIGN AND IMPLEMENTATION

FDA tool is the important tool of MATLAB which is used to design the filter of required specification. There are different responses (i.e., high pass, low pass, band pass, band stop, differentiator, integrator, etc.) and design method (i.e., IIR, finite impulse response [FIR]) for implementing the filter. By placing the filter order, frequency specifications and magnitude specifications, Filter can be customized. Tools create coefficients in the MATLAB workspace in matrix form through the specifications provided.

The VLLMS algorithm is implemented using digital filter in FPGA. Initially, the linear FIR filter is designed using FDA tool as shown in the Fig. 2 with 3 coefficients cutoff frequency of 300-450 kHz, sampling frequency of 1.5 MHz.

The architecture chosen is direct form FIR filter. The designed FIR filter coefficients are exported to Simulink workspace.

The Xilinx System Generator (XSG) is a high-level design tool which enables the prototype developer to design high-performance DSP systems using FPGAs.

The XSG tool enables us to integrate Xilinx with Simulink, it creates a. ise file which is used in Xilinx using the model file of Simulink. Xilinx block sets work only in the gateway blocks, i.e., gateway-in and gateway-out. Any sample-based input is given to the gateway-in block, the output can be seen on the scope by passing through the gateway out block.

First LMS algorithm based adaptive filter is designed in Simulink as shown in Fig. 3.

Then, the selected adaptive VLLMS is chosen for implementation for this research work. The VLLMS adaptive filter is implemented using system generator. The Simulink model for the same is presented in Fig. 4.

The Simulink model uses Simulink block:

- Gateway in: This block converts the Simulink inputs of integer, double, and fixed point to Xilinx fixed point type of specified bit size. It functions as an input port to the Xilinx block
- Gateway out: This block converts fixed point inputs from the Xilinx blocks to Simulink block outputs of integer, double, or fixed point. It functions as an output port to the Xilinx block
- Other Simulink blocks are basic adder, multipliers, and delay that are used to make the filter.

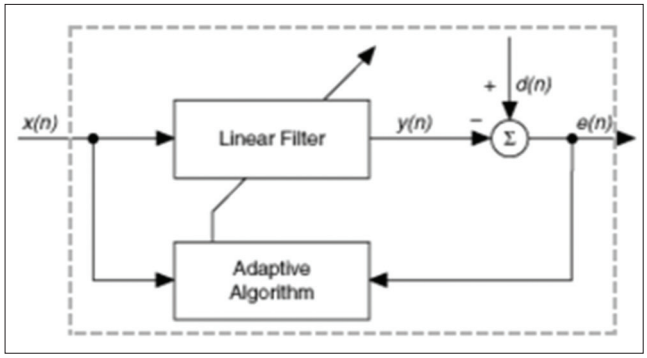

Fig. 1: Generic adaptive filter diagram

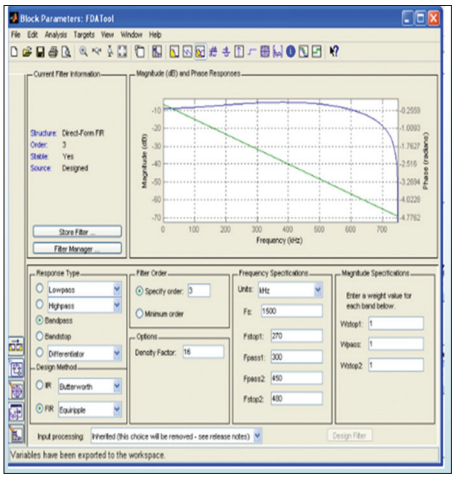

Fig. 2: FDA tool - finite impulse response filter design

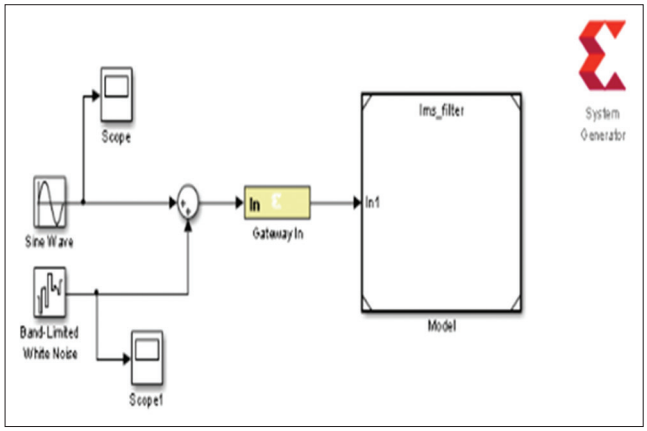

Fig. 3: Least mean square filter - Simulink

The designed VLLMS is 3-Tap FIR filter with an adaptive algorithm of VLLMS. The initial filter coefficients are designed using FDA tool for a band pass filter of 300-450 kHz with a sampling frequency of 1500 kHz. The leak factor considered for this paper is 0.8. The convergence μ factor considered for this paper is 0.2. The design contains 9 multipliers, 8 adders, and 10 delay blocks.

RESULTS

Initially, the LMS algorithm is implemented using system generator blocks. The noisy input signal as shown in Fig. 5 is applied to designed LMS block.

The filtered output is shown in Fig. 6, the register-transfer level (RTL) schematic of the respective LMS-FIR filter design is shown in Fig. 7.

The VLLMS algorithm is implemented using Virtex-6 ML605 FPGA board. The adaptive filter is evaluated for the noisy input signal as shown in Fig. 8.

The steady state mean square error e(n) is shown in Fig. 9 for the noisy input as shown in Fig. 8.

The RTL schematic of VLLMS adaptive filter is shown in Fig. 10.

The device utilization summary of LMS adaptive filter is given in Table 1. Here, it can be seen that the proposed algorithm is area efficient since the number of slice registers used is 1 out of 54576. The combinational path delay found here is 1.222 ns. The algorithm is found to be area efficient as shown in Table 1.

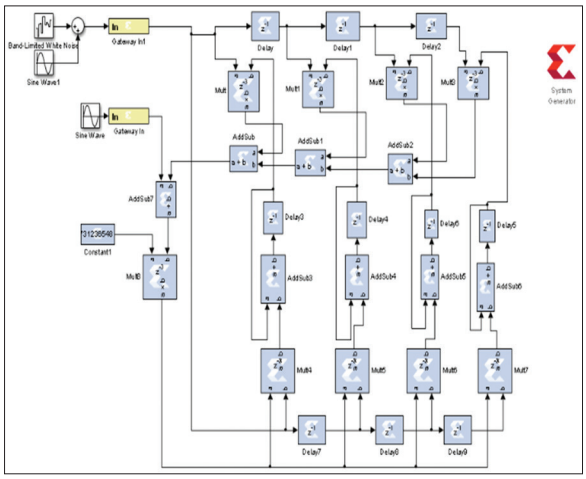

Fig. 4: Simulink model of variable leaky least mean square adaptive filter

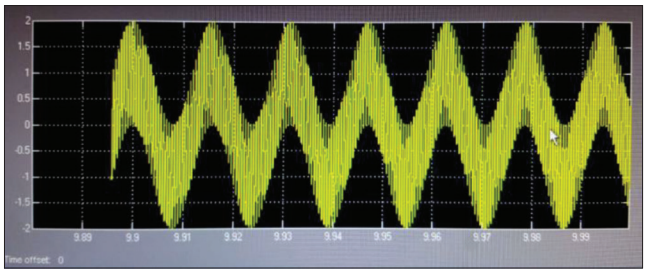

Fig. 5: Noisy input signal

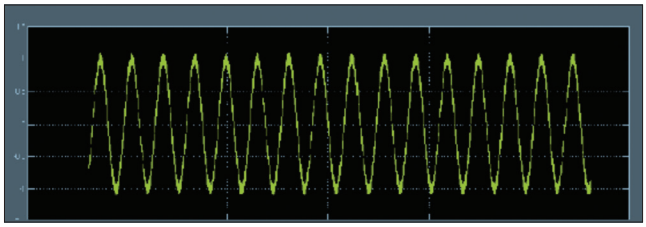

Fig. 6: Filtered output

CONCLUSION

Adaptive noise cancellation is one of the research areas of adaptive filter applications. Adaptive noise cancellations find its application

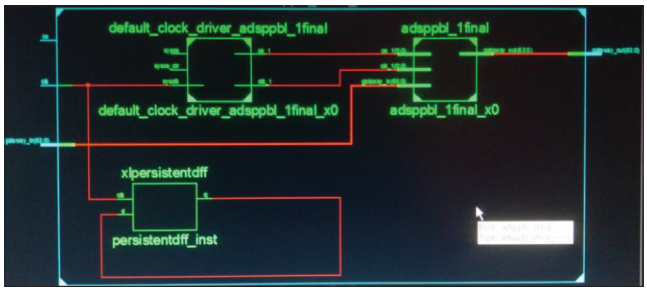

Fig. 7: Register-transfer level schematic of least mean square adaptive filter

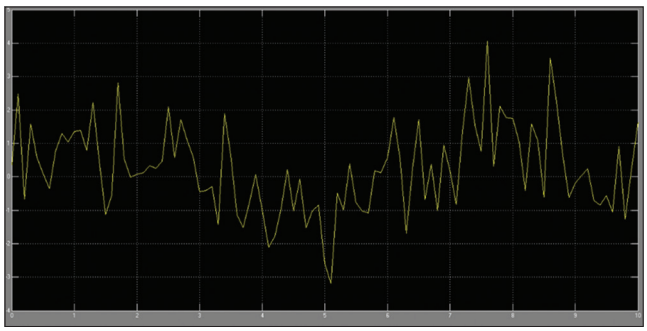

Fig. 8: Noisy input for variable leaky least mean square algorithm

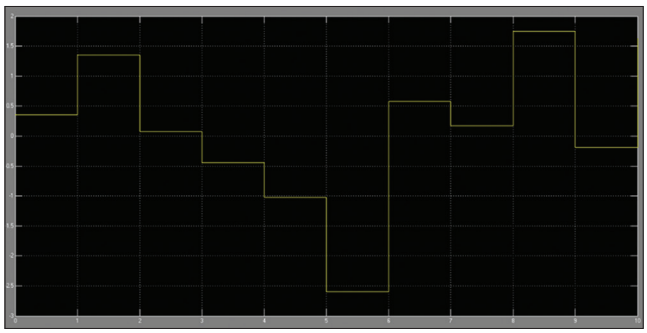

Fig. 9: Mean square error for first iteration

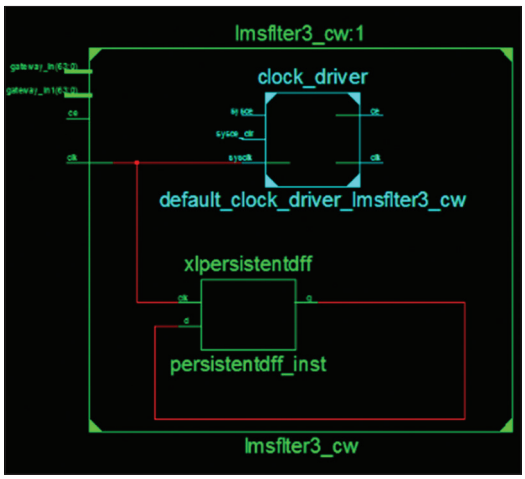

Fig. 10: Register-transfer level schematic of variable leaky least mean square adaptive filter

Table 1: Device utilization summary of variable-LLMS adaptive filter

Logic utilization	Used	Available	Utilization
Number of slice registers	1	54576	0%
Number of fully used LUT-FF pairs	0	1	0%
Number of bonded IOBs	1	190	0%
Number of BUFG/BUFGCTRLs	1	16	6%

LLMS: Leaky least mean square

cockpit control and speech signal. In this research work, LMS algorithm is implemented using system generator. Further, VLLMS algorithm is chosen for implementation because of its fast convergence compared to LMS algorithm. This design is tested for sinusoidal signal added with additive noise (additive white Gaussian noise) on Virtex6 ML605 FPGA board. It is observed that the number of slice registers used is 1 among 54,576 and the area utilized for it is 0% compared to other algorithms. The number of fully used LUTs is 0%. This VLLMS algorithm method is area efficient and the system generator is used for interfacing Simulink blocks and Xilinx blocks. In the future, implementation of VLLMS algorithm explored various digital filter architectures such as parallel FIR filter to further minimize the convergence time.

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