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Fuzzy Controlled Switched Capacitor Boost Inverter

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Abstract

The increase in the usage of renewable energy and power electronic applications prompted the development of multilevel inverters. A new multilevel switched capacitor boost inverter is designed which gives the required number of output voltage levels with a dc source. The number of power electronic components used here are less comparatively. A single inductor multi-output DC-DC converter is coupled with an inverter through dc link capacitor to carry active power to the grid. Hence this boost inverter shows good reliability, less cost and low losses. The dc linked capacitor helps in voltage balancing. The total harmonic distortion is reduced. the cascaded H-bridge converter has gained significant interest due to a modular structure with easy construction and maintenance, isolated dc buses with no voltage unbalance problem and easy extension. The inverter switches are triggered using Phase Opposition Disposition (POD) Pulse Width Modulation technique. . Simulation for five level and seven level boost inverter topologies is done using MATLAB software and hardware implementation of five level boost inverter is executed.

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*Keywords:B*oost converter, inverter, voltage balancing, POD multicarrier PWM method.

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1. INTRODUCTION

The amount of fossil fuels which results in carbon emissions to the atmosphere is finite. Hence the necessity for renewable energy resources has been increasing a lot nowadays. The most frequently used renewable sources are solar and wind. These are reliable, greener and more eco-friendly. They have an environmental boon like low emission comparatively. Solar is the most renewable sources of energy. In the recent decades the solar power through photovoltaic systems is affordable and free from dirt or pollution. Grid-connected solar photovoltaic (PV) power is emerging as the quickest power generating technologies [1]. The keystone to exploit the solar based PV sources is the inverter which plays the conversion role from DC to AC. A multilevel inverter (MLI) is appropriate for direct drive solar power system because it enriches the quality of output voltage and also less voltage is blocked in switching devices which tends to minimize the power losses [2].]. A low total harmonic distortion (THD) is generated from the output signal when MLI is used, because of this the size of output filter gets lowered, its cutoff frequency is influenced by the modulation technique and the switching frequency [3]. As PV cells produce less DC electricity a boost converter is placed at the front-end of MLI in order to obtain higher voltages to sink up with the grid utility [4].A newly developed multi output boost converter (MOB) containing series DC link capacitors is connected to the MLI[4]. A newly developed multi output boost converter (MOB) containing series DC link capacitors is connected to the MLI. The inverter stage has certain number of topologies. In large power functions, there are certain interferences between power converters and load such as dv/dt stress, common mode voltages and cable interactions. These can be limited using PWM converters. In either way the load is impended with design restrictions by the PWM converters [5]. An MLI is predictably designed in such a way so as to produce a sine waveform which can be attained from the capacitor voltages. Supposedly, there are three capacitor voltage synthesis-based MLI. (1) Diode-clamped (2) flying capacitors (3) Cascaded inverters.

Generally, in diode clamped the normal component used here is a “diode” where its number escalates with raise in levels. Inducing filters can be shunned as the harmonic content would be low at higher levels. Since the switching frequency of all the devices is the fundamental frequency, the efficiency is expected to be very high. Controlling reactive power is achievable. But controlling the real power in every converter is actually difficult. A different diode clamped MLI is discussed in [6] which uses less number of diodes comparatively. In flying capacitor, the norm of using capacitors is leading. And with the rise in the no. of capacitors increases the levels of MLI. This topology provides switching redundancy in order to balance the voltage levels. Here it controls both real and reactive power. Hence fetched its application in transmitting the voltage. It becomes problematical in controlling inverter. As it operates at high switching frequency, while real power transmission is happening high switching losses occur.

Similarly, a modified flying capacitor has been discussed in [7]. In cascaded MLI, the number of switches and sources increase with the no. of cascade stages. This involves one phased inverter with separate dc sources. To achieve the required sum of voltage levels it has a need of very fewer components. No clamping diodes or voltage balancing diodes are compulsory. As the construction is same at every level, the casing becomes easygoing. This is a modulated circuit design. Soft switching can be adopted to eradicate the snubber circuits which are bulky and result in heavy losses. For real power conversions isolated dc sources are necessary.

The plusses of the multi-level inverters are:

1. As the number of levels adds up there exists a rise in voltage and power values in output.
2. Also there is a dropping off in harmonics as the no. of levels increases.
3. Even though there is an increment in voltage and power, it does not affect the ratings of switches.
4. The input current is drawn with less distortion.
5. Operating at low switching frequencies is possible and thus achieves higher efficiencies.
6. It acts as an ideal interface between RES and grid utilities.

This topology explains diode clamped conventional multilevel inverter which has MOB as dc link supplier to boost and control the capacitors voltages to the desired levels and a three phase H bridge inverter to improve the voltage that is yielded as output [8].The capacitor voltages essentially be balanced by adjusting the duty cycles of the switches. This paper describes a novel dc-dc converter for a three level NPC inverter. The basic operation of converter is explained which helps in avoiding the problem of unbalanced capacitor voltages and provides appropriate dc voltage to NPC inverter. Anyway the lower PV output is boosted to higher voltage values in order to synchronize with grid power applications [9]. By fixing the desired output voltages across the capacitors from the input PV voltage the duty cycle values of the MOB switches are calculated. This explains various configurations of

single inductor dual output dc-dc converter. Voltage ratios and output voltage ripples are derived in this paper. Also states that this can be applied for single inductor multi output thriving converters [10]. The span of the values of inductor and capacitor in MOB are designed [11]. For high power conversion an MLI is apt. The harmonic distortion decreases if there is a rise in the number of levels. Generally a conventional MLI consists of three kinds, diode clamped, flying capacitor and a cascaded one. Every time in diode clamped the count of diodes raises followed by the increase in voltage levels [12].Whereas in flying capacitor MLI, the capacitor count has its dominance [13]. Here, a cascaded MLI with less number of switches and sources is used. It is a smallish inverter which costs less and has high efficiency [14]. Medium voltage motor drives has power converter that has a rectifier, Dc link and an inverter. Here a neutral point clamped inverter is used. In that the dc voltage is split by two capacitors. For high power motor drives cascaded H bridge inverters are used. The switches which control the multilevel inverter are triggered by space vector modulation (SVM) method. This method is complicated because of many redundant switching states and stationary vectors [15]. Different topologies of multilevel inverters are explained in a detailed manner. Every type has its advantages and disadvantages. The switch used here in these topologies are Gate Turnover Thyristor (GTO). Also explains Fundamental Frequency Switching (FFS) and Pulse Width Modulation (PWM) methods. FFS states that the thyristor is switched on and off once during a power frequency (60Hz or 50Hz) cycle [16].A novel hybrid multilevel inverter is designed in this paper. This involves a switched capacitor converter and a cascaded H-Bridge converter with an auxiliary switch. This auxiliary switch helps in increasing the number of voltage levels. Simulations for a five level inverter is performed. A single source is required because of its boosting feature [17].There are many modulation techniques for ML power conversion applications. Among those Carrier Based PWM strategies are being longed in multilevel topologies by using multiple carriers. These are classified into Carrier Disposition methods (CD), Phase Shifted methods (PS) and a combination of both called Hybrid (H) methods. The different CD methods are Phase Opposition Disposition (POD), Phase Disposition (PD) and Alternative Phase Opposition Disposition method. In this paper POD PWM method is implemented. If a P level waveform is required, there needs P-1 no. of carriers which shift by 180^0 underneath the reference zero diverting from those carriers above zero level.

2. PROPOSED TOPOLOGY

2.1 Modes of Operation

A five level boost inverter is considered and has been designed. The Fig.1 below shows the basic five level boost inverter type. This has two output bearing boost converter and one inverter. So as to observe equal voltage level raise, the converter design should assure that the voltage across each capacitor should be equal and balanced. In the figures we can the flow of current is highlighted. That explains the modes of operation.

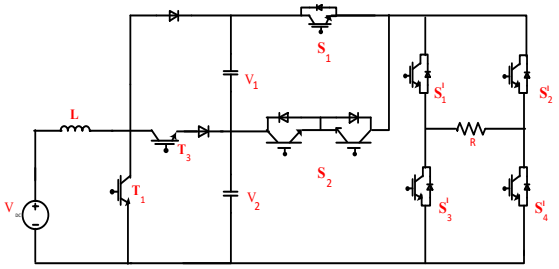

Fig 1 Basic Five level Boost Inverter

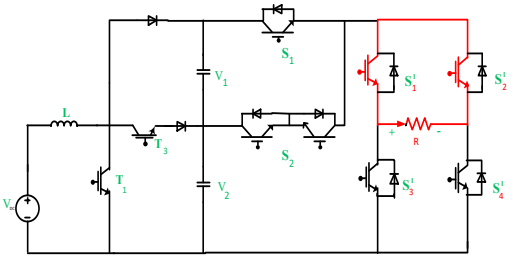

Fig.2

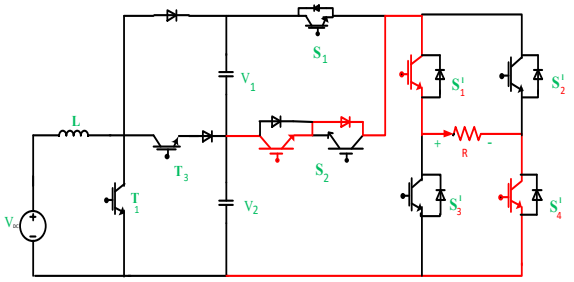

Fig.3

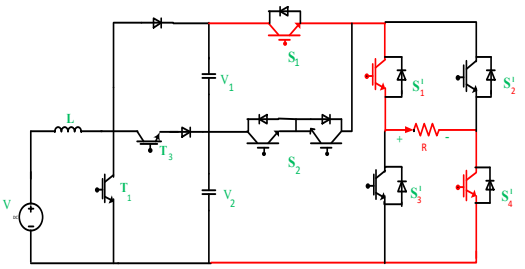

Fig.4

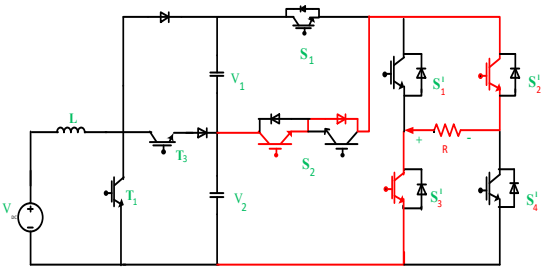

Fig.5

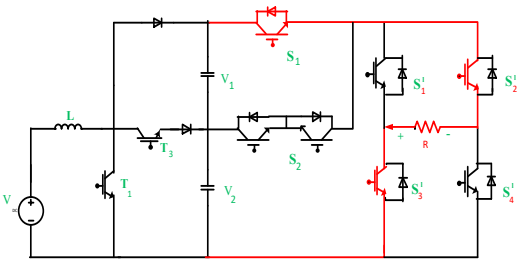

Fig.6

The Fig.2 to Fig.6 explains the different modes of operation. In the figures we can the flow of current is highlighted.

2.2 Inverter and POD Technique

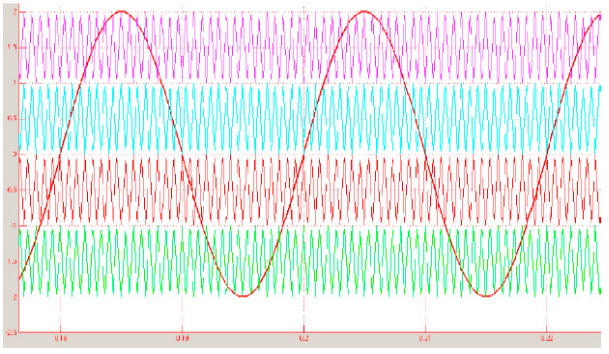

Fig.7 POD comparison.

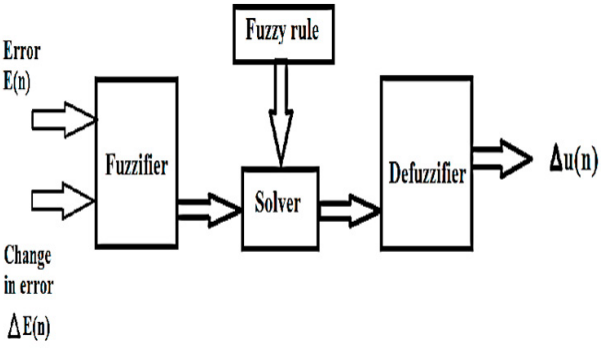

Fig.8 Block Diagram of Fuzzy Controller

The pulses generated from the POD technique will be utilized and mathematically applied some logic between so as to attain the seven pulses as desired by the inverter.

2.3 Boost Converter Operation

Table 1. Switching Sequence of the seven switches.

Voltages and Switches	S1	S2	S1	S2	S3'	S4'
2V	ON	-	ON	-	-	ON
V	-	ON	ON	-	-	ON
0	-	-	-	-	-	-
-V	-	ON	-	ON	ON	-
-2V	ON	-	-	ON	ON	-

Table.2 Operation of Boost Converter

Duty Cycle/ Switches	T1	D (Diode)	T3
D1	ON	OFF	OFF
D2	OFF	ON	OFF
D3	OFF	OFF	ON

In the steady state operation, the net change or the total change in the inductor current must be zero. The equations are as displayed below,

$$(\Delta I_1)_{closed} + (\Delta I_2)_{open1} + (\Delta I_3)_{open2} = 0 \quad (1)$$

$$\frac{VsD_1T}{L} + \frac{Vs - V_1 - V_2}{L} + \frac{(Vs - V_2)D_sT}{L} = 0 \quad (2)$$

By solving the equation we obtain,

$$V_S(D_1 + D_2 + D_3) = V_1 D_2 + V_2 (D_2 + D_3) \quad (3)$$

One should be noted that, the summation of the duty cycles of all the switches must be equal to unity.

$$D_1 + D_2 + D_3 = 1 \quad (4)$$

Inserting (5) in (4) gives as below,

$$Vs = V_1 D_2 + V_2 \ (D_2 + D_3 \ )$$

$$D_2 + D_3 = 1 - D_1$$

Therefore, it can be again written as below,

$$Vs = V_1 D_2 + V_2 (1 - D_1) \quad (5)$$

Eqn (5) is the final relation among the input source, and output voltages and the duty ratios of all the switches. Assuming the input voltages and the output voltages, the duty cycles values can be derived and simulated. Hence the peak to peak inductor current is given by,

.

$$\Delta I = \frac{Vin D_1 T}{L}$$

$$\frac{\Delta V_1}{V_1} \equiv \frac{D_1 T}{R_1 C_1} \quad (6)$$

$$\frac{\Delta V_2}{V_2} = \frac{(D_1 + D_2)T}{R_2 C_2} \quad (7)$$

In this way the boost converter components are designed in order to obtain the desired output voltage levels. Likewise, the three output boost converter is also designed based on the requirement of the output levels.

2.4 Fuzzy Controller Implementation

The reason for using this controller in this topology is to control the observed output value of the voltage. This takes the action to control and henceforth maintains the voltage constant.

The allowance of partial value matching exists. The extent to which an assertion gets satisfied, the analyst can guesstimate till that coverage. Fig.8 shows the block diagram of fuzzy logic controller.

The fuzzy controller window open when its name is typed on the command window. A box like in Fig.9 gets opened.In the window one can observe three major blocks, one input, a output and membership box. In the membership block one has to give certain rules according to the prerequisite. By clicking on the box the rules can be directly inscribed as exhibited in the fig.10.

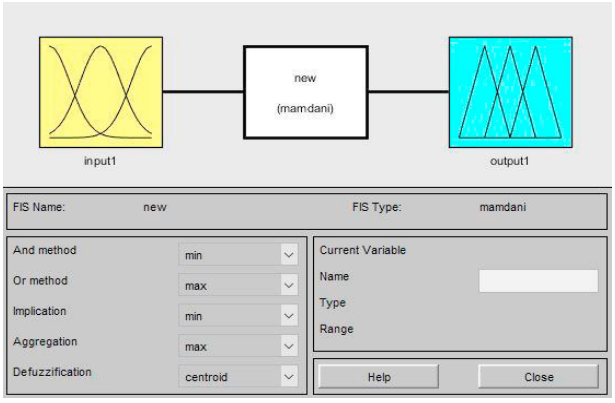

Fig.9 Fuzzy Controller Window.

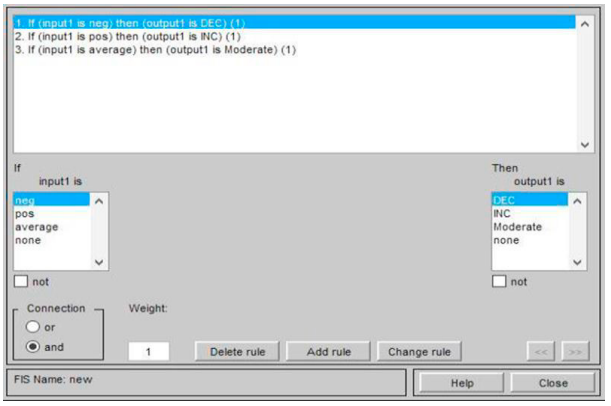

Fig.10 Set up Rules Window.

Agreeing to the constraints of the topology output, three rules are constructed as follows.

1) If (input is neg) then (output is DEC).
2) If (input is pos) then (output is INC)
3) If (input is average) then (output is moderate)

Rule one tells that if the input the negative, i.e. the difference between the reference value and the RMS value is negative. Then the output value will be decreased. Rule two says, if the difference between the reference and RMS is positive, the fuzzy controller increases the voltage to the value of the reference value. Similarly the third rule says that if the input is moderate then the output is moderate.

3. RESULTS

3.1 Simulation Results

The Fig.13 depicted for five level is attained through the MATLAB simulation. The output voltage levels are observed to be as per the requirement. It is designed that the voltage levels should be 60+60=120V.

3.2 Hardware Results

The Fig.21 shown are pulses generated from the Arduino Board. Fig 21(a) shows the pulses to activate the switches in the inverter piece. Whereas the other two pulses shown in Fig.21 (b) and Fig.21(c) are the pulses to the switches in the boost. From the Arduino board the connections are made with driver boards.

Fig.11 Input values set up box.

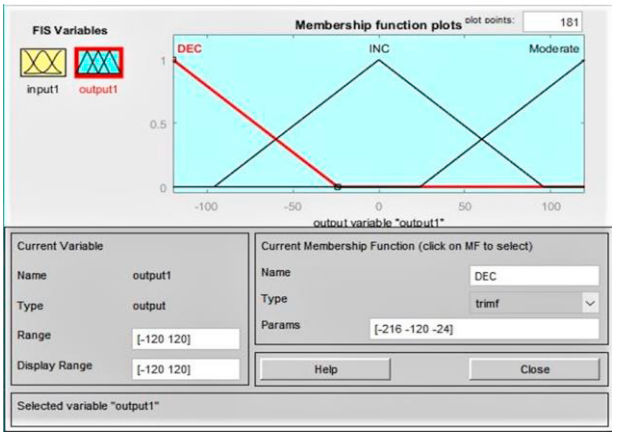

Fig.12 Output Values changes (DEC)

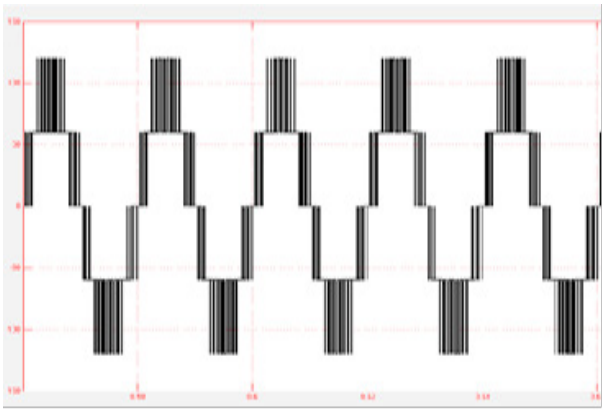

Fig.13 Five level output

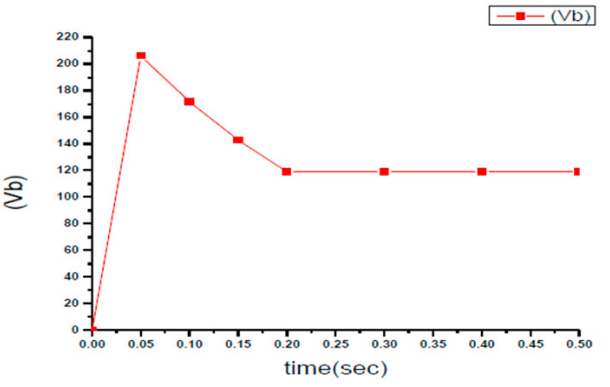

Fig.14 Output Voltage of 2-Output Boost Converter

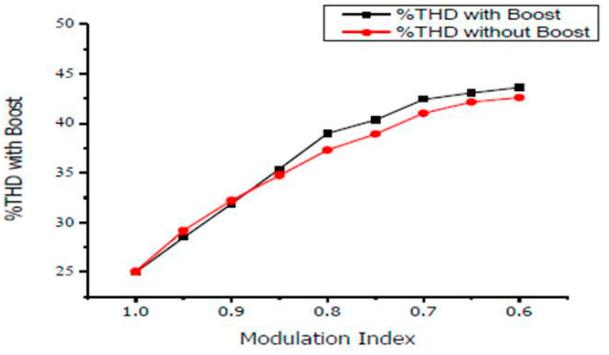

Fig.15 THD Vs M_a

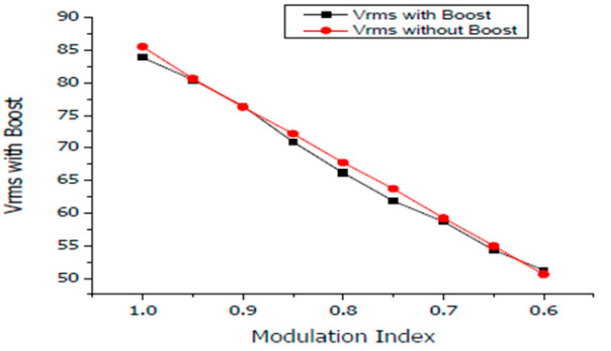

Fig.16 V_{rms} Vs M_a

3.3 Snapshots

The Fig.22 and Fig.23 show the hard ware implementation of the circuit. In the snapshot, there is a DSO on the extreme right. On the wooden plank inverter configuration is soldered on one dotted board which is placed in the front of the board. And the soldered boost part is kept at the back. The driver boards TLP250 are used to give pulses to the switches. Total five driver boards are used. Each board can give two pulses to two number of switches. A 1:9 output pin transformer is used and its configuration is 0-15V and 1 Ampere.

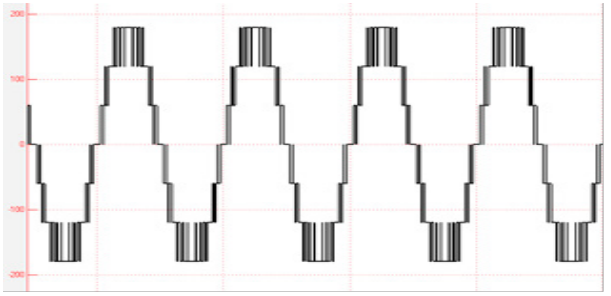

Fig.17 Seven Level Output

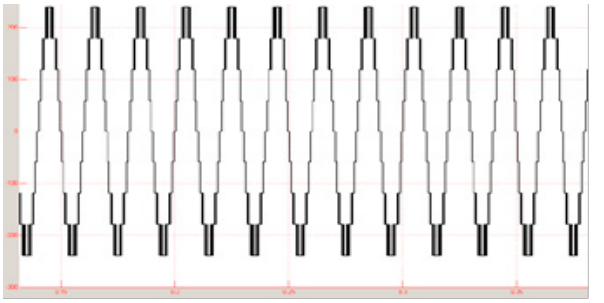

Fig.18 Nine Level Output

Fig.19 Oscillating RMS value of the Output Voltage in Open Loop

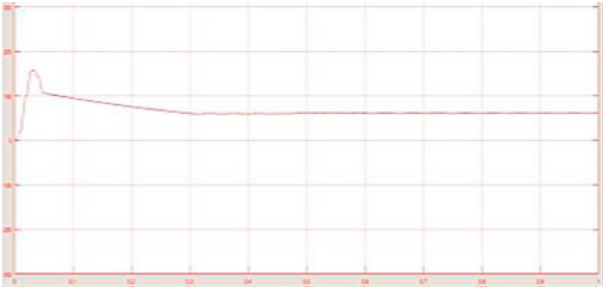

Fig.20 The Constant RMS Output Voltage value in Closed Loop Implementation

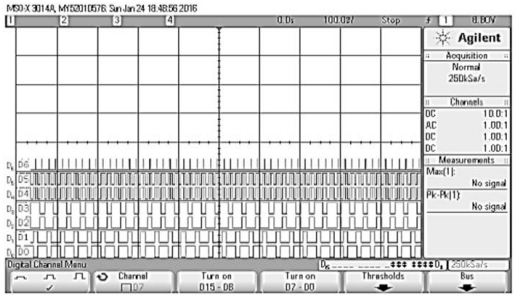

Fig 21 (a)

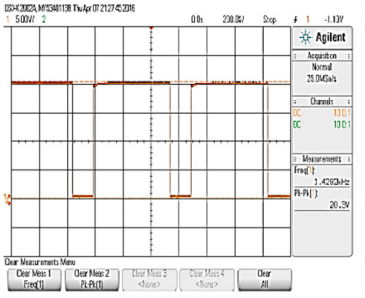

Fig 21(b)

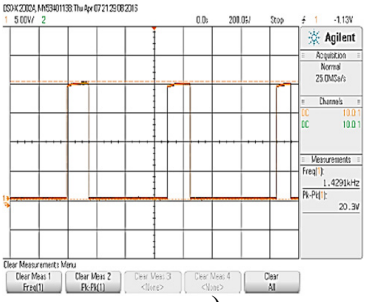

Fig21(c)

Figs 21. Pulses from Arduino Board.

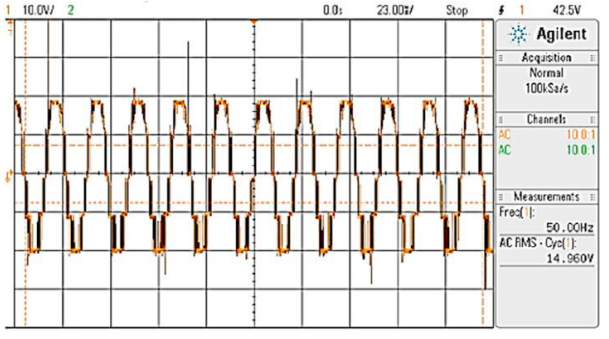

Fig.22 Hardware Output Voltage Waveform

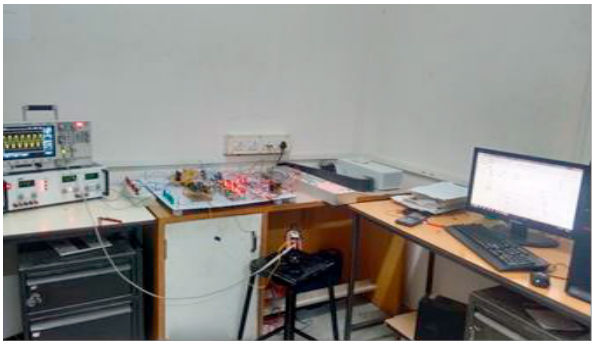

Fig.23 Snapshot

4. CONCLUSION

This topology ascertains the genuine time application in this world. Multi carrier PWM technique to trigger the switches on the inverter chunk and the switches on the boost wing are triggered using pulse generators in MATLAB Simulink ensuing the triggering pattern with certain delays satiating the design parameters. This circuit format uses less no. of switches comparatively. Leads to less distortion and losses as it is a multi-level inverter. Thereby reducing the cost because of less components and shrinks space because of no huge bulk size. Hardware implementation has been performed here and can be improved to the peaks further in the upcoming future. For the switches to activate different hardware circuits are readily available. An Arduino Mega has been used to engender the pulses.

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