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High Step-Up DC-DC Converter with Reduced Switch Stress and Low Input Current Ripple

Kalaimaran.S[a], Sri Revathi.B[b], Prabhakar.M[c]*

[a]M.Tech(PED) Student, VIT University, Chennai, India.
[b]Assistant Professor(Sr.)/SELECT, VIT University, Chennai, India.
[c]Associate Professor/SELECT, VIT University, Chennai, India.

Abstract

This paper proposes a three phase interleaved high gain DC-DC converter for photovoltaic (PV) applications. Interleaving technique reduces the input current ripple and current stress on the power switch while simultaneously handling high power. The voltage gain is extended by using a voltage lift capacitor, coupled inductor and voltage multiplier cell. Since voltage gain extension is realized at the secondary side of the coupled inductors, the voltage stress on the switches is only a fraction of the output voltage. Experimental results obtained from a 24V/260V, 500W prototype converter proves the converter suitability for high step up voltage conversion.

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Keywords: coupled inductor; DC-DC converter; interleaved technique; voltage multiplier cell

1. Introduction

Nowadays, renewable energy sources (RES) are gaining popularity due to stringent environmental pollution norms and fast depleting conventional energy sources. The electrical energy generated from RES like photovoltaic (PV) modules can be used to feed the main AC grid after using an intermediate power electronic converter. Since the output from PV sources is generally low (of the order of 12-60V) and DC in nature, an intermediate high gain DC-

* Corresponding author. Tel.: +91-44-39931154.
E-mail address: prabhakar.m@vit.ac.in

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DC converter is used between the PV module and inverter to minimize size of the transformer connected at the AC grid side. The overall performance of such a system depends mainly on the efficiency of power conversion stages [1], [2]. Hence, selecting an appropriate high gain DC-DC converter is critical.

In conventional boost DC-DC converter, diode reverse recovery problem and switch stress at extreme duty ratios restrict the practical voltage gain. Though a cascaded boost converter offers higher conversion ratio, presence of more components limits its operating efficiency [3], [4]. Magnetically coupled converters like flyback, push pull and full bridge converter can provide the required voltage gain by properly choosing turns ratio of transformer. Unfortunately, the leakage inductance of the magnetic element causes additional voltage stress and incremental losses on the switch [5], [6]. Without using a transformer, several methods to enhance the voltage gain include using voltage multiplier Cell (VMC), coupled inductor (CI) and switched capacitor (SC) networks [7]-[9]. VMC based step up converters provide the required voltage gain but their power handling capability is limited by their component count [10], [11].

In this paper, three phase interleaved boost converter (IBC) based on coupled inductors and VMC is proposed. The three switches present in the IBC are operated with a uniform phase shift of 120° between them. This helps to reduce the input current ripple. Two simple inductors are replaced by coupled inductors to increase the voltage gain and handle higher power. The main features of this converter are (i) high voltage gain, (ii) low voltage and current stress on the switches, (iii) low input current ripple and (iv) high power handling capability.

Nomenclature

D	Duty ratio
f	Switching frequency
k	Co-efficient of coupling
n	Turns ratio of the coupled inductor

2. Proposed Converter and its Operating Principle

2.1. Circuit Description

Fig. 1 shows the power circuit diagram of the developed converter. The three IBC legs with a simple inductor L_1, primary windings of the two coupled inductors L_{2P}, L_{3P} along with lift capacitor C_L, lift diode D_L and D_1 forms Stage 1. Gain extension network consisting of secondary windings L_{2S}, L_{3S} and the VMC network formed by diode-capacitor combination (C_1, C_2, D_3 and D_4) constitutes Stage 2 of the proposed converter. Diode D_o and capacitor C_o act as the output diode and capacitor respectively.

2.2. Operating Principle of the proposed Converter

Operating principle of the proposed converter is explained in six modes under the assumption that (i) all passive elements and semiconductor devices are ideal and (ii) inductors are already charged.

Mode 1 ($t_0 - t_1$):

Switches S_1 and S_3 are turned ON. Through the diodes D_L and D_1, inductor L_1 and primary winding L_{3P} of the coupled inductor start charging equal to the input voltage V_{IN}. Energy stored in the primary winding L_{2P} starts discharging to the load as switch S_2 is in OFF state. Charging and discharging of the secondary windings L_{2S} and L_{3S} are at the same rate of discharging and charging of L_{2P} and L_{3P}. Multiplier capacitor C_1 charges when the secondary windings discharge their stored energy to the load. Capacitor C_2 starts charging through diode D_3. On complete charging, capacitor C_2 reverse biases diode D_3 and forward biases diode D_4 such that its stored energy is transferred to the load. Output capacitor C_o is charged to the magnitude of load voltage.

Mode 2 (t_1-t_2):

Primary winding L_{3P} of the coupled inductor is completely charged at time t_1. To discharge the energy stored in L_{3P} to the load, switch S_3 is turned OFF. Other two switches S_1 and S_2 remain in their ON and OFF state respectively. Whenever switch S_3 is in OFF state, diode D_1 conducts and helps in energy transfer. Diode D_L is in OFF state as switch S_1 is conducting. Discharged energy from L_{2P} and L_{3P} charges their corresponding secondary windings L_{2S} and L_{3S} while supplying the load. At the end of this mode, energy stored in the multiplier capacitor C_2 is completely discharged to the load. Hence, diode D_4 goes out of conduction and diode D_3 comes into conduction aiding the capacitor C_2 in charging. At t_2, capacitor C_L is charged to $\frac{1}{1-D} V_{IN}$.

Mode 3 (t_2-t_3):

At t_2, all the energy stored in L_{2P} is discharged to its secondary winding L_{2S}. Switch S_2 is turned ON enabling L_{2P} to charge towards V_{IN}. Switches S_1 and S_3 are maintained in their ON and OFF states as that of previous mode. Diodes D_1, D_2, D_3 and D_o are conducting while D_L and D_4 are reverse biased. Inductors L_1 and L_{3P} are still in their respective charging and discharging states. Secondary winding of CI L_{2S} supplies the load. Secondary winding L_{3S} and multiplier capacitor C_2 are in charging state.

Mode 4 (t_3-t_4):

Switch S_1 is turned OFF to transfer the energy stored in L_1 to the load. Primary and secondary windings of the coupled inductors continue in the states as that of Mode 3. Switches S_2 and S_3 are retained in their ON and OFF states as such. At t_4, multiplier capacitor C_2 is completely charged through diode D_3 and starts discharging to load through D_4. At the end of this mode, capacitor C_L is charged to $\frac{2}{1-D} V_{IN}$.

Mode 5 (t_4-t_5):

As stored energy in L_{3P} is discharged to the load, current through L_{3P} reaches its minimum limit. Hence, switch S_3 is turned ON to charge L_{3P} towards the input voltage V_{IN}. Switches S_1 and S_2 remain in OFF and ON state respectively. Diode D_1 is reverse biased while D_L is forward biased. States of L_1 and L_{2P} are similar to Mode 4. Capacitor C_2 charges to load voltage V_O through diode D_3. Diode D_4 enters into conduction once C_2 is completely charged at time $t=t_5$.

Mode 6 (t_5-t_6):

Switch S_2 is turned ON such that L_{2P} transfers its stored energy to the load through L_{2S}. L_1 continues to discharge through D_L as switch S_1 is in OFF state. L_{3P} continues to charge through switch S_3. Hence, diode D_1 remains in OFF state. Fully charged capacitor C_2 supplies the load through diode D_4. At t_6, capacitor C_L is completely charged to $\frac{3}{1-D} V_{IN}$. This marks the end of Mode 6 and completion of one cycle. Thus, at the end of every switching cycle, the voltage across C_L is lifted by the number of interleaved phases compared to a classical interleaved boost converter. The equivalent circuit of the converter for all the operating modes is shown in Fig. 2(a)-(f). Fig. 3 shows the characteristic waveforms of the presented converter.

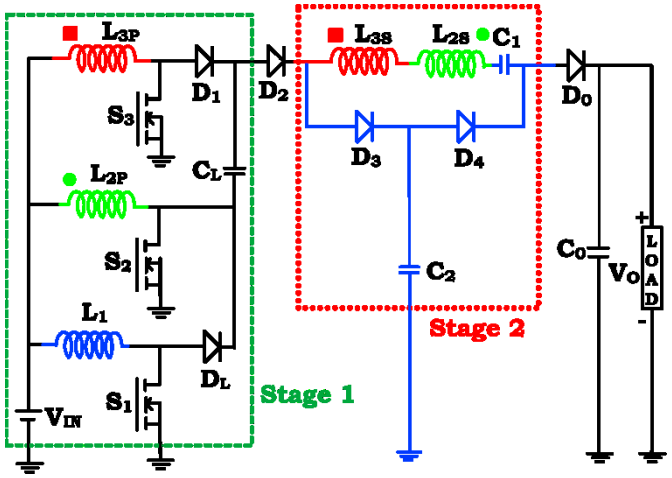

Fig. 1. Power circuit diagram of the proposed converter.

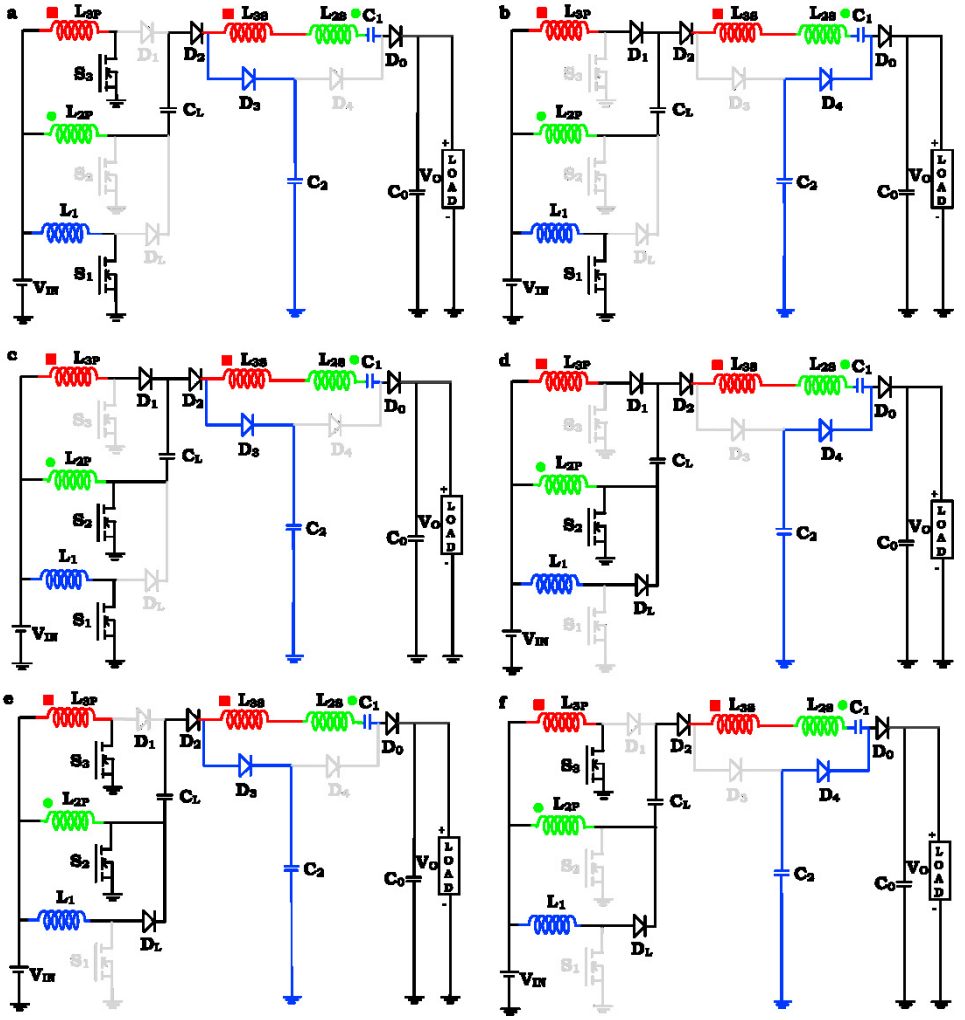

Fig. 2. (a)-(f) Equivalent circuit during Mode 1 to Mode 6.

3. Analysis and Design Details

3.1. Voltage Gain

The three phase IBC operates similar to an individual boost converter. Hence, at the end of Mode 2, the voltage across C_L is expressed as

$$V_{C_L}^{(1)} = \frac{1}{1-D} V_{IN} \tag{1}$$

At the end of Mode 4, the voltage across the lift capacitor C_L is given by

$$V_{C_L}^{(2)} = V_{C_L}^{(1)} + \frac{1}{1-D} V_{IN} = \frac{2}{1-D} V_{IN} \tag{2}$$

During Mode 6 the switch S1 turned OFF. Therefore, voltage across the lift capacitor and V_{IBC} will be

$$V_{IBC} = V_{C_L}^{(3)} = V_{C_L}^{(2)} + \frac{1}{1-D} V_{IN} = \frac{3}{1-D} V_{IN} \tag{3}$$

The secondary side of CIs are connected to VMC network. As two CIs have been used in the power circuit, the voltage gain contributed by the VMC network is given by

$$V_{VMC} = \frac{2nk}{1-D} \tag{4}$$

From (3) and (4), the total output voltage is derived as

$$V_o = V_{IBC} + V_{VMC} \tag{5}$$

Rearranging (5), the voltage gain of the proposed converter is given by

$$\frac{V_o}{V_{IN}} = \frac{3+2nk}{1-D} \tag{6}$$

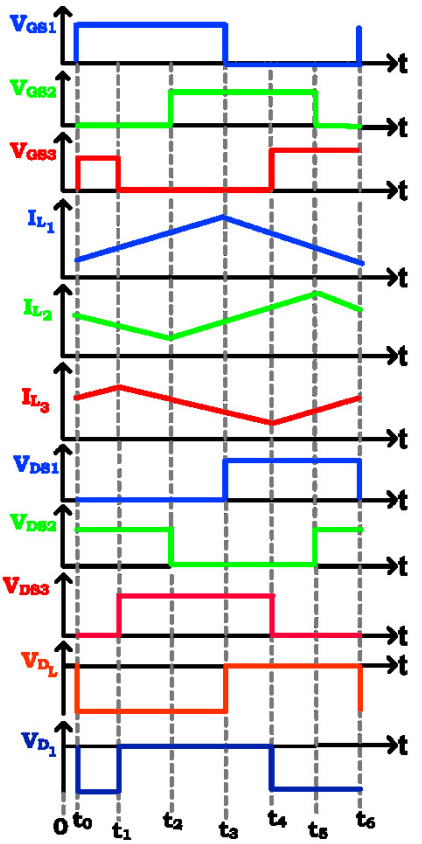

Fig. 3. Characteristic waveforms

3.2. Voltage stress on semiconductor devices

Due to lift capacitor, the voltage stress on the three power switches is not uniform. The voltage stress is given by

$$V_{S_1,S_2} = \frac{3}{1-D} V_{IN}, V_{S_3} = \frac{1}{1-D} V_{IN} \tag{7}$$

The voltage across the diode D_1 is same as the potential across C_L. The stress on D_2 is similar to a boost converter.

$$V_{D_1} = V_{C_L} = \frac{3}{1-D} V_{IN}, V_{D_2} = \frac{1}{1-D} V_{IN} \tag{8}$$

The voltage across the VMC diode D_3 is given by

$$V_{D_3} = \frac{2nk}{1-D} V_{IN} \tag{9}$$

The voltage stress on D_4 and D_o is very less as they are located near the load and conduct most of the time.

3.3. Design of energy storage elements

The specifications of the power circuit are provided in Table.1. The inductors in Stage 1 act as energy storage element in a conventional boost converter. Therefore, their values are computed from

$$L_{Py} = \frac{V_{IN} D}{3 f \Delta i_{L_{Py}}} \tag{10}$$

where $\Delta i_{L_{Py}}$ is the permissible current ripple. In the proposed converter, the inductors are designed by considering the current ripple as 25% of total input current.

Considering the output voltage ripple, the output capacitor is designed from

$$C_o = \frac{I_o D}{f \Delta v_C} \tag{11}$$

Table 1. Specifications of the presented convereter.

Parameter	Value	Component used in hardware	Part Number/Specification/Value
Input Voltage	24V	Power Switches S_1, S_2 and S_3	MOSFETs – IRFP4332 (250V, 60A, 29mΩ)
Output Voltage	260V	Diodes D_1, D_L, D_2, D_3 and D_4	MUR1540 (400V, 15A, 1.3V)
Output Power	500W	Voltage Lift Capacitor C_L	4.7μF, 400V – Polymer
Switching Frequency	50 kHz	Voltage Multiplier Capacitor C_1	2.2μF, 400V – Polymer
Primary Inductance	20μH	Voltage Multiplier Capacitor C_2	10μF, 450V – Electrolytic
Turns Ratio	1.5	Output Capacitor C_o	100μF, 400V – Electrolytic
Co-efficient of Coupling	0.75		
Duty ratio	0.5		

4. Results from Experimented Converter

The proposed converter was fabricated with the specifications provided in Table 1. To test the proposed converter, three gate pulses were generated by suitably programming a Piccolo digital signal processor (DSP) TMS320F28027. The gate pulses were suitably amplified using IR2110 MOSFET driver integrated circuit (IC). Fig.4a. shows the gate pulses applied to the switches S_1, S_2, S_3 and the output voltage of the power converter. The duty ratio and frequency of the gate pulses match with the design details. The converter yields a voltage gain of 10.5 which validates the design procedure adopted. As a large electrolytic capacitor was used at the output, the voltage ripple is negligible. The slight reduction in output voltage as seen from the experimental result is due to the voltage per division scale that was set in the digital storage oscilloscope (DSO).

Fig.4b shows the current through L_1, L_{2P}, L_{3P} and the input current. The total input current is shared by the three interleaved legs present in the proposed converter. As lift capacitor C_L has been used to enhance the voltage gain, the current sharing is unequal. However, the overall performance of the converter is not affected due to the asymmetry caused by C_L. The magnitude of total input current confirms the power handling capacity of the converter. The ripple current magnitude is higher than the expected value. This is because of the asymmetry in the interleaved structure and the duty ratio being greater than 0.33 (D=0.5).

Fig.4c shows the voltage stress on the switches and the output voltage. The maximum switch voltage stress occurs across switches S_1 and S_3. This stress is only about half of the output voltage. The switch voltage stress has been reduced due to the voltage lift concept and voltage gain extension technique which have been implemented in the proposed converter.

Fig.4d shows the photograph of the experimented converter. The simple inductor L_1 and both the coupled inductors were mounted on the main circuit board to reduce the overall size of the converter. For measuring inductor current, suitable arrangements were provided. The overall size of the converter could be reduced further by eliminating the current measurement ports.

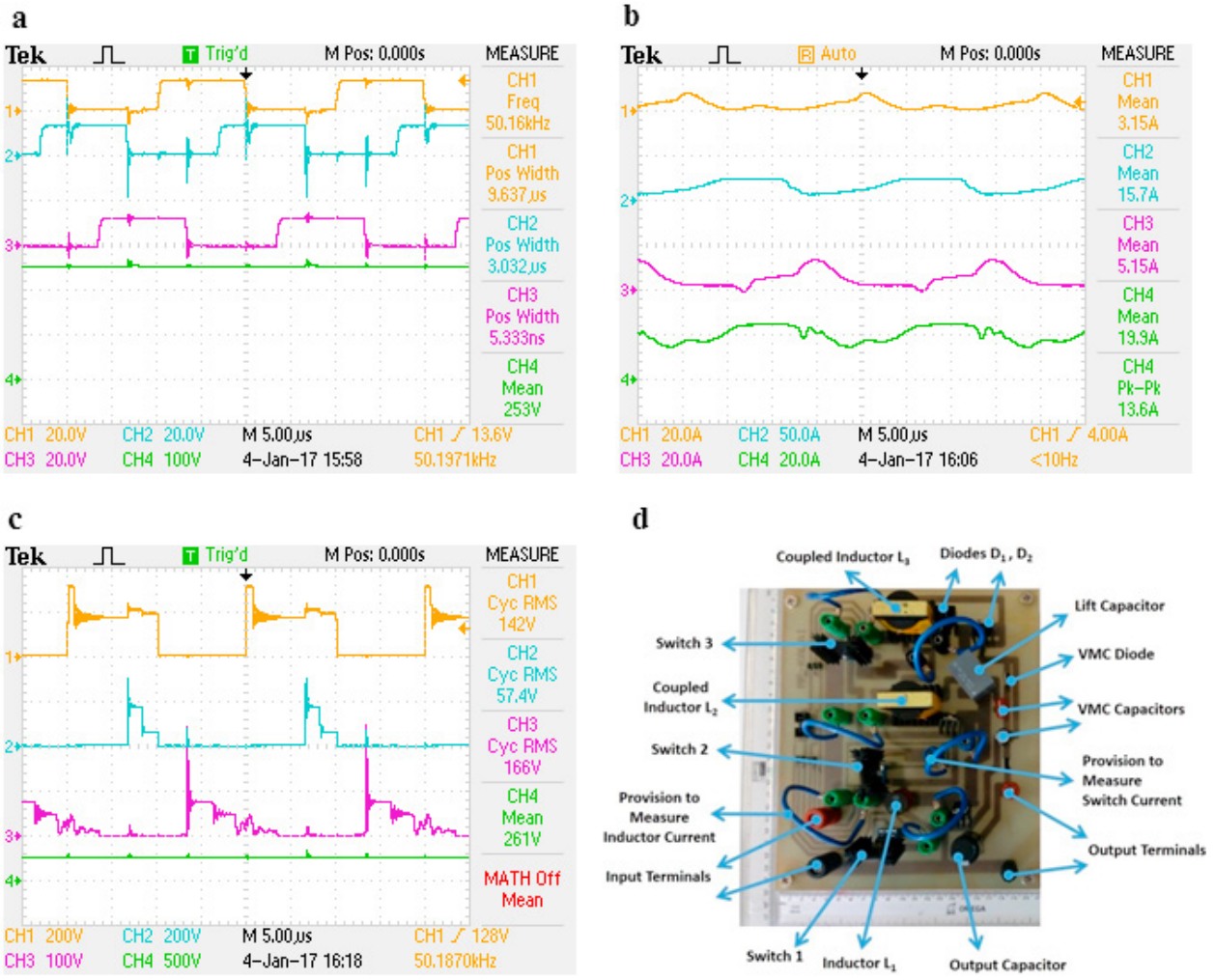

Fig.4. (a) Gate pulses (CH1-CH3) and output voltage (CH4); (b) current through primary windings (CH1-CH3) and input current (CH4); (c) voltage stress on switches (CH1-CH3) and output voltage (CH4); (d) photograph of the experimented converter.

5. Conclusion

In this paper, coupled inductor based high step-up DC-DC converter was proposed. The converter was developed from a three phase interleaved structure. Voltage lift capacitor, coupled inductors and voltage multiplier cells were used to extend the voltage conversion ratio. Resultantly, the voltage stress on the switches was reduced considerably. Experimental results prove that the converter yielded a voltage conversion ratio of 10.5 when operated at a duty ratio of D=0.5. Due to interleaving technique, the total input current was shared by the three interleaved phases. As asymmetry was introduced due to lift capacitor, the ripple current at the input was slightly higher. Some of the advantageous features of the proposed converter are (i) its ability to provide high gain at low duty ratio, (ii)

high power handling ability, (iii) low voltage stress on the switches and (iv) simple structure. With appropriate protection mechanisms and voltage regulation capability along with maximum power point tracking (MPPT) ability, this converter can conveniently be used for interfacing PV sources to a DC microgrid.

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