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Improved statistical variability and delay performance with junctionless inserted oxide FinFET

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Abstract

Junctionless inserted oxide FinFET (JL-iFinFET) is presented, its performance metrics are quantified and compared with JL-FinFET and JL-Stacked-Nanowire-FET (JL-SNWFET) respectively for the same foot-print on the wafer. The Random-Dopant-Fluctuation (RDF) and Metal-Gate-Granularity (MGG) are major variability sources in nano-transistors. Impedance Field Method is used to analyze the statistical variability performance of all three structures caused by RDF and MGG. The result shows JL-SNWFET provides superior DC figure-of-merits and 40% less statistical variability than JL-FinFET with a 10% increase in delay and considerable increase in fabrication complexity. The JL-iFinFET offers 30% lesser process-induced threshold voltage and on-current variations compare to JL-FinFET, without deteriorating delay and RF metrics due to its superior electrostatic control over the channel and multi-channel configuration. Fabrication of JL-iFinFET is also possible without adding much complexity in FinFET process it can be a major contender for continued scaling with JL-Transistors (JLTs).

***Keywords*— JL-iFinFET, RDF, MGG, Statistical variability, FinFET, Junctionless transistor.**

1. Introduction

Junctionless-Fin-Field-Effect-Transistor (JL-FinFET) proposed by J.P.Colinge et al., [1] gain researchers interest because of its nearly ideal Subthreshold Swing (SS), reduced process complexity and cost than inversion mode (IM) devices. In 7 nm and beyond technology, taller and thinner fins are required to get reasonable performance with the FinFET structure, which increases fabrication complexity and cost. To overcome increasing Short Channel Effects (SCEs) at scaling with the FinFET structure, SNWFET is

proposed which comes with the delay penalty and a considerable increase in process complexity. Recently iFinFET structure was proposed in [2] with improved performance than the FinFET structure with almost similar process complexity. The iFinFET structure has thin silicon channels which are separated by oxide (inserted oxide) layers.

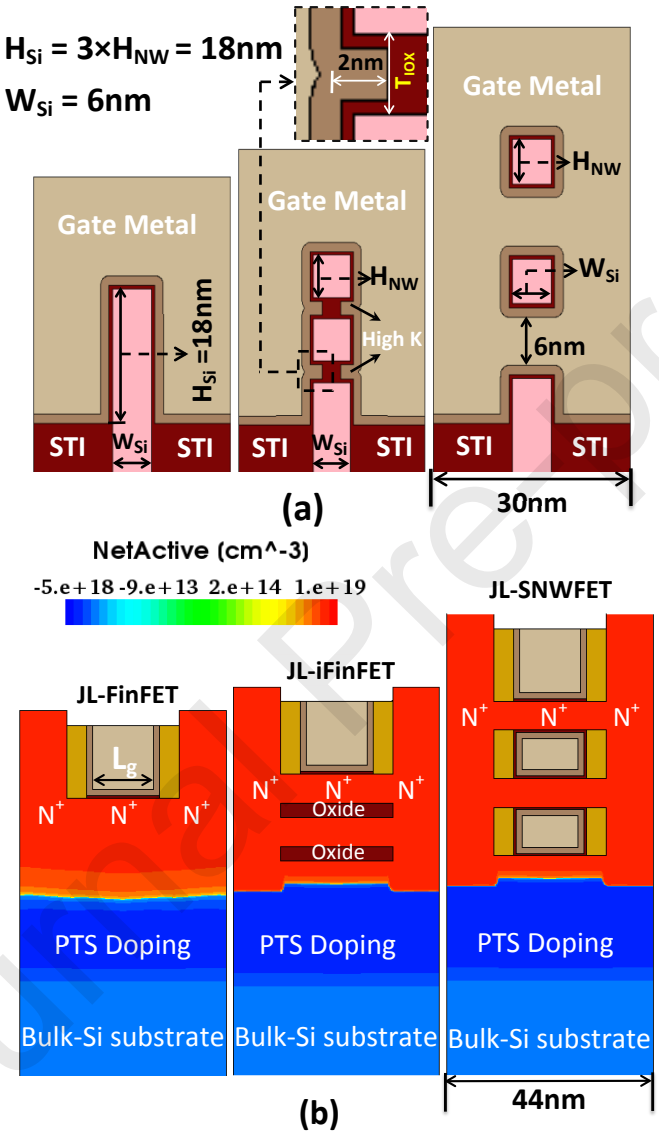

Fig. 1. Simulated device structures for comparison: (a) Cross-sectional view across the channel (X-Z plane). (b) Cross-sectional view along the channel (X-Y plane).

Inserted oxide layers improve electrostatic integrity by allowing fringing fields into the channel surface which provides better gate controllability over the channel potential. It is reported in [3] that increasing inserted oxide thickness (T_{IOX}) improves IM-iFinFET performance with slight increase in delay due to increasing coupling capacitance between the channels. Inversion mode operation mainly causes this delay penalty; it can be alleviated in junctionless transistor by partial depletion mode of operation. These

advantages show iFinFET can be a better structure for JLTs. In this paper key device metrics of JL-iFinFET such as on-current (I_{ON}), Drain Induced Barrier Lowering (DIBL), Intrinsic Delay (Delay), Maximum intrinsic gain (A_{V0}) are quantified and compared with JL-FinFET and JL-SNWFET. The nanoscale dimension makes recent technology devices to be more prone to process variations. In this paper, two major variability sources Random-Dopant-Fluctuation and Metal Gate Granularity induced statistical variation is studied in all three structures. Statistical Impedance Field Method (SIFM) available in Sentaurus device (Sdevice) [4] simulator is used to analyze the statistical variability which is, faster with reasonable accuracy [5, 6]. The RDF induced variations caused by difference in dopant position and concentration in channel of the transistor [7] it is dominant in JLTs due to high doping level at the channel. The actual position of the dopants in the channel cannot be controlled to be identical for all the devices, this work proposes using multi-channel configuration the impact of RDF can be reduced by 50%. The MGG induced variations caused by different workfunctions on metal surface due to different surface orientation of metal grains is another dominant variability in nanoscale transistor [8-10]. By increasing the number of grains covered in gate region, the impact of MGG induced variations can be reduced, on the other hand increasing gate area by Gate-All-Around (GAA) structure may leads to enhanced parasitic capacitance which deteriorate delay performance of the device. This work presents JL-iFinFET as a solution for this problem, it provides better delay and statistical variability performance than JL-FinFET for the same foot-print and silicon volume above STI (Shallow-Trench-Isolation).

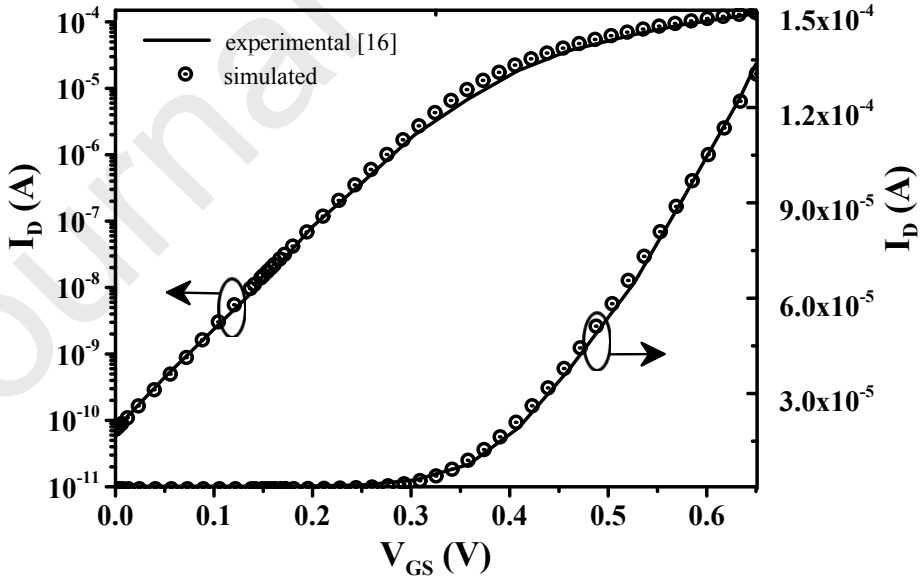

Fig. 2. Matched transfer characteristics with reference [16].

2. Device structure and simulation setup

The device structure is created by Sentaurus process (Sprocess) simulator [11]. The process flow followed is reported in our previous work [12], to reduce leakage current Punch-Through-Stopper (PTS) doping profile is used under the bottom channel. The PTS doping has acceptor doping concentration of $1\times10^{19}cm^{-3}$ to avoid parasitic leakage channel in substrate. The geometrical device parameters considered in this paper are listed in Table. 1. The cross-sectional view of JL-FinFET, JL-iFinFET, and JL-SNWFET from TCAD is shown in Fig.1. Silicon Nitride is used as spacer material and SiO_2, HfO_2 stack composes gate oxide with a thickness of 0.5 nm and 1.28 nm (EOT = 0.7 nm) respectively. The hetero gate oxide (combination of SiO_2, HfO_2) provides superior performance in junctionless transistors [13]. The constant donor concentration of 1×10^{19} cm^{-3} is considered throughout the device (source-channel-drain) and Titanium Nitride is used as gate metal. Sentaurus device simulator is used for 3-D device simulations. For a fair comparison off-current (I_{OFF}) is fixed as 100 pA/μm which is achieved by varying WorkFunction (WF) of gate metal, while the silicon volume above STI is considered as same for all three structures. The constant gate length (L_g) of 12 nm is considered for all three structures. 3-D device simulation is carried out by using Sdevice simulator. Drift-diffusion transport model with density gradient quantum correction is used for quantum effect consideration in nanostructure. To account for mobility dependence on electric field and various scattering mechanisms field dependent mobility model and Inversion-and-Accumulation-Layer mobility model (IAL-MOB) is used. The ionized impurity scattering is major contributor for mobility degradation in junctionless device it is accurately modeled in IAL-MOB model in Sdevice. The measured mobility for $1\times10^{19}cm^{-3}$channel concentration ($80cm^2/Vs$) [14, 15] is matching with the predicted mobility ($85cm^2/Vs$) in our simulation which validates the mobility model accuracy. To predict the subthreshold behavior accurately, band-to-band tunneling model is used with Shockley-Read-Hall (SRH) recombination model. Fig. 2 shows the matched I_D-V_{GS} curve with fabrication results [16] of SNSH-FET (NSH_W = 5 nm, NSH_W = 50 nm) for model parameters calibration. The model parameter calibration detail with the fabricated data is explained in our previous work reported in [17].

Table: 1. Device parameters.

Device Parameter	Range
Gate Length, L_g (nm)	12
Specific Contact Resistivity (Ω-cm^2)	1×10^{-8}
Donor Concentration (cm^{-3})	1×10^{19}
Channel width, W_{si} (nm)	6
Silicon height above STI, H_{si} (nm)	18
Effective Oxide Thickness, (EOT) (nm)	0.7

Table: 2. Transistor performance metrics comparison (V_{DS} = 0.65V).

FOMs	JL-FinFET	JL-iFinFET	JL-SNWFET
I_{ON} (μA)	7.74	9.23	11.1
I_{OFF} (pA)	4.2	5	6.6
V_{tsat} (V)	0.349	0.315	0.3
SS (mV/dec)	67.5	63.8	62.5
DIBL (mV/V)	44	36.6	30
C_{gg} (aF)	33	38.2	50.4
C_{gd} (aF)	10.6	12.8	17.5
Delay (pS)	2.68	2.69	2.95
A_{V0} (dB)	35	38.7	42
g_m (μS)	33	36.8	40

3. Results and Discussions

3.1 DC and RF performance comparison

Fig. 3(a) and 3(b) shows the transfer and output characteristics of all three structures (T_{IOX} = 3 nm). The JL-SNWFET has large drive current and better A_{V0} than other structures due to its superior electrostatic integrity. JL-iFinFET shows 18% improvement in drive current than JL-FinFET because of its improved electrostatic control over the channel potential. Fig. 4(a) projects the Electro-Static-Potential (ESP) across the channel for all three structures, which shows the superior electrostatic integrity of JL-SNWFET and JL-iFinFET over JL-FinFET. The Electron-density (edensity) across the channel, at different channels of JL-iFinFET and other two structures

obtained from TCAD, is presented in Fig. 4(b). The JL-iFinFET and JL-SNWFET has large edensity compared to JL-FinFET due to larger effective width provided by stacked channels. At bottom channel, edensity is less due to intruded dopants from PTS doping. Table. 2 shows the quantified FOMs, for fixed I_{OFF} and T_{IOX} of 100 pA/μm and 3 nm respectively. Intrinsic gain is given by, $A_{V0} = g_{m}/g_{ds}$ where g_m and g_{ds} are gate and drain transconductances. Drain Induced Barrier Lowering is computed as, $DIBL = (V_{tlin} - V_{tsat})/(V_{Dsat} - V_{Dlin})$ where, V_{Dlin} (0.05 V), V_{Dsat} (0.65 V) and V_{tlin}, V_{tsat} are linear and saturation supply voltages and threshold voltages respectively. The threshold voltage is extracted at drain current point $100nA \times W_{eff}/L_{eff}$, where W_{eff} is effective width and L_{eff} is effective gate length. From Table .2 it can be observed that JL-SNWFET has the largest delay than the other two structures, due to increased capacitance provided by gate-all-around configuration.

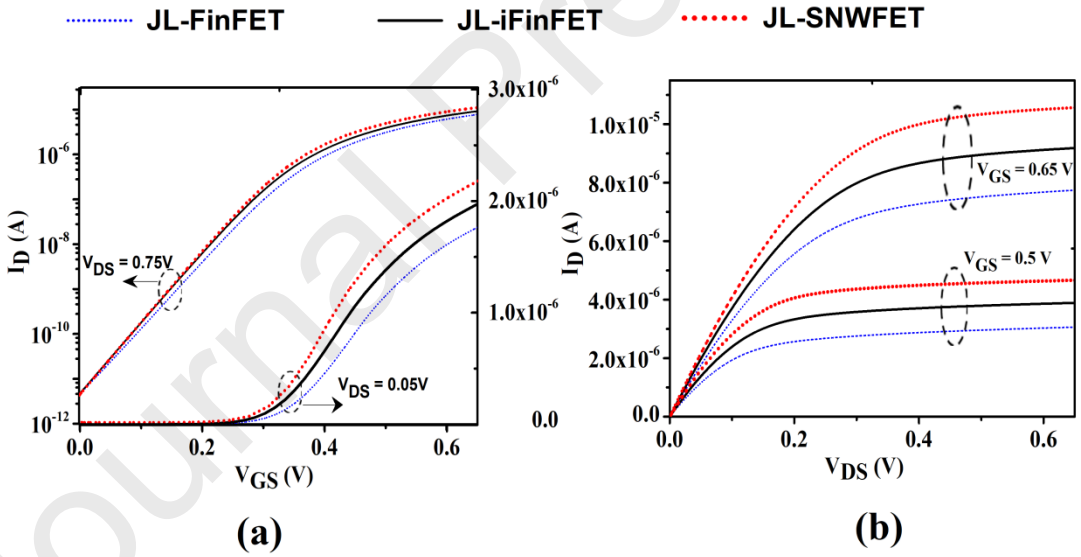

Fig. 3. (a). Simulated transfer characteristics for two different V_{DS} supply.(b). Simulated output characteristics for two different V_{GS} supply (for JL-iFinFET inserted oxide thickness is considered as, T_{IOX} =3nm).

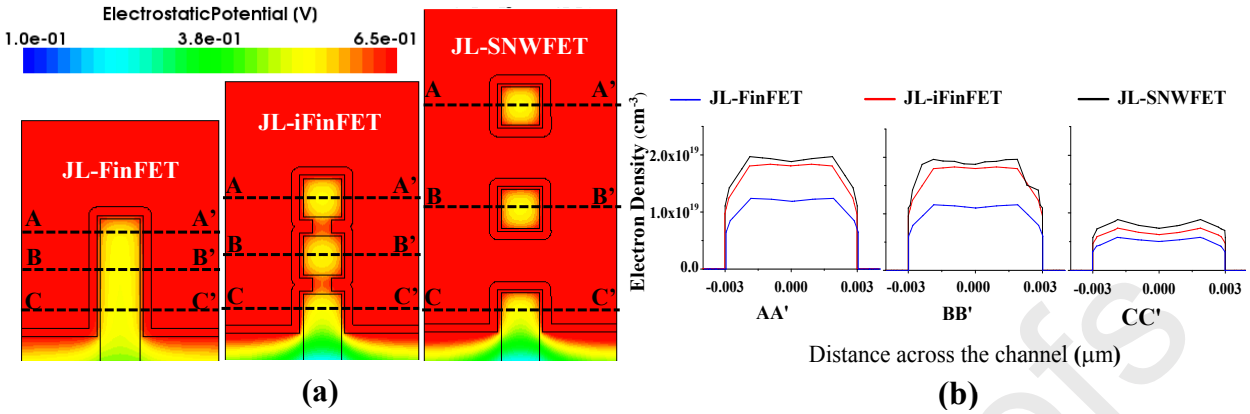

Fig. 4. (a). Electrostatic potential distribution across the channel, (b). Cutline electron density profile across the channels for different cutline (AA', BB', CC') positions. (T_{IOX} is fixed to 3nm, at supply voltages V_{GS} = 0.65V, V_{DS} = 0.05V).

In the case of JL-iFinFET performance improvement can be achieved without delay penalty because the enhanced drive current nullifies the impact of increment in capacitance. The intrinsic delay ($(C_{gg} \times V_{DD})/I_{ON}$) and other device metrics of JL-iFinFET can be improved further by increasing T_{IOX}. The quantified FOMs for fixed I_{OFF} (100 pA/μm), of JL-iFinFET for different T_{IOX} are presented in Table. 3. Because of partial depletion mode of operation increase in C_{gg} caused by enhanced coupling capacitance (shown in Fig. 5(a)) is less effective than an increase in drive current there by 5% improvement in the intrinsic delay is achieved. Fig. 6 shows the comparison of carrier density in channel between junctionless and IM-iFinFET device at saturation supply voltage (V_{GS} = V_{DS} = V_{DD} =0.65V). As the carrier density is concentrated at middle of the channel in case of JL device due to (bulk conduction) partial depletion mode of operation [18] the coupling capacitance between nanowires increase is not much compared to IM device as a result increasing T_{IOX} improves the delay performance. Intrinsic delay as a function of T_{IOX} is shown in Table 3. Due to enhanced gate control 15% reduction in DIBL is achieved with JL-iFinFET, which eventually leads to 5% improvement in A_{V0} (in dB) for an increase in inserted oxide thickness from 3 to 5 nm. Comparison of computed current-cutoff frequency ($f_T = g_m/(2\times\pi\times C_{gg})$) [19-22] for all structures is displayed in Fig. 5(b), which shows JL-iFinFET has superior performance compared to JL-FinFET and JL-SNWFET. Fig. 7 displays the obtained g_m, g_{ds} and A_{V0} as a function of V_{GS} for different structures which shows JL-SNWFET has maximum gain due to larger g_m and maintained g_{ds}.

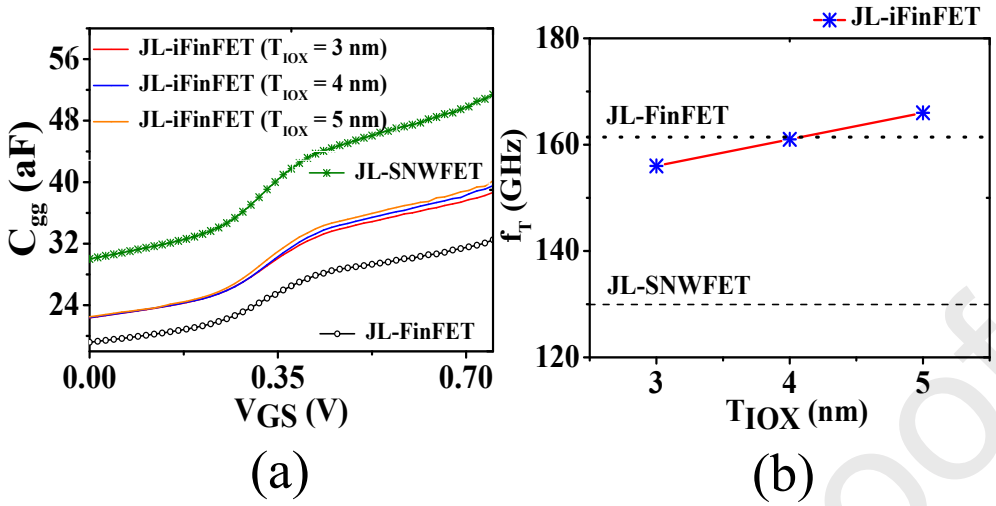

Fig. 5. (a). Total gate capacitance as a function of gate voltage for different T_{IOX}. (b). current-cutoff-frequency as a function of T_{IOX} (V_{DS} = 0.65V).

Table: 3. Impact of inserted oxide thickness on performance metrics of JL-iFinFET (V_{DS} = 0.65V).

T_{IOX} (nm)	I_{ON} (μA)	DIBL (mV/V)	C_{gg} (aF)	g_m (μS)	Delay (pS)	A_{V0} (dB)
3	9.23	36.6	38	36.8	2.69	38.7
4	9.93	33.3	38.6	38.5	2.52	40.2
5	10.5	32	39.3	40.3	2.43	40.6

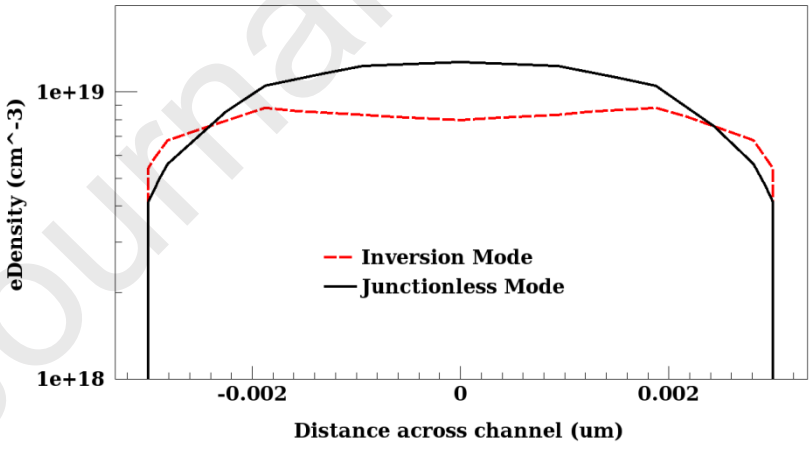

Fig. 6. Comparison of e-Density profile across the channel of JL and IM device at V_{GS} = V_{DS} = 0.65V (cut-line taken at middle of channel, IM device channel acceptor doping concentration is considered as $1\times10^{17}cm^{-3}$).

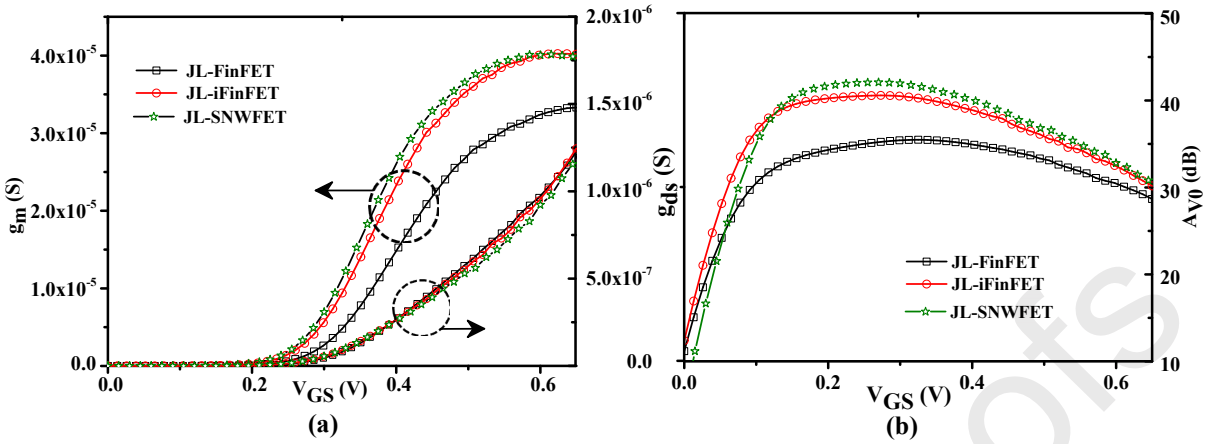

Fig. 7. (a). Obtained g_m and g_{ds} (b). Computed A_{V0} as a function of gate voltage for different structure (T_{IOX} = 5 nm, V_{DS} = 0.65V).

3.2 **Statistical variability performance comparison**

Statistical variability analysis was performed using SIFM in Sdevice simulator with the sample size of 1000. In SIFM the variability sources such as MGG and RDF are considered as a perturbation to the reference structure and response to this perturbation is assumed to be linear. Using green's function linear current response for each randomized structure is computed as explained in [6, 12, 23]. Using the computed linear current response for each bias point and transfer characteristics of unperturbed reference device, the transfer characteristics of randomized sample is computed by weighted-IV method available in Sentaurus visual (Svisual) tool [24]. From computed transfer characteristics of randomized samples interested device metrics are extracted and used for statistical analysis.

To analyze the impact of MGG average grain size used as 5 nm and 40%, 60% probability of occurrence is assumed for grains with WF+200, WF-200 meV [9, 25-27] respectively. To analyse the impact of statistical variability threshold voltage and on-current variability factor (β%) are considered as FOMs. The β% for each randomized sample is computed by equation. 1, which gives how much percentage deviation in on-current is observed in randomized sample from reference device (I_{ON} on-current of randomized sample and $< _{ON} >$ is average on-current for 1000 randomized samples). Fig. 8(a) and 8(b) shows the distribution of threshold voltage and β% obtained for 1000 randomized samples considering RDF effect only, similarly Fig. 9(a) and 9(b)

shows MGG induced threshold voltage and on-current variability. Both Fig. 8 and 9 depicts the distribution of threshold voltage and β% are following normal distribution for all three structures (solid line), which shows it can be easily modelled for circuit simulation. The standard deviation of the threshold voltage (σV_{TH}) and on-current variability factor ($\sigma\beta\%$) caused by RDF and MGG respectively, for all three structures are listed in Table. 4. Due to high doping level RDF is dominant variability source in JLTs, both V_{TH} and β% spread is more for RDF induced variation. The JL-iFinFET and JL-SNWFET have better immunity towards threshold variability and on-current variability caused by RDF and MGG because of: (i). Enhanced electrostatic control over the channel potential [7]. (ii). larger effective gate contact area. (iii) Threshold averaging caused by multi-channel setup [28]. The MGG induced threshold voltage variability is given by equation. 2 [29] (σWF and N_{grain} is the standard deviation of workfunction between grains and the number of grains on gate surface). Due to larger gate contact area the JL-iFinFET and JL-SNWFET has higher N_{grain} along with multi-channel configuration which leads to 30% and 40% better variability performance compare to JL-FinFET.

$$\beta = \frac{I_{ON} - < I_{ON} >}{< I_{ON} >} \times 100\% \quad (1)$$

$$\sigma V_{TH} = \frac{\sigma WF}{\sqrt{N_{grain}}} \quad (2)$$

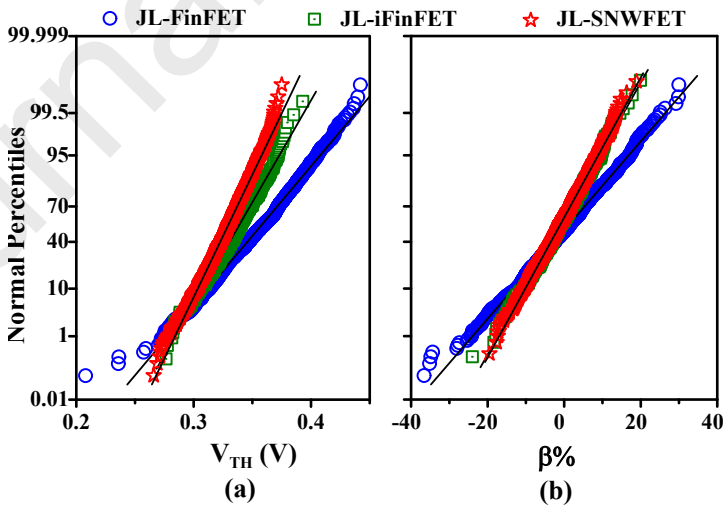

Fig. 8. Statistical variability comparison between different structure for RDF induced (a) V_{TH} variability and (b) β% variability (V_{DS} = 0.05 V).

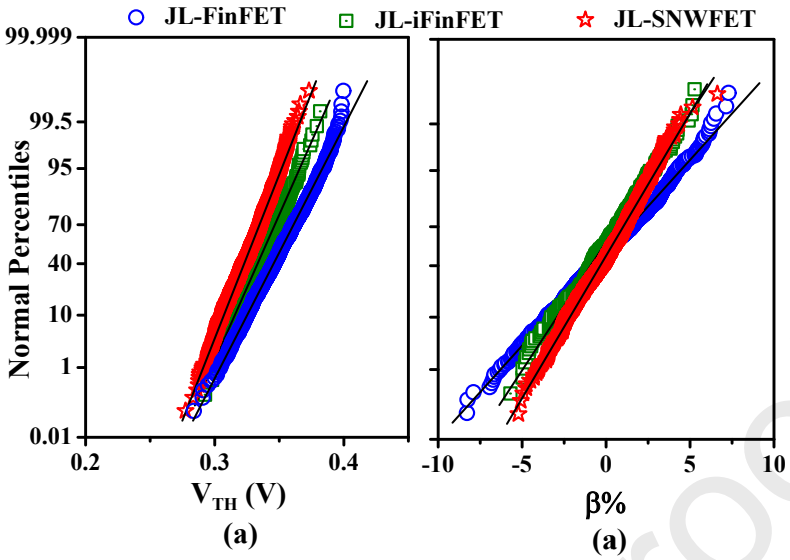

Fig. 9. Statistical variability comparison between different structure for MGG induced (a) V_{TH} variability and (b) β% variability (V_{DS} = 0.05 V).

Table: 4. Statistical variability comparison between different structure (V_{DS} = 0.05 V).

Device Structure	RDF		MGG		RDF+MGG	
	σV_{TH} (mV)	σβ (%)	σV_{TH} (mV)	σβ (%)	σV_{TH} (mV)	σβ (%)
JL-FinFET	32.6	10.2	20	2.7	40	10.6
JL-iFinFET	22	7	16.8	2.1	27	7.3
JL-SNWFET	18	6	15.2	1.75	23.8	6.3

In order to analyze the impact of the number of channels on statistical variability single, double and three channel stacked nanowire FET is simulated (all channels considered GAA) and its statistical variability performance is analyzed. Fig. 10 (a,b) and 11(a,b) shows the distribution of threshold voltage and β% due to RDF and MGG, obtained for 1000 randomized samples for different number of channels. As the doping in different channel is assumed to be independent in all three channels, different doping distributions averages the threshold [28] level at different channel as a result threshold voltage and on-current variability is reduced with increasing number of channels.

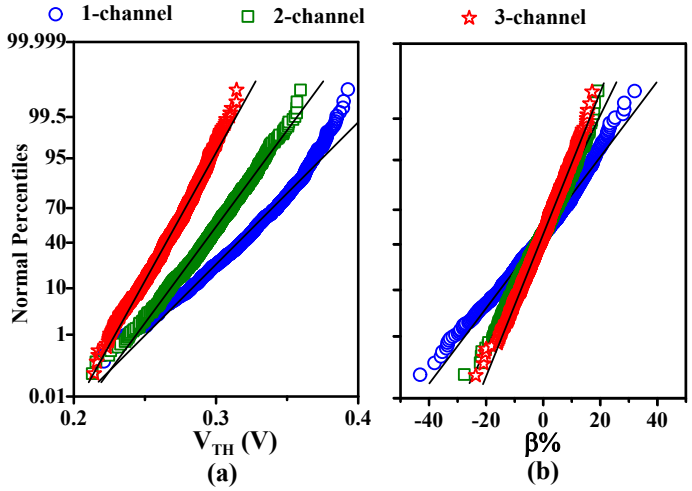

Fig. 10. Statistical variability comparison between JL-SNWFETs with different number of channels, for RDF induced (a) V_{TH} and (b) β% variability (V_{DS} = 0.05 V).

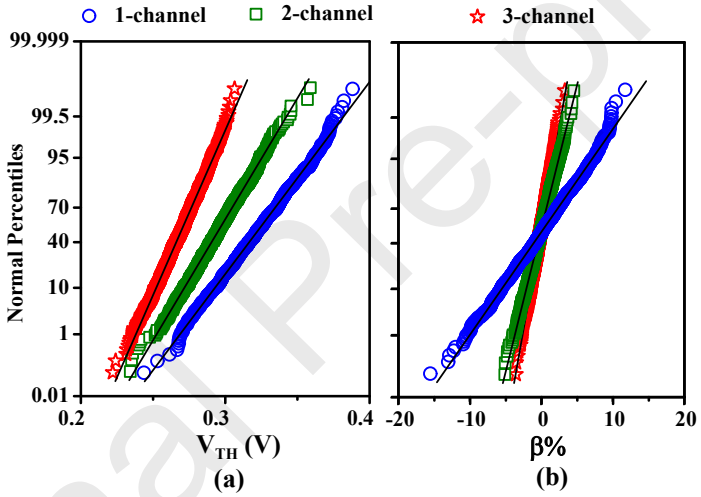

Fig. 11. Statistical variability comparison between JL-SNWFETs with different number of channels, for MGG induced (a) V_{TH} and (b) β% variability (V_{DS} = 0.05 V).

Table: 5. Impact of multiple channels on statistical variability performance(V_{DS} = 0.05 V).

Device Structure	RDF		MGG		RDF+MGG	
	σV_{TH} (mV)	σβ (%)	σV_{TH} (mV)	σβ (%)	σV_{TH} (mV)	σβ (%)
1-channel	31	11.8	23	4.31	38	12.5
2-channel	20	7.55	16.2	1.54	26.3	7.8
3-channel	17	5.5	13.6	1.1	21.9	6

The standard deviation of the threshold voltage and on-current variability factor caused by RDF and MGG respectively for different number of channels is listed in Table. 5. Around 30% and 40% improvement is observed in V_{TH} variability by increasing the number of channels from

1 to 2 and 3 respectively. 38% and 52% reduction in on-current variability is observed for 2 and 3-channel JL-SNWFET than single channel which proves reduction in statistical variability with increase in number of channels. To compare different structures threshold variability factor (A_{VT}) is used, which shows threshold variability per effective area it is computed by equation. 3 (W_{eff} and L_{eff} are effective width and length respectively).

$$A_{VT} = \sigma V_{TH} \times \sqrt{2} \times \sqrt{W_{eff} \times L_{eff}} \quad (3)$$

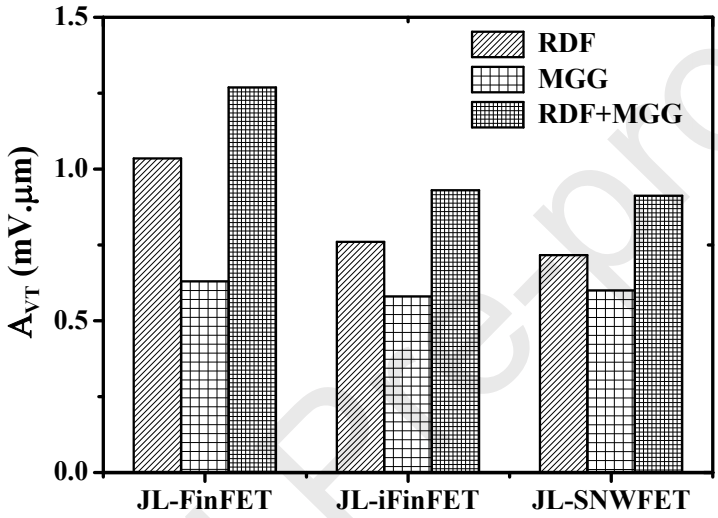

Fig. 12. A_{VT} factor comparison between different structure (V_{DS} = 0.05 V).

Fig. 12 compares the A_{VT} factor computed for JL-FinFET, JL-iFinFET and JL-SNWFET, which shows JL-iFinFET almost matching JL-SNWFET statistical variability performance. In case of JL-SNWFET the better statistical variability performance obtained with 10% larger delay and increased process complexity as a penalty. As JL-iFinFET outperforms JL-FinFET in terms of both RF/analog performance and statistical variability without causing much increase in process complexity it can be an alternate to FinFET structure.

4. Conclusions

Junctionless inserted oxide FinFET (JL-iFinFET) is presented and its DC and statistical variability metrics are compared with JL-FinFET and JL-SNWFET for the same foot-print. The JL-SNWFET provides superior DC and statistical variability metrics compare to JL-FinFET with increase in

delay penalty and fabrication complexity. With the presented JL-iFinFET considerable improvement in DC and statistical variability metrics is achieved compare to JL-FinFET without increasing delay penalty and fabrication complexity. Impact of number of channels on statistical variability is analyzed and it is found that increasing the number of vertically stacked channels of a transistor with the same foot-print effectively improves the immunity of the device towards statistical variability. For better RF/analog operation f_T has to enhance without degrading A_{V0} which is contented by JL-iFinFET along with superior statistical variability performance as an added benefit. These advantages make the JL-iFinFET as a promising candidate for continued scaling with junctionless transistors over JL-FinFET.

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