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Investigation of Radiation Hardened TFET SRAM Cell for Mitigation of Single Event Upset

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ABSTRACT This study analyzes the soft error sensitivity of SRAM cell which employs double-gate tunnel field effect transistor (DG TFET). The mitigation technique for the data recovery after the heavy ion strike is discussed. The conventional 6T TFET SRAM cell is designed using DG TFET of 30 nm. For the circuit simulation, the symbol of DG TFET is developed with the help of a look-up table based Verilog-A code. The radiation induced single event upset (SEU) causes a change in the stored data of SRAM cell. In order to improve the SEU sensitivity, the radiation hardening-by-design technique (RHBD) is introduced in 6T TFET SRAM cell by connecting the RC feedback loop between the two cross coupled inverters. The standby power of the TFET SRAM cell is calculated and compared before and after the radiation mitigation technique insertion.

INDEX TERMS Double gate TFET, radiation hardening-by-design, single event upset, TFET SRAM.

I. INTRODUCTION

Radiation induced single event upset (SEU) is a soft error caused by a transient signal induced by an energetic particle (e.g., protons, neutrons, alpha particles or other heavy ions) strike. The charged particle passing through the semiconductor device generates electron-hole pairs along its path. The collected charge (Q_{coll}) of electron-hole pair can change the state of the memory cell, register, latch or flip flops, only if it is greater than the critical charge (Q_{crit}), which is the minimum charge required to trigger a change in the data state [1], [2]. Simulation of SEU can be performed with either the circuit simulators such as SPICE [3]–[5], or drift-diffusion finite element device simulators [6]–[8]. Circuit simulators have the advantage of being computationally efficient than device simulators. In circuit level simulation, the SEU is emulated by inserting a transient current source to strike at the circuit node [7], [9]. Static circuit like SRAM is the dominant form of embedded memory occupying majority of the total chip area in IC products. Due to the down scaling technology, SRAM is more susceptible to radiation induced SEU [10]–[12].

A technique, commonly known as radiation hardening-by-design (RHBD) is used to mitigate the soft error caused by the ionizing radiation in circuit level [13]. FinFET SRAM circuits have better soft error immunity than CMOS SRAM [14]–[16]. To mitigate the SEU effect in FinFET based circuits, the radiation hardened circuits have been reported [17], [18]. Tunneling field effect transistors (TFETs) with steep sub-threshold slope have become emerging devices in ultra-low power applications [19]–[21]. Several studies on the TFET based SRAM circuits have been reported [22]–[25]. The soft error generation and propagation in Si FinFET, III-V FinFET, and III-V Hetero-junction tunnel FET (HTFET) are investigated using device and circuit simulation [26].

In this paper, the soft error performance, its mitigation technique and the power consumption before and after the radiation are studied in 6T SRAM cell using DG (Double Gate) TFETs. This paper is organized as follows: Section II describes the DG TFET device structure and simulation methodology. Section III explains the SEU effect and its mitigation technique on 6T TFET SRAM cell. Section IV provides the conclusion.

II. DEVICE STRUCTURE AND SIMULATION METHODOLOGY

Technology computer-aided design (TCAD) is used for TFET device simulation [27]. The 2-D structure of n- and

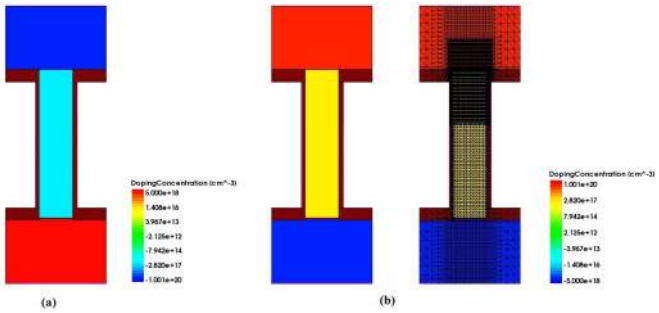

FIGURE 1. Simulated structure of DG TFET (a) n-type (b) p-type (without and with meshing).

TABLE 1. Device specifications.

Parameters	n/p-Type
Gate length (L_g)	30 nm
Body thickness (T_{ch})	8 nm
Gate oxide thickness (T_{ox})	1 nm
Source doping concentration (N_s)	1×10^{20} cm^{-3}
Drain doping concentration (N_d)	5×10^{18} cm^{-3}
Channel doping concentration (N_{ch})	1×10^{17} cm^{-3}

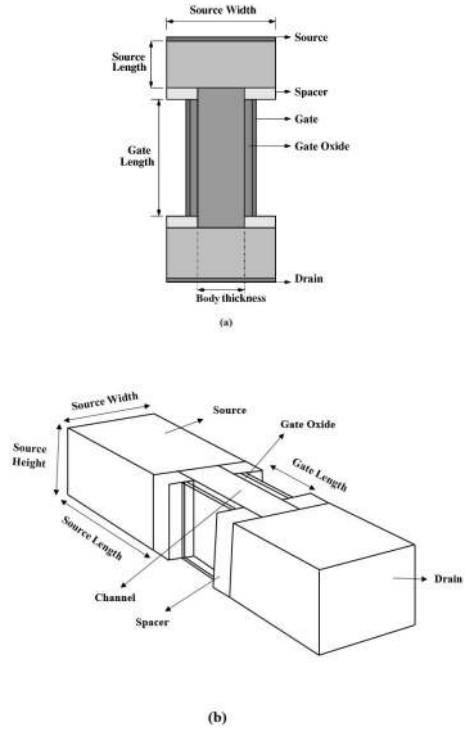

FIGURE 2. Schematic structure of DG TFET (a) 2D view (b) 3D view.

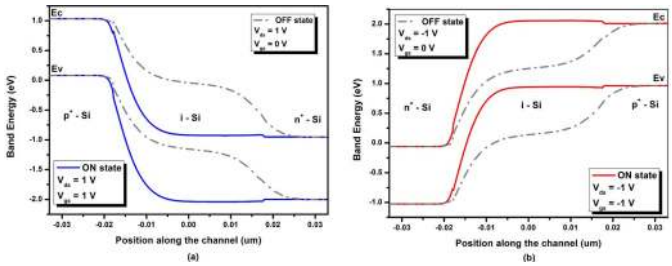

FIGURE 3. Simulated energy band diagram (a) n-type DG TFET (b) p-type DG TFET.

p-type Silicon based DG TFET is shown in Fig. 1(a) and (b). Figure 2(a) and (b) depict the 2-D and 3-D schematic diagrams of DG TFET which shows various parameters of the device. The meshing is applied in the entire device to create the calculation points where the current and voltage equations are solved. It can be seen from Fig. 1(b) that a very fine mesh is applied between the source and channel region where the tunneling occurs. Thus the accurate values of current and voltages can be predicted at the tunneling junction. The device dimensions are given in Table 1 and the device is calibrated against the published results [28]. The device simulator includes appropriate models for doping dependence mobility, effects of high and normal electric fields on mobility, quantum confinement model and velocity saturation. A non-local Hurkx band-to-band tunneling incorporated with Shockley-Read-Hall recombination model is used along with Fermi-Dirac statistics. The supply voltage used in this study is 1 V.

The tunneling current of TFET (I_{on}) can be derived by using Wentzel-Kramers-Brillouin (WKB) approximation method [29], which is given by,

$$I \propto exp\left(-\frac{4\Lambda\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar\left(\Delta\phi + E_g\right)}\Delta\phi\right) \tag{1}$$

where m^* is the effective carrier mass, E_g is the bandgap, e is the electron charge, $\Delta\phi$ is the energy range over which the tunneling can take place, $\hbar$ is the Planck's constant and Λ is the spatial extent of the transition at source-channel interface. Λ can be defined by

$$\Lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{ox}t_{Si}} \tag{2}$$

where t_{ox}, t_{Si}, ε_{ox}, and ε_{Si} are the oxide and silicon-film thickness and dielectric constants, respectively. Figure 3(a) and (b) shows the band diagram of n- and p-type DG TFETs, respectively. In the absence of gate voltage ($V_g = 0$ V), the tunneling barrier is large enough to give a small leakage current (I_{off}). In ON state ($V_g = 1$ V), in case of n-TFET, the positive gate voltage makes the tunneling junction between source and channel. For the p-TFET, the tunneling junction occurs between drain and channel when the negative gate voltage is applied.

The I_d-V_g characteristics of both n- and p-type DG TFET is depicted in Fig. 4. The linear and log scale of the plot is denoted in left and right Y axis respectively.

A. DEVICE-TO-CIRCUIT MODELING

Since compact SPICE models for TFETs are yet to be developed, the look-up table based Verilog-A code for DG TFETs is generated using the results extracted from TCAD

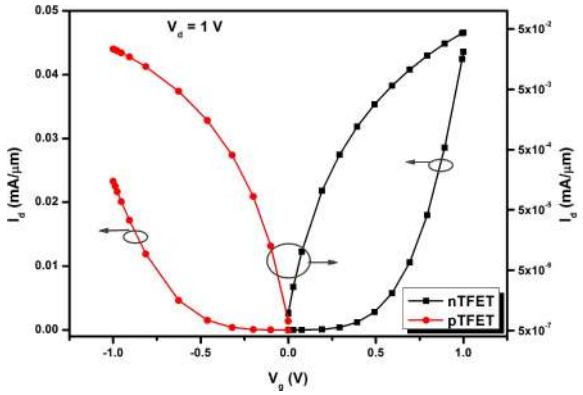

FIGURE 4. I_d-V_g characteristics of n- and p-type DG TFETs.

Algorithm 1 Sample Verilog-A Code for n-TFET

```
module NTFET(d,g,s);
inout d,g,s;
electrical d,g,s;
real Ids, Cgs, Cgd;
parameter real w=1; //Device width
analog begin
Ids = $table_model(V(d,s), (V(g,s)), "IdVg-ntfet.tbl","1LL,1LL");
Cgd = $table_model(V(d,s), (V(g,s)), "Cgd-ntfet.tbl","1LL,1LL");
Cgs = $table_model(V(d,s), (V(g,s)), "Cgs-ntfet.tbl","1LL,1LL");
I(d,s) <+ Ids*w;
I(g,d) <+ Cgd*ddt(V(g,d))*w;
I(g,s) <+ Cgs*ddt(V(g,s))*w;
end
```

to enable circuit simulations. The flowchart for look-up table based Verilog-A model generation from TCAD simulations is shown in Fig. 5. The current and capacitance characteristics are extracted from both the DC and AC simulations respectively. The device characteristics, I_{ds} (V_{ds}, V_{gs}), C_{gs} (V_{ds}, V_{gs}), C_{gd} (V_{ds}, V_{gs}) are captured in two dimensional look-up tables and employed by the Verilog-A code [30]–[33]. This Verilog-A code is implemented as a three terminal device (source, gate and drain) by using Cadence Virtuoso tool. Algorithm 1 shows a sample Verilog-A code for the n-TFET. In this code, $table_model function needs three inputs: V_{ds} (1st column of the look-up table), V_{gs} (2nd column of the look-up table) and current or capacitance values (3rd column of the look-up table). The values (I_{ds}, C_{gs}, C_{gd}) are assigned from the look-up tables in ".tbl" according to the terminal voltages. The circuit symbol for n- and p-type DG TFETs are represented in Fig. 6(a) and (b), respectively.

III. SEU IN TFET BASED SRAM CELL

The 6T TFET SRAM cell is constructed with DG TFETs. The schematic of 6T TFET SRAM cell is shown in Fig. 7, where n- and p-type DG TFETs are employed for the two cross coupled inverters (M1, M2 and M3, M4). M1 and M3 are the pull-up transistors (PU) and M2 and M4 are the pull-down transistors (PD). M5 and M6 are the n-type access transistors (ATs). BL and BLB are the input bit lines to the SRAM cell. The word line (WL) is used to control the ATs.

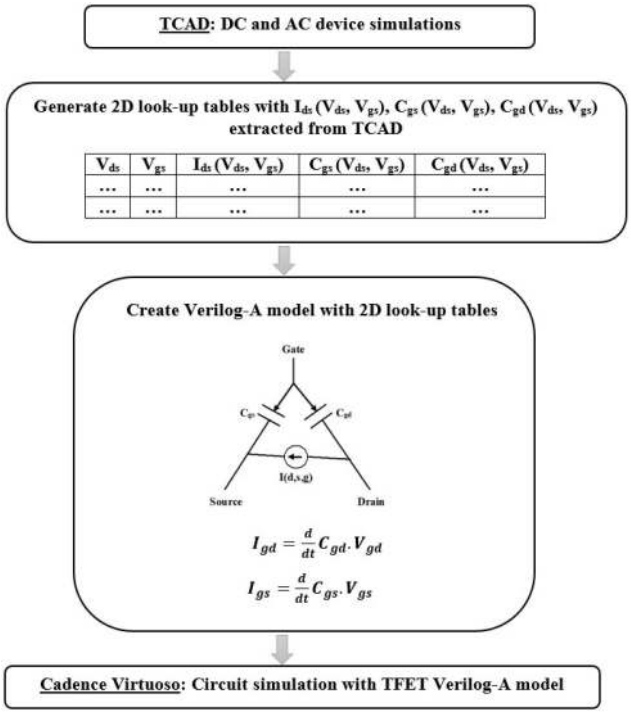

FIGURE 5. Flowchart for look-up table based Verilog-A model generation from TCAD simulations.

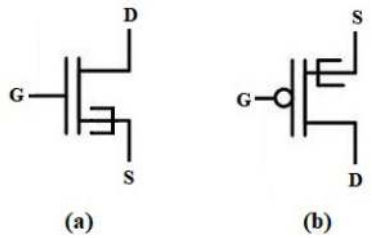

FIGURE 6. Symbol of DG TFETs (a) n-type (b) p-type.

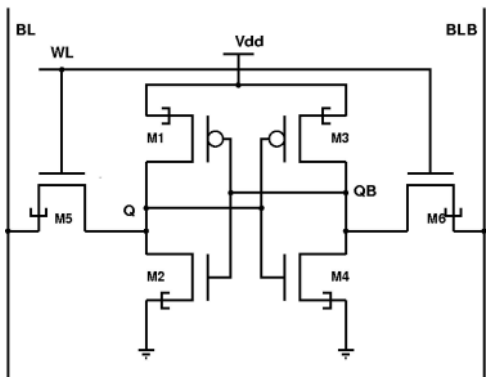

FIGURE 7. 6T TFET SRAM cell.

The timing diagram of 6T TFET SRAM cell is illustrated in Fig. 8. When WL is high, the ATs (M5 and M6) get turned ON and the data stored at the nodes Q and QB reflects the inputs BL and BLB, respectively. When WL is low, the data

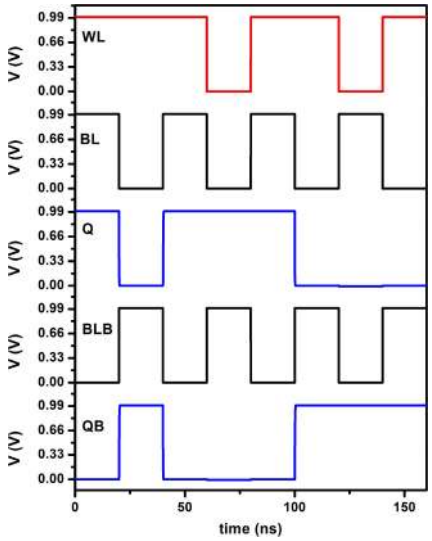

FIGURE 8. Timing diagram of 6T TFET SRAM.

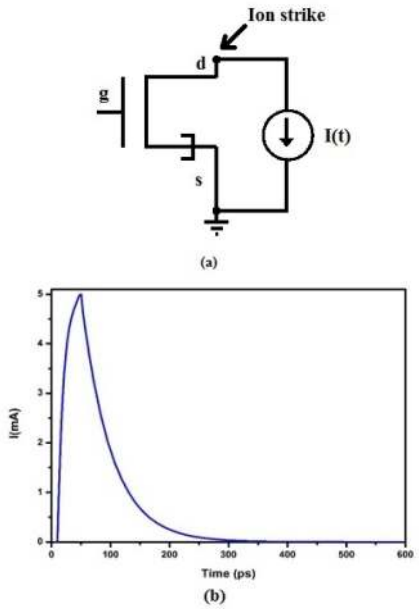

FIGURE 9. (a) Ion strike tunneling by a current source (b) current pulse.

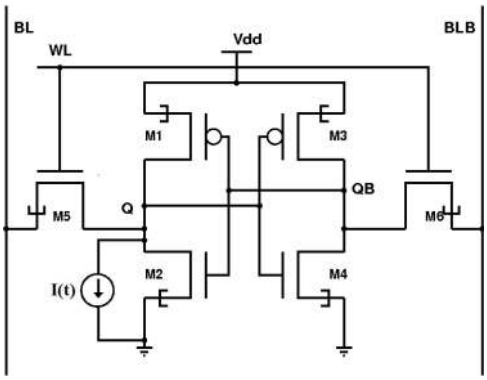

FIGURE 10. 6T TFET SRAM cell with injected current source.

stored at the nodes Q and QB retains its values until WL goes high.

The modeling of an SEU at circuit level is done by connecting a transient current source at the impact node (drain of M2) and measuring node voltages (Q and QB). Generally, the sensitive part of the inverter configuration is the drain of the n-type transistor, which is in OFF state [34]. The particle strike modeled by a current source used in this study is represented in Fig. 9(a). The models derived by the researchers to characterize Q_{crit} are as follows, (i) simplified model by Roche (ii) current model by Freeman (iii) diffusion collection model and (iv) double exponential current model [7]. The most widely used model to find out the single event transients introduced by the ion strikes is double exponential current model, which is described as [35],

$$I(t) = I_o\left\{exp\left(\frac{-t}{\tau_\alpha}\right) - exp\left(\frac{-t}{\tau_\beta}\right)\right\} \tag{3}$$

where $I_o = Q_{coll}/(\tau_\alpha - \tau_\beta)$, in which I_o is the magnitude of the current pulse. τ_α and τ_β is the time constants of the exponentials. For instance, the injected current pulse shown in Fig. 9(b) uses $I_o = 5$ mA , $\tau_\alpha = 50$ ps, and $\tau_\beta = 10$ ps.

Figure 10 shows the schematic of 6T TFET SRAM cell with current source introduced at the drain of M2 which is in OFF state. To measure Q_{crit}, the current source denoted in Equation (3) is injected at the drain node of M2 and $I(t)$ is swept until the bit flip occurs [35]. The resultant transient voltage is observed at I_o of 5 mA, τ_α of 50 ps and τ_β 10 ps. Figure 11 depicts the node voltages of 6T TFET SRAM due to the SEU effect.

- '1' to '0' upset at Q: The voltage at the drain node of the transistor M2 is discharged to a value below 0 V due to the charge collection resulted from the heavy ion strike [36]. It is shown in Fig. 11(a).
- '0' to '1' upset at QB: The voltage change ('1' to '0') at the node Q due to the heavy ion strike, turns on transistor M3 and cuts off M4. It makes the data change at the node QB [36]. It is depicted in Fig. 11(b).

A. RHBD TECHNIQUE

The RHBD technique can be applied to the circuit design for reducing the soft error sensitivity by including RC feedback loop. Figure 12 depicts the radiation hardened 6T TFET SRAM cell. In this circuit, the radiation effect caused by the injected current source at drain node of M2 is removed by connecting the RC feedback loops (R1, C1 and R2, C2) between the two cross coupled inverters (M1, M2 and M3, M4). The values of R1, R2 and C1, C2 are chosen to be 50 ohms and 10 pF respectively, which are used to slow down the propagation of voltage transients and increase the Q_{crit} [37]. It is known that whenever $Q_{coll} < Q_{crit}$, the soft error will be mitigated [38]. The data recovery mechanism for the radiation hardened TFET SRAM cell is presented.

- When the node Q flipped from 1 to 0 due to the heavy ion strike, M4 is temporarily OFF. The voltage at the

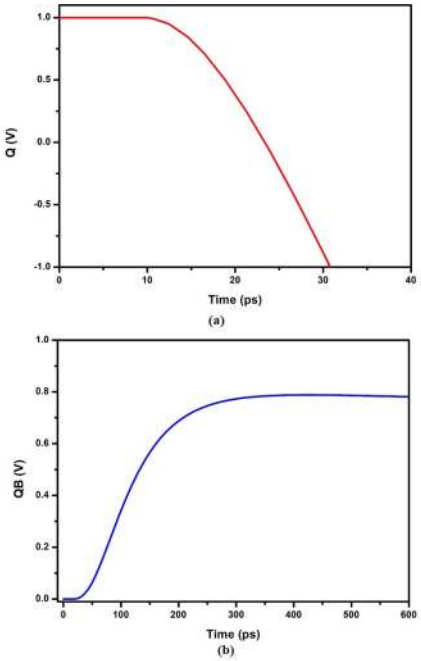

FIGURE 11. Node voltages due to SEU (a) '1' to '0' upset at Q (b) '0' to '1' upset at QB.

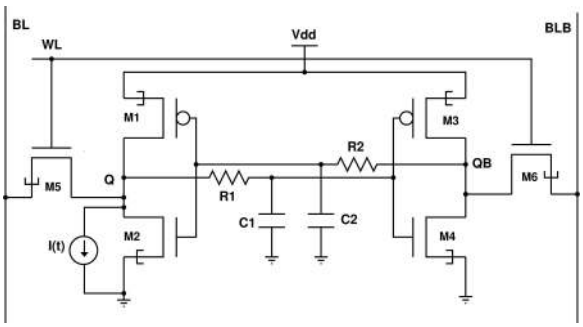

FIGURE 12. Radiation hardened 6T TFET SRAM cell.

inverter 1 is in initial state (logic 0). Consequently, M1 is always ON. Therefore, Q will be flipped to its initial state (logic 1) as shown in Fig. 13.

- The data change at the node Q ('0' to '1') turns on the transistor M4 and the data at the node QB will be recovered.

Due to the use of RHBD technique, the SEU effect of 6T TFET SRAM cell is reduced and this is evident from the plot of node voltages which is illustrated in Fig. 13. It can be seen from the plot that the short-lived transients cannot disturb the other nodes and hence the node voltages Q and QB are recovered to its initial states due to the connection of feedback loops between the two cross coupled inverters [39].

B. CELL AREA, DELAY AND POWER ANALYSIS

The cell area, delay and power dissipation of the 6T TFET SRAM will be affected due to the insertion of RC feedback loops. In order to evaluate the cell area required for the 6T

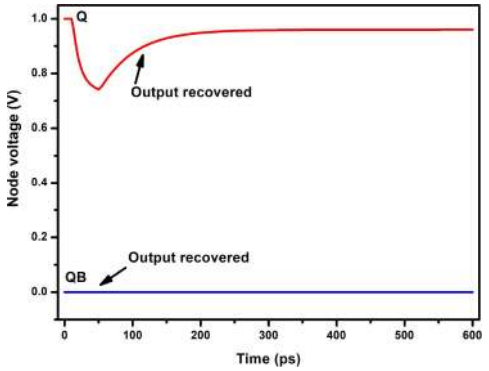

FIGURE 13. Node voltages of radiation hardened 6T TFET SRAM cell.

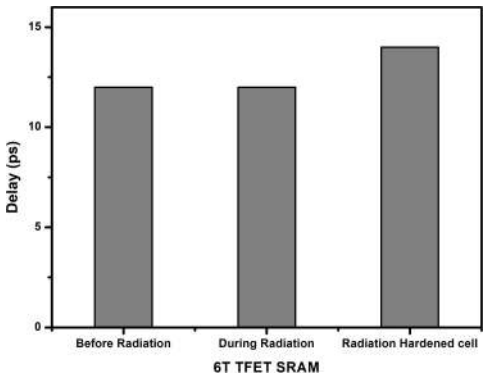

FIGURE 14. Delay of 6T TFET SRAM cell.

TFET SRAM, a layout is needed for the circuit design. Due to unavailability of the compact SPICE model for TFET, the area of the TFET based circuit can be defined by the number of transistors, capacitors and resistors required for the circuit. The 6T TFET SRAM has six transistors, and hence it occupy the least area. Since the radiation hardened 6T TFET SRAM required additional RC feedback loops, the area needed for the circuit will be increased. The delay and standby power of the 6T TFET SRAM cell is calculated and compared as follows:

- Before radiation (i.e., before the current pulse insertion)
- During radiation (i.e., after the current pulse insertion)
- Radiation hardened cell (i.e., after the RHBD technique)

The delay comparison is shown in Fig. 14. It is seen from Fig. 14 that the delay is increased when the RHBD technique is used in 6T TFET SRAM cell due to the additional RC feedback loops. The standby power of 6T TFET SRAM cell is measured by performing the transient analysis, and the procedure to compute power dissipation is explained in the Cadence manual [40]. During the power calculation in standby mode, WL is 0 then the two ATs (M5 and M6) are turned off and the content of the SRAM cell remains unchanged until the supply voltage exist [41].

The comparison of standby power is shown in Fig. 15. It can be referred from Fig. 15 that the standby power of conventional 6T TFET SRAM cell is 5.015 nW. During radiation analysis, the standby power of 4.706 nW is obtained.

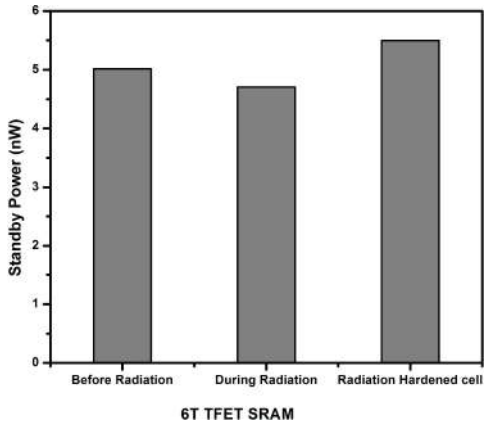

FIGURE 15. Standby power of 6T TFET SRAM cell.

The radiation hardened 6T TFET SRAM cell consumes more power. It is due to the voltage across the capacitor connected between the two cross coupled inverters. The capacitance leakage increases the leakage current exponentially [42]. The voltage across the capacitor results the exponential increase in leakage current.

IV. CONCLUSION

In this paper, the response of the SEU effect on 6T DG TFET SRAM circuit and its mitigation technique are explored. In circuit simulation, the performance of 6T DG TFET SRAM cell is analyzed by injecting the transient current source at the struck node (drain of M2). Due to the heavy ion strike, the data stored at the SRAM cell is changed. The RC feedback components which are connected between the two cross coupled inverters of the SRAM circuit, increases the critical charge and slows down the voltage transients thus recovering the data. The standby power was calculated and compared for the memory cell and it can be observed that there was not much deviation in power consumption after the radiation mitigation technique. Thus it could be concluded that TFET can be used for minimizing SEU effects in SRAM circuits that consume less power.

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