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Linear Peak Current Mode Control of Semi Bridgeless AC-DC Converter

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Abstract

Objectives: The main objective of this work is to obtain input power factor closer to unity and regulation of output voltage of semi bridgeless AC-DC converter using linear peak current mode control. **Methods/Statistical Analysis:** Linear Peak Current Mode control technique is applied to Semi-Bridgeless AC-DC Converter in this paper. This technique helps in achieving power factor closer to unity. The output voltage of the converter is regulated at 200V.The prototype is designed for 200W.Simulation results are obtained for 200W using PSIM software(Simulation Software Package) the converter is analyzed under variable load and supply conditions. **Findings:** At variable load conditions, power factor is maintained closer to unity and output voltage is regulated to 200V. The efficiency for the converter is found to 96% at full load conditions. **Application:** Battery charging applications.

Keywords: AC-DC Converter, Compensating Ramp, Phase Shifting, Peak Current Mode, Semi-Bridgeless

1. Introduction

Generally, switching converters operate in three conduction modes, continuous conduction mode (CCM), discontinuous conduction mode (DCM) and critical conduction mode (CrCM). CCM operation is useful in high power converters because they require high inductance values and sub harmonics oscillations elimination[1]. DCM is advantageous for low power converters. They require low inductance values compared to CCM and sub harmonics do not appear. Up to few hundred watts, these three conduction modes apply. In particular, upto half kilowatt, CCM and CrCM are implemented[2]. Above kilowatt, CCM becomes a better solution. CCM also holds the advantages of lower noise, lower conduction losses. Losses of reverse recovery also show a downfall in CCM. But CCM operated rectifier exhibit greater complexity compared to CrCM and DCM.

In derived converters, change in modes of operation from CCM to DCM, the system changes from second order to first order[3]. CrCM of a switching converter is operated at the boundary between CCM and DCM. Generally, in a CrCM, on-time of the switch is fixed with variable off time. The proposed semi bridgeless converter operates in discontinuous conduction mode as inductor current touches zero between switching cycles.

The converter involves a delay between the pulses provided to the gate terminals of the two switches. Gating voltage to the second switch is 180° phase shifted from the first switch. This phase shifted gating helps in current synthesizing and simultaneously brings out input current shape[4]. In this paper, linear peak current mode (LPCM) control is applied to Semi bridgeless AC-DC converter. Since the converter operates in DCM, the control technique applied also operates in DCM. In LPCM, the peak value of the inductor current is sensed whereas in conventional average current mode control, the average value of inductor current is sensed[5]. The proposed converter is used in battery charging applications since it can afford high efficiency at light loads so that charging time, charging cost, amount and cost of electricity can be minimized[6,7].

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2. Semi Bridgeless PFC Converter

AC-DC conversion requires a rectifier which consists of four diodes, aligned two in parallel. Semi-bridgeless[8] comprises of two slow diodes *Da* and *Db* as shown in Figure 1. These two diodes connect the output to the PFC ground. Their function is to reduce EMI related issues[9]. These diodes do not have continuous conduction of current. Hence, their conduction losses are less. *Q1* and *Q2* are the MOSFET's in the converter as shown in Figure 1. *D*1 and *D*2 are the normal diodes used for forward conduction of current. *Dq1* and *Dq2* are the body diodes of the switches *D*1 and *D*2 respectively. In this converter, most of the current passes through the body diodes of the switches. Hence, for such a topology, switches are to be chosen in such a way that their body diodes withstand higher values of current[10]. Compared to conventional topologies like bridgeless PFC and dual boost topology, this converter avoids the problem of input floating[12]. The gating pulse for switch *Q1* is denoted as *Vg1* and the gating pulse for switch *Q2* is denoted as *Vg2*.

2.1 Modes of Operation

The circuit operation is analysed with four different modes. The modes of operation described apply for converter with duty cycle less than 0.5. The operation of the converter in positive half cycle is presented as follows.

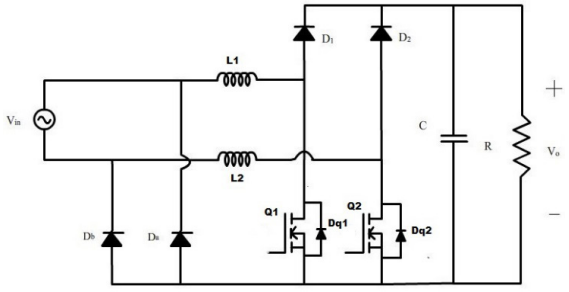


Figure 1. Phase Shifted Semi Bridgeless converter.

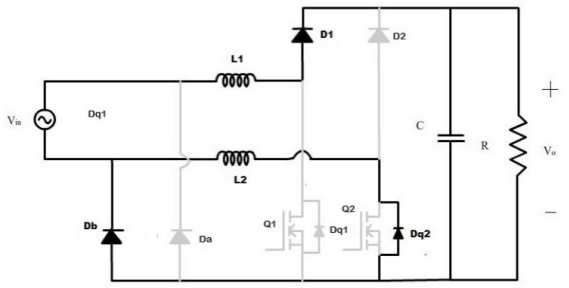


Figure 2(a). Q1 and Q2 OFF, Q2 body diode conducting.

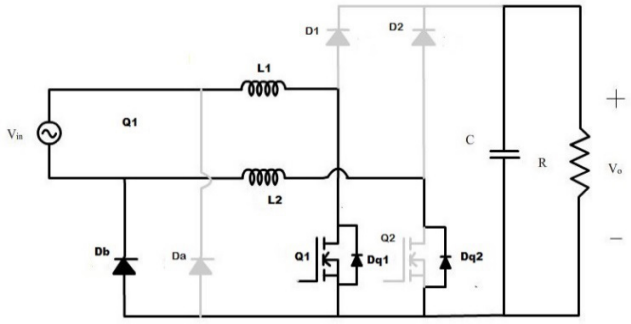


Figure 2(b). Q1 ON, Q2 body diode conducting.

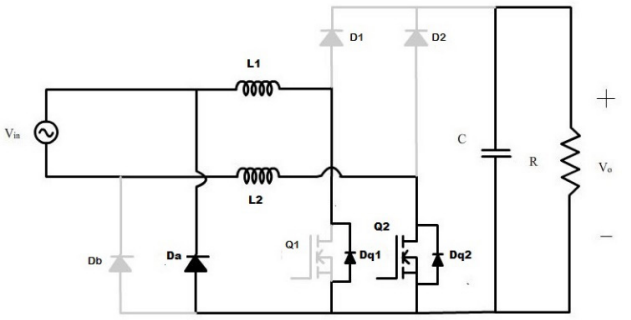


Figure 2(c). Q1OFF, Q2 ON.

Interval 1 [$t0$ - $t1$]:

At time interval $t0$, both the switches $Q1$ and $Q2$ are OFF. In this interval, the energy stored in the intervals $L1$ and $L2$ is sent to output through the path of $L1$, $D1$, $Dq2$, $L2$ and Db as shown in Figure 2(a).

Interval 2 [$t1$ - $t2$]:

At interval $t1$, $Q1$ is ON and $Q2$ is OFF. The currents in the inductors $L1$ and $L2$ increase linearly and energy is stored in the inductors. The voltage across the capacitor C appears across the load. *Db* and *Dq2* shares the return current as shown in Figure 2(b).

Interval 3 [$t2$ - $t3$]:

Interval 1 is repeated here. Both the switches are OFF here. The energy in the inductors is released in the path of $L1$, $D1$, *Dq2*, $L2$ and *Db* as illustrated in Figure 2(a).

Interval 4[$t3$ - $t4$]:

In this interval, $Q1$ is OFF and $Q2$ is ON. The energy in the inductors is released in the path of $L1$, $D1$, $Q2$, *Dq2*, $L2$ and *Db* as shown in Figure 2(c).

The operation of negative half cycle is similar to that of positive half cycle. The theoretical waveforms of the converter are presented in Figure 3.

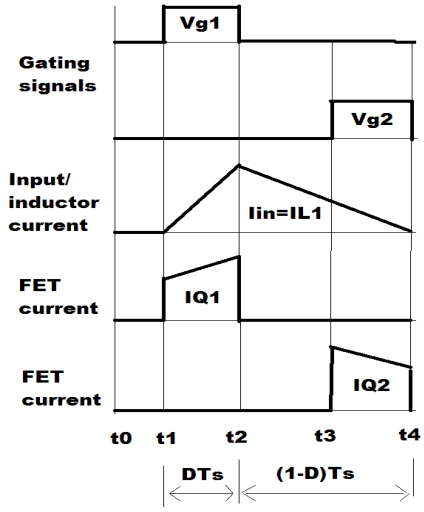


Figure 3. Theoretical waveforms of Semi Bridgeless converter.

2.2 Linear Peak Current Mode Control

Linear peak current mode control is applied to both CCM and DCM operations[12-16]. The operation of LPCM in DCM is illustrated in Figure 4. The aim of this control technique is to modify the shape of input current in phase with input voltage at lower conversion ratios. Three signals considered for analysis are the output voltage feedback signal; the input voltage feed forward signal and the switching current signal. The slope of the compensating ramp helps to achieve power factor correction which depends on both the output voltage feedback signal and the input voltage feed forward signal. Duty cycle is modulated based on the slope variation of the ramp signal. A voltage error signal Ve is obtained from the comparison of output voltage Vo and voltage reference, Vref. This signal is compared with the compensating ramp and the output of comparator is fed to set-reset flip flop. The compensating ramp ensures stability of feedback loop and power factor correction. The compensating ramp also suppresses sub-harmonic oscillations. The compensating ramp is shown in Figure 5. LPCM holds a control law for the modulation of duty cycle.

The proposed control law is derived as follows: Let m_c be slope of the compensating ramp, *Ve* be the voltage of the output error, m_{on}= Vi/L, where L is the inductance of the converter, Vi(t) be the input AC voltage and R is the resistance of the converter. From the analysis, slope of compensating ramp m_c is obtained from the expression,

$$V_e - m_c DT_s = rm_{on}DT_s \quad (1)$$

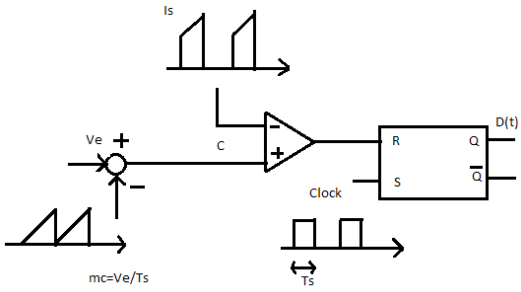


Figure 4. Linear peak current mode controller.

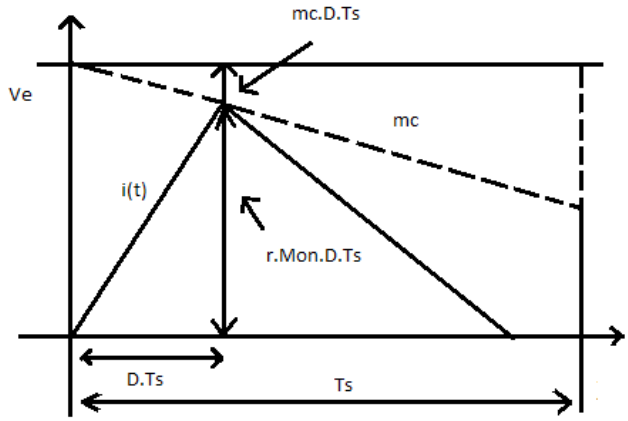


Figure 5. Compensating Ramp in DCM.

Where T_s be the switching period, *r* is gain of current sensor of the switch and on simplifying,

$$mc = \frac{Ve}{DTs} - rmon \quad (2)$$

In terms of conversion ratio M', m_c is written as

$$mc = \frac{F(M')Ve}{DxTs} - rmon \quad (3)$$

where $F(M') = \frac{1}{\sqrt{1-M'(t)}}$ (4)

and $M'(t) = \frac{Vi(t)}{Vo}$ (5)

For a boost converter, the input voltage is always less than output voltage. To satisfy this, M'(t) should be less than 1 in the whole period. In terms of Taylor's expansion and considering first two terms, F(M') is written as

$$F(M') \cong 1 + cM'(t) \quad (6)$$

Here coefficient c is chosen to be good approximation for M' (t)<0.5. c=0.5 is the approximate value.(Refer Figure. 6). In case, if duty cycle is expressed as function of time then,

$$D(t) = D_x\sqrt{1-M'(t)} \tag{7}$$

Where $Dx = \frac{\sqrt{4V0^2 L}}{\sqrt{Vi^2 RTs}}$ (8)

Approximated control law is

$$D_a(t) = \frac{D_x}{1+cM'(t)} \tag{9}$$

Then approximated slope of compensating ramp becomes

$$mca = \frac{Ve}{DxTs} + Vi(t)[\frac{Vec}{DxTs} - \frac{r}{L}] \tag{10}$$

Figure 7 shows the slope of ideal and approximated compensating ramps when Vi(t) varies for different values of Ve, Ve1 and Ve2. This helps in choosing better Ve for design of voltage error amplifier. D is ideal duty cycle whereas Da and m_{ca} are the approximated duty cycle and approximated compensating ramp respectively. Generated voltage signal for compensating ramp implementation is

$$V_{ch}(t) = m_{ca}T_s \tag{11}$$

Under steady state conditions,

$$V_{ch}(t) = K_1V_e + K_2V_i(t) \tag{12}$$

Where constants

$$K_1 = \frac{1}{D_x} \tag{13}$$

$$K_2 = \frac{1}{T_s}[\frac{V_{ec}}{D_xT_sV_0} - \frac{r}{L}] \tag{14}$$

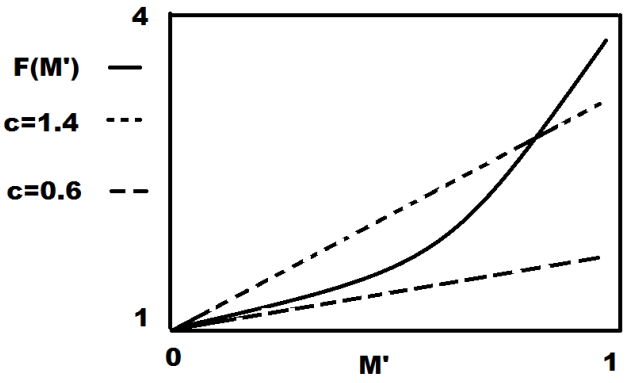


Figure 6. Approximation in the Compensating Ramp.

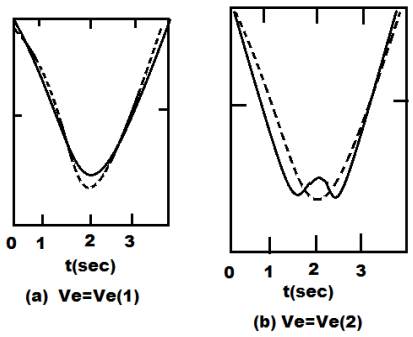


Figure 7. Slope of ideal and approximating compensating ramps.

K2 could be either positive or negative value. But to depict the shape of compensating ramp, it is chosen negative. For the implementation of control law, a basic block diagram is shown in Figure 8. A signal *Ve* is obtained through a low pass filter A(s) to which the output error is provided. Simultaneously from RC circuit, a signal $Vch(t)$ is applied. This signal is obtained by the combination of output error voltage *Ve* and input signal *Vi(t)* . At the two inputs of the op-amp, the error signal and the generated ramp are applied. The signal from the current sensor of the switch and the output of the op-amp are compared to modulate the duty cycle through a Set- Reset flip flop.

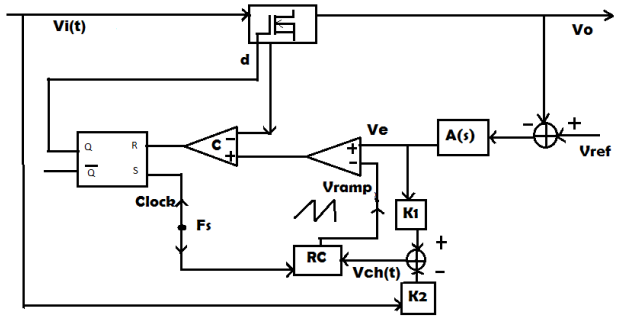


Figure 8. Basic Block Diagram of LPCM.

4. Simulation Results

Simulation for this proposed control technique to the converter is done using PSIM. The converter specifications are shown in Table 1. Figure 9 shows input voltage and input current waveforms for full load condition. It is observed that PF is around 0.96. The value of input voltage and input current are 110V (peak to peak) and 5A (peak to peak) respectively.

Table 1. Converter Specifications

Parameter	Range
Input Voltage (Vin)	110V rms
Output Voltage (Vo)	200V DC
Inductors L1,L2	1.3mH
Output Capacitor, C	470μF
Resistive Load, R	200Ω
Output Power	200W
Switching Frequency, Fsw	70KHz

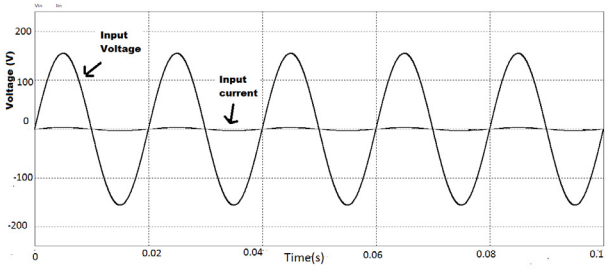
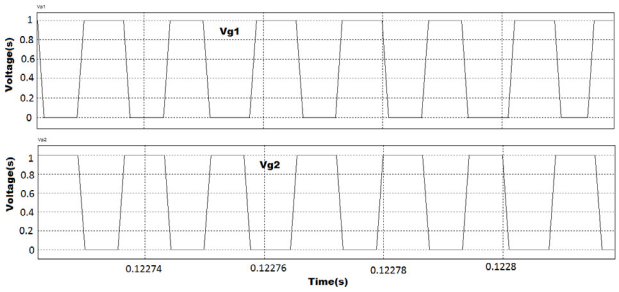
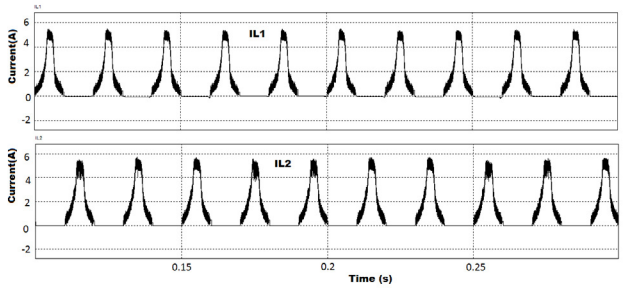


Figure 9. Input current and Input voltage waveforms.



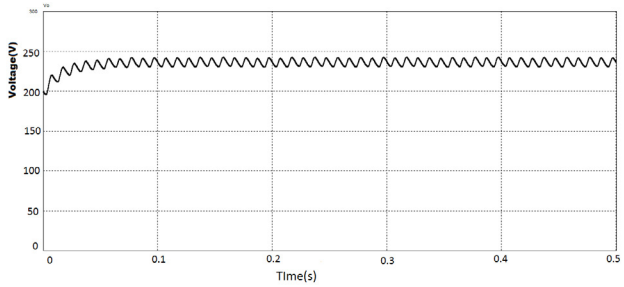
(a)



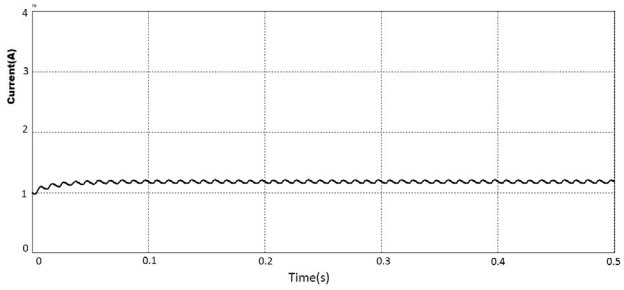
(b)

Figure 10. (a) Gating pulses to switches Q1 and Q2 (b) Inductor currents IL1 and IL2.

The gating pulses obtained from Set-Reset flip-flop is 70KHz.A delay of 7.14μS is provided between the switches to get the required phase shift of 180°. The shift could be viewed in Figure 10(a). The inductor currents has a peak value of around 5A. Figure 10(b) shows the charging and discharging patterns of inductor currents executed as modes of operation in shown in section II. The output voltage has a value of 230V as shown in Figure 11(a). This voltage is observed across a resistor of 200Ω and the output current has a value of around 1A as shown in Figure 11(b).



(a)



(b)

Figure 11. (a) Output Voltage waveform (b) Output current waveform.

The voltage signal shown in Figure 12 is obtained from the integrator to which the inputs are inductor current sensed and error output voltage. The value is around -20V. The efficiency of the converter is observed for variable loads and is plotted as Figure 13. Maximum efficiency obtained at full load is 96%. Compared to average current mode control, LPCM exhibits good efficiency at low loads.

4. Conclusion

Linear peak current mode control for semi bridgeless AC-DC converter for power factor correction and voltage regulation is proposed. From the simulation results, it is inferred that a good power factor is achieved and output voltage is regulated at variable load conditions. With the use of LPCM technique, circuit implementation is sim-

plified and low cost standard PWM controller is utilized. This technique could also be applied to continuous conduction mode for better results.

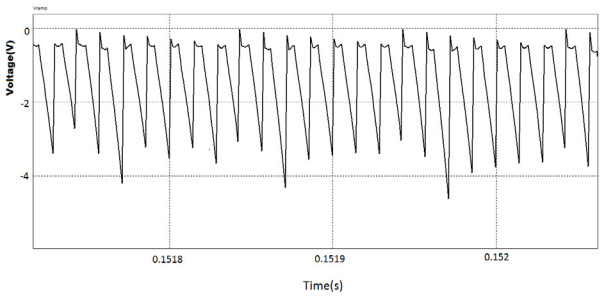


Figure 12. Compensation of ramp.

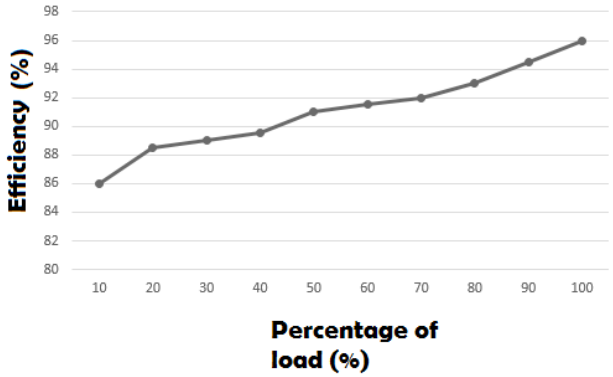


Figure 13. Efficiency Vs Load.

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