

Low Power 64 Point FFT Processor

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Abstract

Objectives: This paper proposes a design of Low power FFT (Fast Fourier Transform) processor used in OFDM (Orthogonal Frequency Division Multiplexing) application as there is demand for low power design of portable communication device. **Methods:** This FFT processor is based on SDF (Single Path Delay Feedback) pipelined Architecture. Digit slicing multiplier less architecture aids in realizing the complex Multiplication. To reduce power dynamic power dissipation, the proposed architecture applies clock gating buffer. Control circuit is implemented using Gray code sequence instead of binary code sequence. The design proposed here is implemented in Verilog HDL. Cadence tool is used for synthesizing the proposed design Findings: The number of complex multiplication is also reduced by using radix -2⁵ algorithms. The result shows reduced power consumption up to 25%. **Improvements:** This paper is presented for 64 Point FFT design; this can also be extended for Higher N point FFT design.

Keywords: Clock Gating, FFT, Multiplier Less Multiplier, Radix 2⁵, SDF

1. Introduction

1.1 overview

FFT is a very important technique in modern DSP and Telecommunication especially for application in OFDM system¹. The first FFT algorithm was proposed by² the complexity to $O(N \log_2 N)$ from $O(N^2)$ of DFT, N denote the FFT size. For hardware design different FFT Processor architecture have been proposed. The main classification is memory based³⁻⁴ and pipeline architecture styles⁵. Memory based FFT processor design known as processor element approach. It consists of single processing element and memory unit, hardware cost is less but have long latency and low throughput. This drawback is overcome in pipeline architecture. The important pipeline types are SDF and MDC (Multipath Delay Commutator). In both the types multiplication complexity is same but the difference is memory size and Hardware utilization rate. SDF⁵⁻⁸ pipeline architecture require less memory size than MDC. Higher radix algorithm⁵ reduce computation complexity. The complex multiplier is realized by using digit slicing concept multiplier less architecture. In order to improve the power efficiency the buffer is designed

with clock gating. Logic Encoding technique is used for counter design in control unit.

1.2 Organization of the Paper

A brief review of Radix 2⁵ FFT algorithm is described in Section 2 and the proposed FFT architecture is presented in Section 3. In Section 4 the implementation and comparison is described. In section 5 the conclusion are summarized.

2. Radix 2⁵ FFT Algorithm

A Discrete Fourier Transform (DFT) of length N is expressed as follows

$$X(k) = \sum_{n=0}^{N-1} x(n)W_N^{nk}, k = 0, 1, \dots, N-1 \quad (1)$$

Where W_N denotes twiddle factor, k and n denotes frequency index and time index respectively.

The radix 2^k algorithm⁵ has the same butterfly structure as radix 2, the only difference is in the number of twiddle factor for each stage. The 64 point FFT computation with

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radix 2⁵ algorithm consists of 6 stages. This algorithm is formulated using 6 dimensional linear index mapping. The radix 2⁵ algorithm expression⁹ is given below.

$$n = \left\langle \frac{N}{2}n_1 + \frac{N}{4}n_2 + \frac{N}{8}n_3 + \frac{N}{16}n_4 + \frac{N}{32}n_5 + n_6 \right\rangle_N$$

$$n_1, n_2, n_3, n_4, n_5 = 0, 1 \quad n_6 = 0, \dots, \frac{N}{32} - 1$$

$$k = \left\langle k_1 + 2k_2 + 4k_3 + 8k_4 + 16k_5 + 32k_6 \right\rangle_N$$

$$k_1, k_2, k_3, k_4, k_5 = 0, 1 \quad k_6 = 0, \dots, \frac{N}{32} - 1$$

$$X(k_1 + 2k_2 + 4k_3 + 8k_4 + 16k_5 + 32k_6)$$

$$= \sum_{n_6=0}^{\frac{N}{32}-1} \sum_{n_5=0}^1 \sum_{n_4=0}^1 \sum_{n_3=0}^1 \sum_{n_2=0}^1 \sum_{n_1=0}^1 \times \left(\frac{N}{2}n_1 + \frac{N}{4}n_2 + \frac{N}{8}n_3 + \frac{N}{16}n_4 + \frac{N}{32}n_5 + n_6 \right) W_N^{nk} \tag{2}$$

The twiddle factor is expressed as follow

$$W_N^{\left(\frac{N}{2}n_1 + \frac{N}{4}n_2 + \frac{N}{8}n_3 + \frac{N}{16}n_4 + \frac{N}{32}n_5 + n_6 \right) (k_1 + 2k_2 + 4k_3 + 8k_4 + 16k_5 + 32k_6)}$$

$$= \underbrace{(-1)^{n_1 k_1}}_{\text{Stage1BU}} \underbrace{(-j)^{n_2 k_1}}_{\text{Stage2BU}} \underbrace{(-1)^{n_2 k_2}}_{\text{Stage2BU}} \underbrace{W_8^{n_3(k_1 + 2k_2)}}_{\text{Stage2TF}}$$

$$\times \underbrace{(-1)^{n_3 k_3}}_{\text{Stage3BU}} \underbrace{W_{16}^{(2n_4 + n_5)(k_1 + 2k_2 + 4k_3)}}_{\text{Stage3TF}} \underbrace{(-1)^{n_4 k_4}}_{\text{Stage4BU}} \underbrace{(-j)^{n_5 k_4}}_{\text{Stage4TF}}$$

$$\times \underbrace{(-1)^{n_5 k_5}}_{\text{Stage5BU}} \underbrace{W_N^{n_6(k_1 + 2k_2 + 4k_3 + 8k_4 + 16k_5)}}_{\text{Stage5TF}} \underbrace{W_N^{n_6 k_6}}_{\text{Stage5TF}} \tag{3}$$

The signal flow graph for 64 point FFT using radix 2⁵ algorithms is shown in Figure 1⁹.

3. The Proposed FFT Architecture

The types of architecture mostly used in FFT processor design are pipeline and memory based architecture. Pipeline based architectures are most popular because they are designed by increasing the performance and regularity of data path. The classification of pipeline is based on the structure of buffer (memory) which is known as SDF and MDC. SDF architecture has less hardware requirement and higher utilization rate than MDC. We proposed SDF pipeline architecture for FFT 64 point. The diagram is shown in Figure 2.

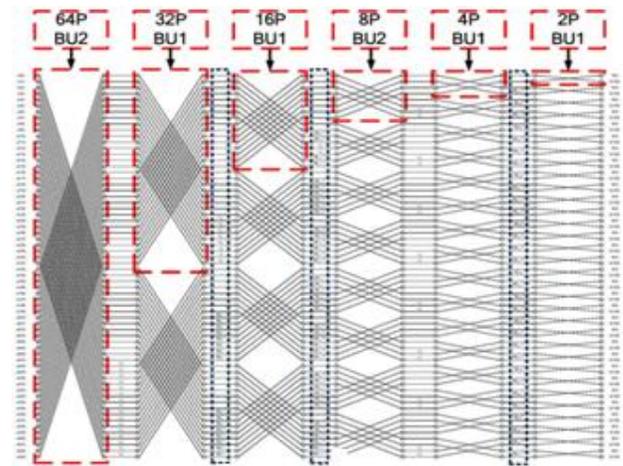


Figure 1. 64 Point Signal Flow graph using Radix 2⁵.

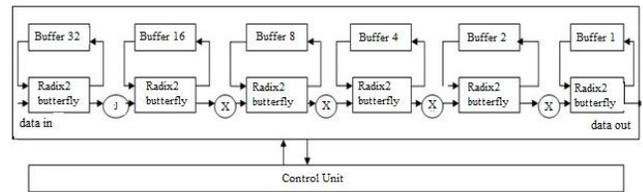


Figure 2. Block diagram of 64 point FFT SDF.

The modules shown in Figure 2 are buffer of various size implemented by First In First Out (FIFO) for Time multiplexing, Complex multiplier, Radix-2 Butterfly unit and Control unit. FIFO functions as shift register, it receives data from butterfly module and feedback again to butterfly unit. The radix-2 butterfly operation is shown in Figure 3.

3.1 Complex Multiplier

In FFT, complex multiplication is one of the operations which is considered for performance analysis. One of the complex multiplications with three multiplier is given by Expression (4) and shown in Figure 4. Various complex multipliers have been proposed¹⁰ earlier.

$$(a_r + ja_i)^*(b_r + jb_i) = \{b_r(a_r - a_i) + a_i(b_r - b_i)\} + j\{b_i(a_r + a_i) + a_i(b_r - b_i)\} \tag{4}$$

3.1.1 Digit Slicing Multiplier

The digit slicing based multiplier aids in reducing the computation complexity. The binary number can be sliced into binary numbers of shorter length. This concept is applied for designing digit slicing multiplier. The basic is represented by following Expression¹¹ (5) and (6).

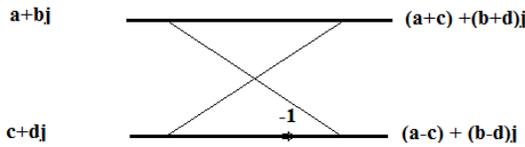


Figure 3. Radix-2 butterfly.

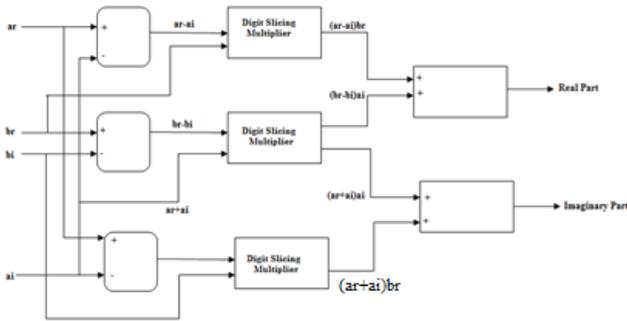


Figure 4. Complex multiplication.

$$F = F_R + jF_I$$

$$F = \sum_{k=0}^{b-1} (2^{p-1})F_{Rk} + j \sum_{k=0}^{b-1} (2^{p-1})F_{Ik} \tag{5}$$

Where $F_{Rk} = \sum_{j=0}^{p-1} 2^j F_{Rkj}$ and $F_{Ik} = \sum_{j=0}^{p-1} 2^j F_{Ikj}$

In this equation F_{Rk} and F_{Ik} have values which are either zero or one. Any value whose absolute value is less than one can be represented in two's complement as

$$x = \left[\sum_{k=0}^{b-1} 2^{pk} X_k \right] 2^{-1(pb-1)} \tag{6}$$

Here x is any number with an absolute value less than one and x is sliced into b blocks, each block being p bits wide.

$$X_k = \sum_{j=0}^{p-1} 2^j X_{k,j}$$

For example $X = A*B$ In this multiplication one of the operand (A) divided into four parts as shown in Figure 5 A divided into four parts Such as

- part 1 = $A_3A_2A_1A_0$
- part 2 = $A_7A_6A_5A_4$
- part 3 = $A_{11}A_{10}A_9A_8$
- part 4 = $A_{15}A_{14}A_{13}A_{12}$

There are four different cases for the multiplication between the four bits and the twiddle factors. Figure 6 shows the block diagram of the digit-slicing multiplier less using the shift and addition technique. Shift-and-add multiplication is similar to the multiplication performed by paper and pencil.

$$K_0 = (A_3A_2A_1A_0)*B,$$

$$K_1 = (A_7A_6A_5A_4)*B,$$

$$K_2 = (A_{11}A_{10}A_9A_8)*B,$$

$$K_3 = (A_{15}A_{14}A_{13}A_{12})*B$$

$$X = A*B = K_0 + 2^4K_1 + 2^8K_2 + 2^{12}K_3$$

3.2 Clock Gating

There are two components of power in digital circuit they are dynamic power and static power

$$\text{Dynamic Power} = \alpha f_{CLK} C V^2 \tag{7}$$

Where α represent the switching activity of a circuit, f_{CLK} is the frequency of the clock, V is the supply voltage and C is capacitance. The device static power represents the transistor leakage power when the device is powered. The clock signal has been a notorious source of power dissipation because of high frequency. It does not perform useful computation but serves the purpose of synchronization. Clock is the most popular method for power reduction. Clock gating¹² saves power by reducing unnecessary clock activity inside the gate module due to that dynamic power dissipation is reduced. In FFT the buffer is involved in more switching activity. Below diagram shows the buffer with clock gating.

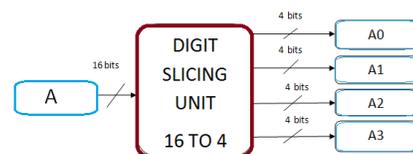


Figure 5. Digit slice.

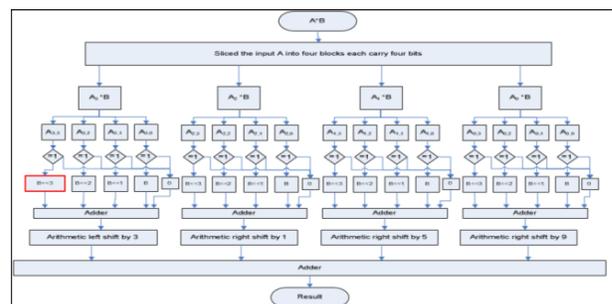


Figure 6. Complex multiplication using digit slicing.

3.4 Gray Counter Design

The Logic level power optimization technique is the reduction of switching activity. The total number of transition¹² of a binary counter is

$$B_n = 2(2^n - 1) \tag{8}$$

The total number for a gray code counter is

$$G_n = 2^n \tag{9}$$

The power dissipation is based on switching activity i.e., number of transition. A gray code counter is more efficient than a binary counter for designing a control circuit. The proposed 64 point FFT SDF architecture requires 5 bit counter for control circuit. It is designed using Gray code sequence counter. The Table 1 shows the number of transition based on Equation (8) and (9)

4. Results and Comparisons

The architecture of the proposed FFT processor was designed in Verilog and simulated to verify its functionality. The simulation and synthesis were performed using the cadence design tool 180 nm CMOS Technology.

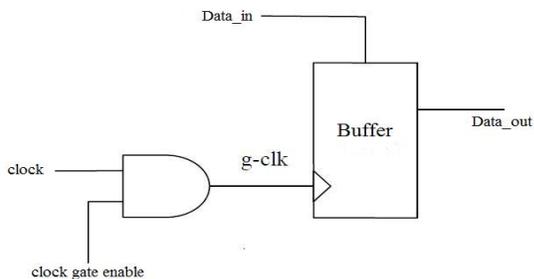


Figure 7. Clock gating buffer.

Table 1. Number of transition comparison

Number of Bit	Number of Transition for binary	Number of Transition for Gray
5	62	32

Table 2. Comparisons of FFT processor

	Word length	Power (mW)	Frequency (MHz)	Area (No. slice used)
FFT(using without clock gating buffer and binary sequence counter)	16	39.329	166.6	13512
Proposed	16	29.348	166.6	13350

Table 2 shows the performance comparison between the proposed 64 point FFT and normal FFT processor .The proposed FFT Processor design is based on algorithm radix 2⁵, digit slice based multiplier less multiplier for multiplication, with clock gated buffer and gray counter sequence for control circuit.

The results shows power consumption of proposed FFT processor is 29.3 mw at 166 MHz. This is around 25 % lesser when compared with the power consumption of normal FFT processor design but with 2% increase in area.

Generated by: Encounter(R) RTL Compiler v11.20-s017_1				
Generated on: Sep 24 2015 04:55:45 pm				
Module: top_ver1_net_count_single1_cg				
Technology: tsmc18 1.0				
library:				
Operating conditions: slow (balanced_tree)				
Wireload mode: enclosed				
Area mode: timing library				
Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
top_ver1_net_count_single1_cg	13350	15111.048	29333223.933	29348334.981
Generated by: Encounter(R) RTL Compiler v11.20-s017_1				
Generated on: Sep 16 2015 03:33:30 pm				
Module: top_ver1_net_gray_single1				
Technology: tsmc18 1.0				
library:				
Operating conditions: slow (balanced_tree)				
Wireload mode: enclosed				
Area mode: timing library				
Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
top_ver1_net_gray_single1	13512	15504.540	39314365.425	39329869.965

5. Conclusion

In this paper, radix 2⁵ algorithm, digit slice based multiplier for complex multiplication, with Clock gated buffer, gray counter sequence for control circuit used for designing of low power 64 point FFT processor. The result shows that the design using, with clock gated buffer and gray counter sequence for control circuit lowers power consumption by 25% than the design without clock gated buffer and normal binary counter sequence. Our proposed FFT

processor design can be used to reconfigurable FFT processor of various OFDM based application for low power consumption.

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7. References

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