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Research paper

Low power combinational and sequential logic circuits using clocked differential cascode adiabatic logic (CDCAL)

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Abstract

This paper presents the Clocked Differential Cascode Adiabatic Logic (CDCAL), the quasi-adiabatic dynamic logic that can operate efficiently at GHz-class frequencies. It is operated by two phase sinusoidal power clock signal for the adiabatic pipeline. The proposed logic uses clocked control transistor in addition to the less complex differential cascode logic structure to achieve low power and high speed operation. To show the feasibility of implementation of both combinational and sequential logic circuits using the proposed logic, the CLA adder and counter have been selected. To evaluate the energy efficiency of the proposed logic, an 8-bit pipelined carry look-ahead (CLA) adder is designed using CCDAL and it is also compared against the other high speed two phase counterpart available in the literature and conventional static CMOS. The simulation results show that the CCDAL logic can operate efficiently at high frequencies compared to other two phase adiabatic logic circuits. All the circuits have been designed using UMC 90nm technology library and the simulations are carried out using industry standard Cadence® Virtuoso tool.

Keywords: *Low Power; Quasi-Adiabatic Logic; Two Phase Clocked Charge Recovery Circuit; Low Power Adder.*

1. Introduction

In recent years, the semiconductor industry has moved towards the deep submicron process technology and the transistors count of digital Integrated Circuits (ICs) have become huge. Due to the increased number of transistors per chip with increased frequency of operation, the power consumption of a chip increases dramatically for every technology generation. This motivates the design engineers of VLSI industry to work on various non-conventional design methodologies to achieve low power in static CMOS circuits. There are several methods, including pipelining and subsequent supply voltage scaling to reduce the dynamic power dissipation at a particular switching frequency. However, the delay and energy overhead due to the pipeline registers is significant and affects the overall system efficiency.

Charge recovery circuitry using the adiabatic principle is proved to be one of the most promising approaches to reduce the power dissipation of CMOS based digital circuits. Several charge recovery logic styles [1], [2] that uses multi-phase clocking schemes have been reported in the literature. In these multiphase designs, the multiple clock signal generation and synchronization among these clock signals are considerable and also they are sensitive to the clock skew. To improve the energy efficiency and also to simplify the clocking design, the sinusoidal clocked single phase and two phase adiabatic circuits [3] [4] have been proposed. A number of two phase clocked quasi adiabatic circuits [4] consisting of 2p or 2n2p latch operate efficiently for relatively lower operating frequencies of the order of few hundred megahertz. Conversely, the fundamentally static CMOS structured and control transistor based two phase clocked adiabatic circuits [5]-[7] have been demonstrated. These logic styles have single rail output that uses diode based control transistor for its adiabatic operation. Hence, they are suitable only for the low speed designs. A new class of charge recovery circuits [8] [9] based on subthreshold operation have also been reported for the high speed operation. However, they need additional dc power supply sources in addition to the power clock and they also need additional transistors for its adiabatic operation.

This paper introduces Clocked Differential Cascode Adiabatic Logic (CDCAL) operated by two complementary sinusoidal power clock signals. CDCAL uses clocked control transistor for charging and discharging the output node adiabatically, which is explained in section 2. The energetics of the CDCAL inverter/buffer is also explained in section 2. The design of adiabatic sequential circuits using CDCAL is discussed in section 3. The design of CLA adder using CDCAL and the simulation results and the comparison of the proposed design and its energy efficiency against the other two phase counterpart are presented in section 4. Conclusions are given in section 5.

2. Clocked differential cascode adiabatic logic (CDCAL)

The structure and operation of CDCAL, energetics of CCDAL inverter/buffer are discussed in this section.

2.1. Structure and operation of CDCAL

Fig. 1(a) shows the structure of CDCAL inverter/buffer. It uses two complementary sinusoidal signals as power supply source, also called as power clock signals PC and PCBAR. It has dual rail output and operates in two phases, namely, evaluate and hold. The basic buffer/inverter has the nMOS transistors (MN1 and MN2) in

the pull-down (PDN) path and the control transistor MN3. By replacing the transistor MN1 and MN2, the desired logic function can be realized with the complementary function tree. The pull down path is connected to the PCBAR for discharging the output during evaluation phase. The PMOS latch using MP1 and MP2 is connected in the pull-up network (PUN) along with the control transistor MP3. The PUN is connected to the PC for charging the output during the evaluation phase of the power clock signal.

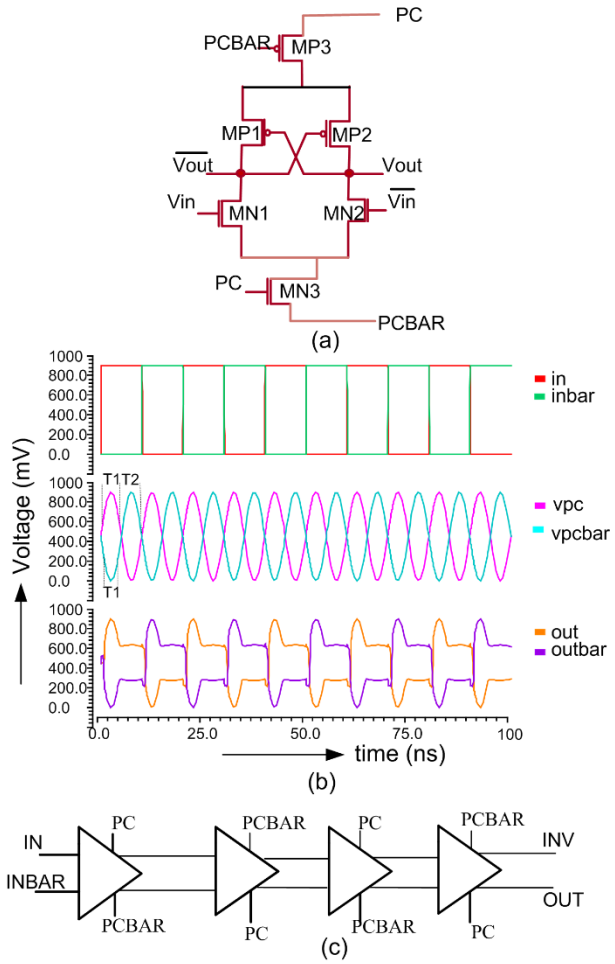

Fig. 1: A) CDCAL Inverter/Buffer, B) Signal Transients and C) Buffer Chain.

To understand the operation of the CDCAL inverter/buffer, consider Fig. 1(b). During the evaluation phase (T1), PC is in the upper half of the clock cycle and PCBAR is in the lower half of the clock cycle and vice versa for the hold phase (T2). During T1, the complementary inputs in is logic 1 and inbar is logic 0 as shown in Fig. 1(b) and the function transistor MN1 is on. The output voltage V_{out} follows the power clock PCBAR for its lower half of the power clock cycle as the control transistor MN3 is on only for the lower half of the power clock cycle. While the V_{outbar} discharges towards the PCBAR, the transistor MP2 is on and V_{out} starts following the power clock PC. The output voltage follows the power clock PC only for its upper half of the clock cycle as the control transistor MP3 is on only for the upper half. During hold phase (T2), both the control transistors MN3 and MP3 are off and the outputs remain the same. It is seen that the complementary outputs V_{out} and V_{outbar} do not follow the power clock for its complete cycle and the voltage swing at the output terminals are reduced. Hence, the switching power is reduced that improves the energy efficiency of the CDCAL. In this multistage adiabatic pipeline practical system, the next stage performs evaluation while the first stage is in the hold phase. Pipelining of the multistage gates is done by powering the alternative stages using PC and PCBAR as shown in Fig. 1(c).

2.2. Energetics of CDCAL

The energy spent by the CDCAL inverter/buffer is due to the following components:

- The proposed inverter charges the output node through MP3 and the stored charge is recovered or discharged to the power supply through MN3. The voltage swing at the output node is $(V_{dd}-V_c)/2$ and the energy spent during the adiabatic charging/ discharging operation is given by the equation

$$E_{adiab} = \frac{RC}{T} C\left(\frac{V_{dd} - V_c}{2}\right)^2$$

  Where R is the channel resistance of the pull up/pull down path, C is the output nodal capacitance, T is the time period of the power clock, V_{dd} is the peak power clock voltage and V_c is closer to threshold voltage of current control transistor. It is observed that the output voltage during charging or discharging is reduced approximately to $V_{dd}/2$ which minimizes the switching power.
- The non-adiabatic energy loss is caused by the threshold voltage. During the output transition, the transistors will not conduct immediately until the voltage difference between the gate to source is equal to threshold voltage (Vt) and the corresponding energy loss is 1/2 CVt2.
- The third component is energy loss due to the crowbar current. Crowbar current is the short circuit current during evaluation phase of the adiabatic operation. During evaluation phase both the control transistors (MP3 and MN3) are on and there are straight paths between the power rails when the input is switching. It is also noted that the energy loss due to the crowbar current is significant at lower range of frequencies.

Therefore, the total energy spent by the inverter/buffer per cycle is as given by

$$E_{Total} = \frac{RC}{2T} C(V_{dd} - V_c)^2 + CV_t^2 + E_{crowbar}$$

The energy equation shows that the adiabatic energy loss depends upon the switching frequency and it is also noted that the energy dissipation is less for lower range of power clock frequencies. However, CDCAL inverter suffers from the drawback of floating nodal output. During the hold phase of the sinusoidal power-clock, both the control transistors become off and the complementary outputs are disconnected from both the power-clocks PC and PCBAR. Thus, the circuit becomes susceptible to noise due to charge leakage and charge sharing. This may lead to the problem of incorrect operations for the complex digital logic circuits realized using CDCAL. The CDCAL inverter with modified control transistor connection is shown in Fig. 2. It gives improved performance due to the larger gate overdrive voltage of the control transistor. The proposed connection also reduces the effective resistance of the control transistors in the pull-up and pull-down path.

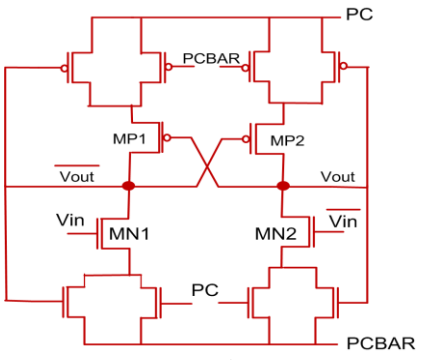

Fig. 2: CDCAL with Modified Control Transistor.

3. Sequential circuits using CDCAL

To show the implementation of a sequential circuit, the design of flip-flops and the 4-bit counter are discussed in this section. All the previously reported sense amplifier based adiabatic logic circuits [1], [2] incur issues related to signal storage in the register. In the sense amplifier based sequential circuit designs, the complementary outputs follow the power clock during the evaluation phase and the register becomes '0', when the supply clock ramps down to '0'. The proposed flip-flop uses control transistor, which does not discharge the output to '0' during evaluation phase and thus they eliminate the problem of signal storage.

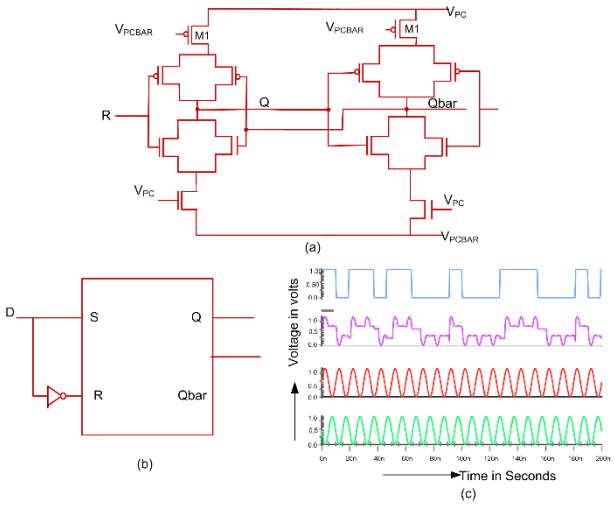

Fig. 3: A) SR Flip-Flop. B) D Flip-Flop. C) I/O Waveforms of D Flip-Flop.

The design of a SR and D flip-flop [7] using the proposed CDCAL is shown in Figs. 3(a) and (b). The transistor schematic of SR flip-flop has two inputs S, R and a common clock signal. Here, the power clock PC can be used as a clock signal. The D flip-flop can be realized by using SR flip-flop as shown in Fig. 3(b). The simulation results of D flip-flop are shown in Fig. 3(c). The result shows that the output follows D during the upper half of the clock cycle while the output remains the same during the lower half of the power clock.

The transistor schematic of the T flip-flop [7] is shown in Fig. 4. The logic equation is derived from its gate level design as given by,

$$Q_{n+1} = T\overline{Q_n} + \overline{T}Q_n$$

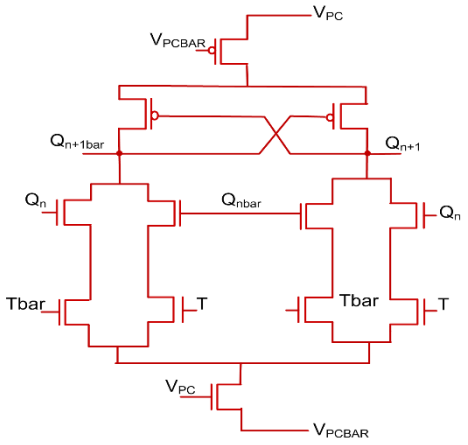

Fig. 4: T-Flip-flop.

The 4-bit counter is realized by cascading four T-flip-flops as shown in Fig. 5(a). All the four flip-flops are active and increments to a new state during evaluation phase. The inputs to the flip-flops are computed and kept ready during hold phase. Thus, it is shown that the counter has no latency and it is incrementing from 0 to 15 for every power clock cycle during the evaluation phase. The simulation results of the 4-bit counter are shown in Fig. 5(b). The energy is measured for different power clock frequencies and it is able to operate upto the frequency of 1GHz. The result shows that the energy consumption of 4-bit CDCAL based counter is 46 fJ and 61fJ at 400 MHz and 1GHz, respectively.

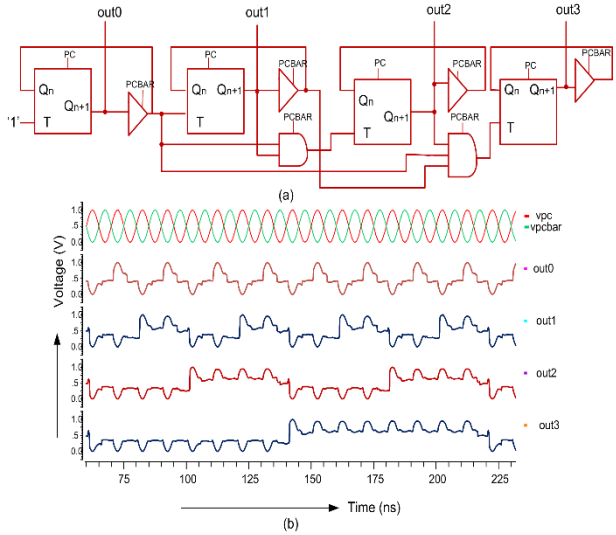

Fig. 5: A) 4-Bit Counter, B) Output Waveforms of 4-Bit Counter.

4. CLA adder using CDCAL

The pipelined 8-bit CLA adder has been designed using CDCAL. The adiabatic CLA adder uses two complementary two phase sinusoidal power clock signals [6] as power supply. Fig. 6 shows the architecture of pipelined 8-bit adiabatic CLA adder. It uses propagate generate (PG), CLA (carry look-ahead) and Sum generation module blocks. The function of the PG is as given by

$$G_i = A_i \bullet B_i$$

$$P_i = A_i \oplus B_i$$

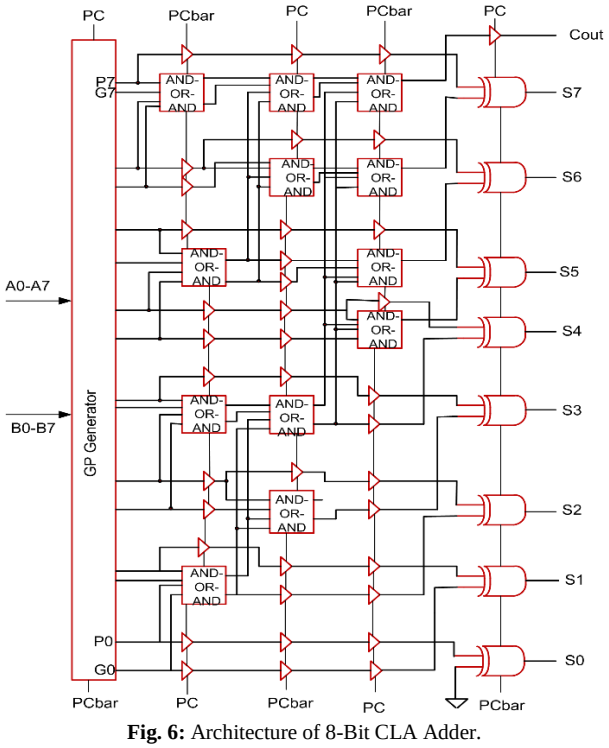

Fig. 6: Architecture of 8-Bit CLA Adder.

The sum S_i and carry C_i output functions of each stage of the 8-bit CLA adder as represented by

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + P_i \bullet C_i$$

The adiabatic adder is realized by instantiating all the adiabatic library cells and then the netlist is generated for the schematics. The output is evaluated for the 8-bit CLA adder using random vector inputs. The adder realized using CDCAL has a latency of 5 and it takes 2.5 clock cycles to compute the output.

The energy efficiency of the CDCAL is analyzed by using a CLA adder as a benchmark circuit. Although there are a variety of quasi adiabatic adders [10], [7] available in the literature, their implementation needs vast design methodologies and they have limited range of frequency operation. Hence, high speed adiabatic logic, namely, boost logic and fully pipelined static CMOS adders are realized for justifiable comparison. The 8-bit static CMOS adder is designed using four stage pipelining to operate at high switching frequencies. The D-latches are used as the state elements.

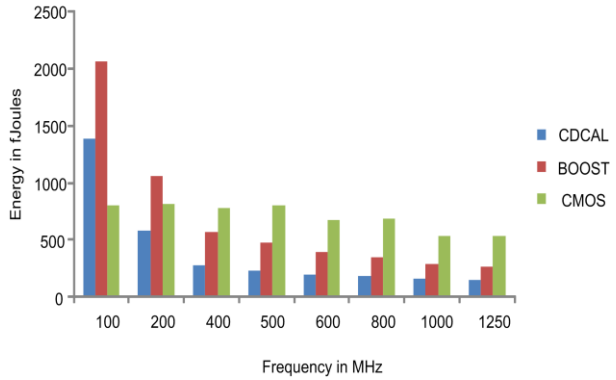

Fig. 7: Power Consumption of CDCAL against Boost Logic and Static CMOS.

Fig. 7 shows the power consumption comparison of 8-bit pipelined CLA adder using CDCAL, boost logic and static CMOS logic. The simulation results show that the CDCAL adder is energy efficient compared to the static CMOS adder over the frequency range of 200 MHz to 1000MHz. It is noted that the sizing of pull up transistor with respect to pull-down functional transistor plays an important role in the functionality of adder. The result proves that the CDCAL has an adiabatic gain of 1.2 to 3 and the energy savings of 28 to 73% over the frequency range of 200 to 1000 MHz against the static CMOS adder. It is also seen that the energy consumption of boost logic adder is two-fold more than that of the CDCAL adder as shown in Fig. 6. The adder circuits realized using CDCAL functions correctly even beyond the frequency of 1GHz.

5. Conclusion

In this paper, a two phase clocked novel charge recovery logic called Clocked Differential Cascode Adiabatic Logic (CDCAL) is presented. The performance evaluation of CDCAL is made through design of both the combinational and sequential logic circuits. The realization of flip-flop using proposed logic demonstrates the possibility of charge recovery in memory circuits. The counter realized using CDCAL is able to work upto the clock frequency of 1GHz and it consumes energy of 61 fJ at 1 GHz. The energy efficiency of the CDCAL adder is evaluated by comparing the power dissipation with the static CMOS counterpart. Simulation results show that there is an energy savings of 73% over static CMOS adder and 50% over boost logic.

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