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Multi-Level DC-DC Converter for High Gain Applications

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ABSTRACT

The output voltage from most renewable energy sources like photovoltaic arrays and fuel cells will be at low level. This must be stepped up considerably for practical utilization or grid connection. The presented multilevel boost converter DC-DC converter topology consists of the conventional boost converter and voltage doubler stages to provide high voltage gain. The proposed topology uses only one switch along with one inductor, (2N-1) diodes and (2N-1) capacitors for obtaining an output which is N times the conventional boost converter. In this topology, each device blocks only one voltage level. The main advantages of this topology are continuous input current, large gain without high duty cycle or transformer, modularity and use of devices with low voltage ratings. Experimental results obtained from the 100W prototype demonstrate the voltage gain capability of the converter and validates the converter design.

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1. INTRODUCTION

The demands of step-up power conversion are continually increasing in applications like automobiles and renewable energy systems. In most renewable energy systems like solar and fuel cell, the voltage obtained is very low and has to be significantly stepped up for meaningful utilization. Conventionally, interleaved and cascaded boost converters were used to obtain the required high voltage gain [1]-[4]. Though cascading of boost converters achieved the required gain, it resulted in incremental cost and complexity of the control circuit. Further, these topologies have inherent problems of high ripple current and relatively higher losses which restrict operation at high efficiency and high gain.

Isolated topologies use transformers or coupled inductors with required turns ratio to achieve the required voltage gain [5]-[8]. High turns ratio is not preferred due to high leakage at the secondary which cause increased switching losses at the output. These topologies suffer from limited switching frequency, increased transformer losses, increased voltage stress across the device and are bulky.

Converters that operate without a transformer but are still suitable for grid connection are necessary for improving system efficiency. In [9] and [10], coupled inductors and switched capacitors were used to obtain the required high conversion ratio. These topologies provided the required voltage gain by using more components and complex magnetic elements. Due to these reasons, such converters are not widely used in practice.

The topologies proposed in [11]-[13] achieved the required gain by employing voltage multiplier cells (VMCs) and coupled inductors with VMCs. The switch stress in these topologies was close to half of the output voltage. In [14] a soft switched multi-output converter using a magnetic amplifier is presented. To reduce the device stresses, switched inductor and switched capacitor based topologies were proposed in [15]. However, the use of switched inductor and switched capacitor structure resulted in relatively reduced efficiency.

In [16], the output diodes were soft-switched to increase efficiency. The idea of non-isolated multi-level DC-DC power conversion is an attractive alternative solution to obtain the required high voltage gain and high power level [17]-[19]. Devices with lower voltage rating are sufficient to obtain multi-level converters because each stage experiences only a certain fixed and equal voltage stress which is considerably lower than the output voltage. As the voltage stress across the switch is lower, devices with low on-state resistance (RDS-ON) can be used to reduce the conduction losses and achieve improved efficiency. Further, the low voltage blocking capability requirement of the diodes permits use of Schottky rectifier diodes and reduces the reverse recovery problems.

In this paper, a DC-DC multi-level boost converter (MBC) which consists of a conventional boost converter with several voltage multiplier stages is presented. The number of levels can be increased by adding two capacitors and two diodes per extra level, thereby making it convenient for modular implementation. The detailed operating principle along with the design details and hardware results are presented in the subsequent sections.

2. CIRCUIT DESCRIPTION

2.1. Power Circuit Diagram

The power circuit diagram of the 5-level multi-level boost converter is shown in Figure 1. Switch S, inductor L, diode D1 and C1 form the conventional boost converter stage. The output from the capacitor C1 is considered as first level and is denoted as Vc. Diodes D2, D3 and capacitors C2, C3 form the first VMC stage or the second output voltage level 2Vc. Proceeding in a similar manner, it can be observed that diodes D4-D9 and C4-C9 form the remaining VMC stages. The corresponding output voltage levels are obtained across capacitors C5, C7 and C9. In general, for an N-level converter, appropriate numbers of the diode-capacitor combinations have to be used.

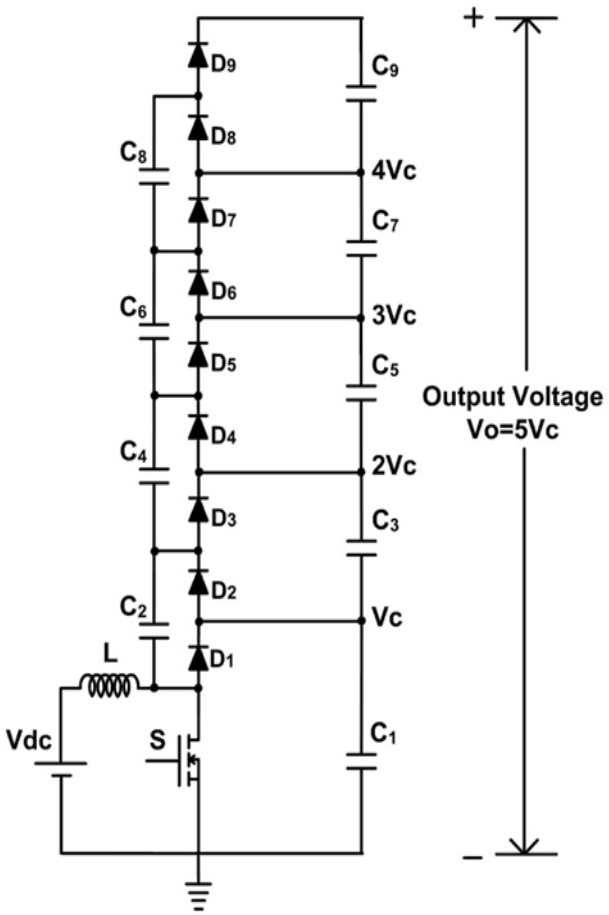

Figure 1. Power Circuit Diagram

2.2. Modes of Operation

The circuit has two main modes of operation; when S is ON and when S is OFF. The working of the circuit in the two modes is described below. During the ON state of switch S, the inductor L charges to the voltage level dictated by Vdc. If the voltage across the capacitor C2 is less than the voltage across C1, then the voltage across C1 is clamped across C2 through the diode D2. Simultaneously, the sum of the voltages across C2 and C4 is less than the sum of the voltages across C1 and C3 so the voltages across C1 and C3 are clamped across the capacitors C2 and C4 through D4. Similarly, the voltages across C1, C3, C5 and C9 are clamped across the capacitors C2, C4, C6 and C8. Figure 2 describes the circuit operation when the switch is turned on.

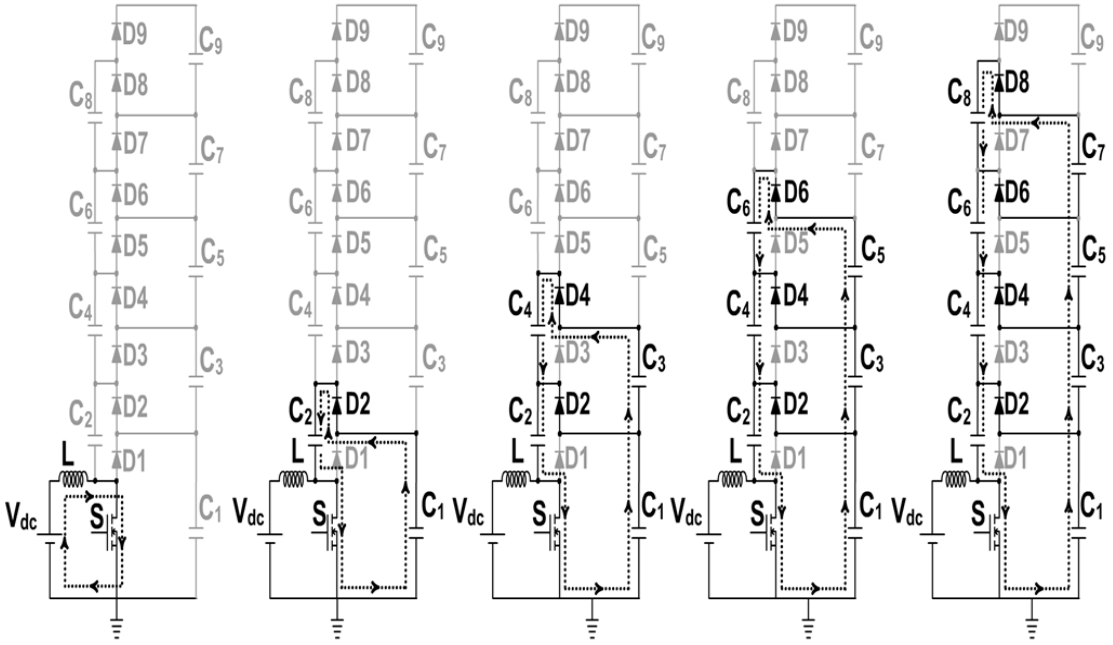

Figure 2. Mode 1. Power Circuit when switch is ON.

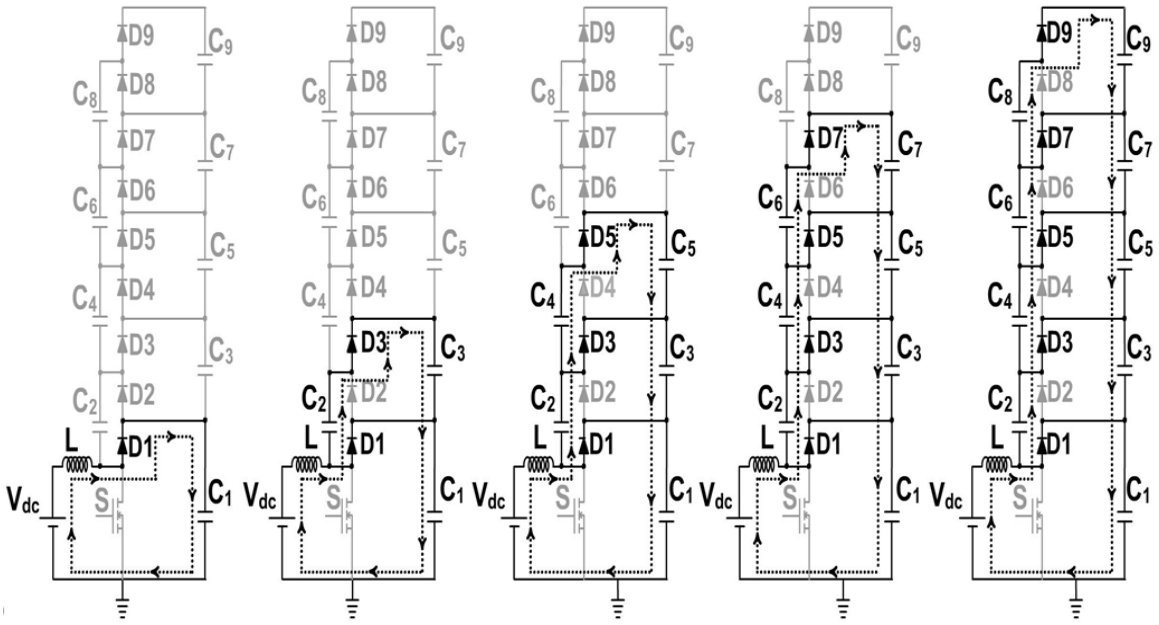

Figure 3. Mode 2. Power Circuit when switch is OFF.

During the OFF state of the switch S, the combined voltage across the inductor and the source Vdc forward biases D1 and switches all the other diodes. In this state, the inductor current charges C1 through D1. Simultaneously voltage in the inductor, voltage across C2 and the voltage Vdc clamp the voltage across capacitors C1 and C3 through D3. Similarly, the induced voltage in L, Vdc and the voltage across C2 and C4 clamp across capacitors C1, C3. Similarly, the voltage Vdc, the voltage across the inductor L and the voltages across C2, C4, C6 and C8 clamp across C1, C3, C5, C7 and C9. It is observed that the diodes D2, D4, D6, and D8 are complementary to didoes D1, D3, D5, D7 and D9. Figure 3 shows the power circuit diagram when switch S is turned OFF.

3. DESIGN DETAILS

In the proposed converter, the design of the elements used is similar to the conventional boost converter. The voltage gain of a conventional boost converter is,

$$\text{Voltage Gain M} = \frac{1}{1-D} \tag{1}$$

where D is the duty ratio of the switch.

For an N-level multilevel boost converter, the voltage gain is given by,

$$\text{Voltage gain M} = \frac{N}{1-D} \tag{2}$$

The design specifications are, input voltage V_{dc} = 24V, output voltage V_o = 240V, output power P_o = 100W and switching frequency f = 50 kHz. Figure 4 shows the voltage gain plot which can be used to determine the combination of duty cycle and number of levels required to achieve a voltage gain of 10. It is observed that converters with lower levels (N=2, 3) need to be operated at very high duty ratios to achieve the required voltage gain. This is practically difficult and results in higher voltage stresses and reduced efficiency. Hence, the number of levels is increased to 5.

A duty cycle of 0.5 with 5 levels provides sufficient turn off time for the power device and avoids excessive voltage stress. Based on the duty cycle and output power, the critical value of the inductance L_{crit} is given by,

$$L_{crit} = \frac{D \times (1-D) \times R}{2 \times f} \tag{3}$$

The main switch S is present closer to the input and before the multiple conversion stages. As a result, the switch S will experience a voltage stress similar to a conventional boost converter only. The voltage stress is given by the expression,

$$\text{Switch voltage stress } V_{S,\,DS} = \frac{V_{dc}}{1-D} \tag{4}$$

The maximum voltage blocked by each diode is equal. Diodes in each level will experience a voltage stress corresponding to that particular level. As the voltage obtained at each level is equal to that of a conventional boost converter the diode voltage stress is expressed as

$$\text{Diode voltage stress } V_{Diode} = \frac{V_{dc}}{1-D} \tag{5}$$

All the diodes present in the converter will contribute to some potential drop due to the forward voltage drop (VD) across them. The number of diodes and their accumulated potential drops till a particular voltage level determines the actual potential at each level. Therefore, the potential at the k^{th} stage is determined by,

$$\text{Potential at } k^{th} \text{ stage kVc} = \frac{V_{dc}}{1-D} - nV_D \tag{6}$$

where n is the total number of diodes encountered till k^{th} stage.

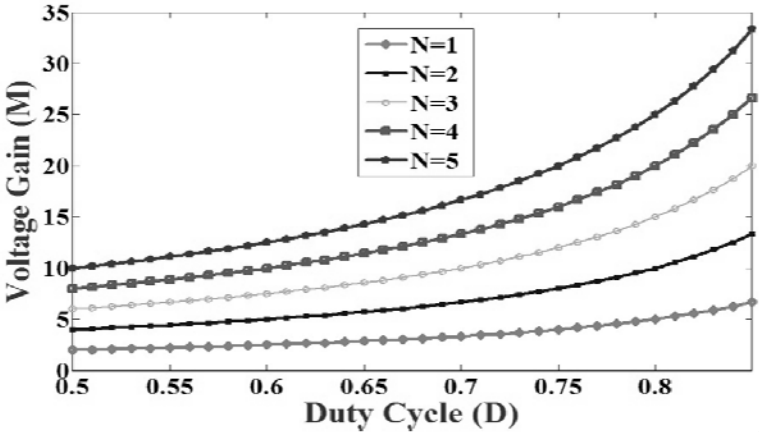

Figure 4. Gain vs Duty Cycle Plot

4. EXPERIMENTAL RESULTS

A 100W prototype is built to validate the operation of the proposed converter. A PIC 18F45K20 flash microcontroller was used to generate the gate pulse in an open loop structure at a switching frequency of 50 kHz at a duty cycle of 0.6. The duty cycle was adjusted to 0.6 so as to compensate for the diode voltage drop at each stage.

The input voltage of 24V was supplied by two 12V lead acid batteries. The switch used was a power MOSFET, IRFP250M and the diodes were MBR360 Schottky Barrier type. The experiments were carried out with a resistive load. Figure 5 shows the gate pulse, output voltage and output current waveforms. It is observed that the average output voltage and power obtained from the converter confirms its conversion ratio and the power delivering capability.

The voltage distribution across each of the output capacitors is shown in Figure 6. This validates the multilevel operation of the converter. Figure 7 shows the gate pulse and input current and output current. The proportional step down of current related to step up of voltage is observed. Further, the ripple current magnitude is within specified limits and this validates the design aspects of the converter.

Figure 8 shows the switch voltage and current stress. It is observed that the voltage stress across the device is 50V which is very less for 24V input and 240V output. Further, this validates equation 4. Figure 9a shows the switching of diodes D1, D3, D5, D7 and D9, i.e. the odd diodes. Figure 9b shows the switching of diodes D2, D4, D6 and D8, i.e. the even diodes. Figure 9c shows the complementary switching of the odd and even diodes; this validates the diodes voltage drop expression given by equation 6.

Figure 10a shows the input power drawn by the converter; Figure 10b shows the output power delivered. From this, the efficiency of the converter was computed and found to be about 72%. As the power switch and diodes undergo hard switching, the power loss across them becomes significant.

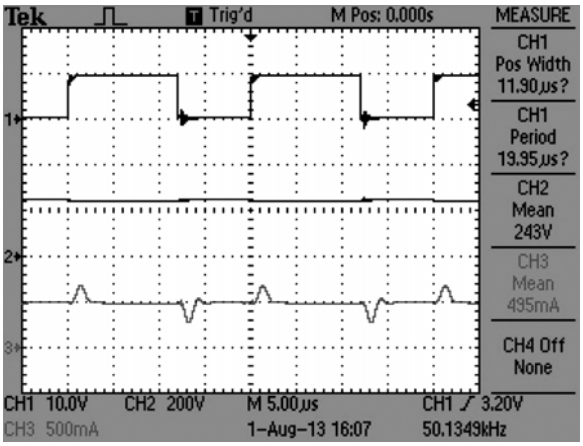

Figure 5. Gate Pulse, Output Voltage, Output Current.

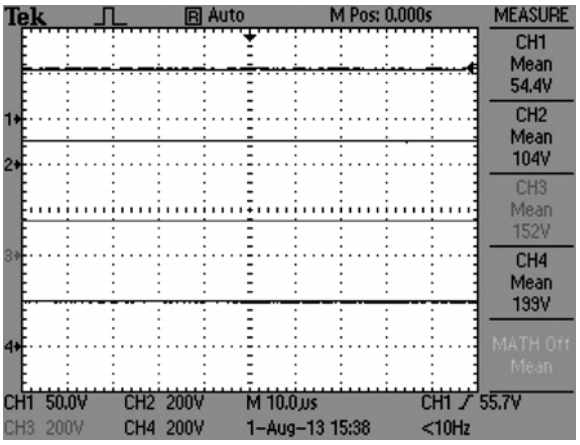

Figure 6. Multilevel Outputs.

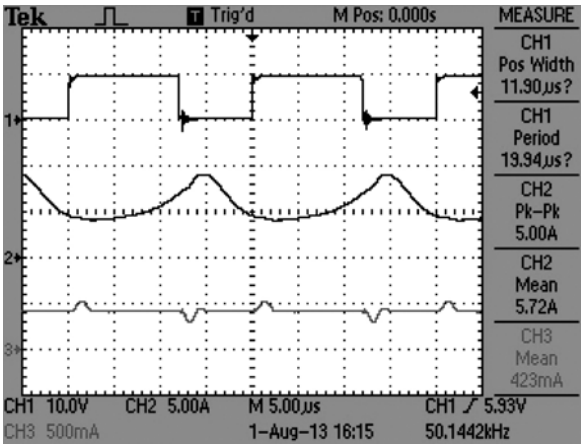

Figure 7. Gate Pulse, Input Current, Output Current.

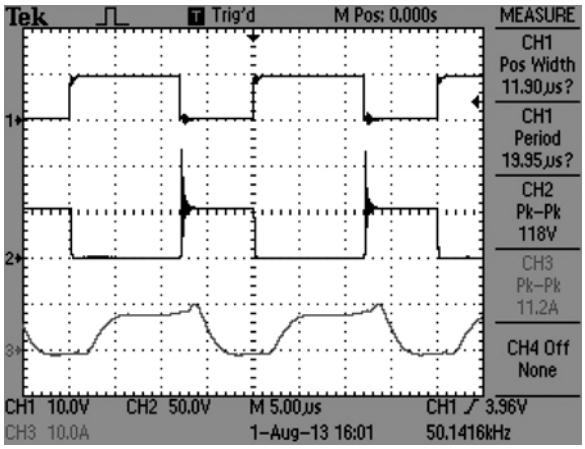

Figure 8. Switch Stress.

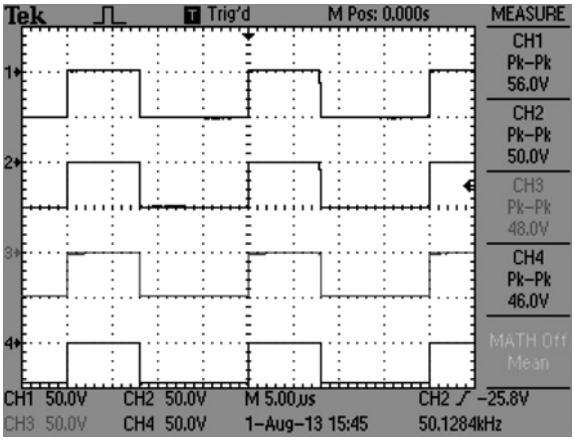

Figure 9a. Switching of Diodes D1, D3, D5 and D7.

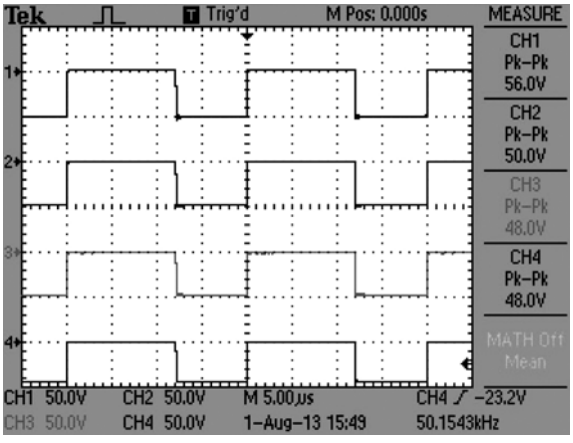

Figure 9b. Switching of Diodes D2, D4, D6 and D8.

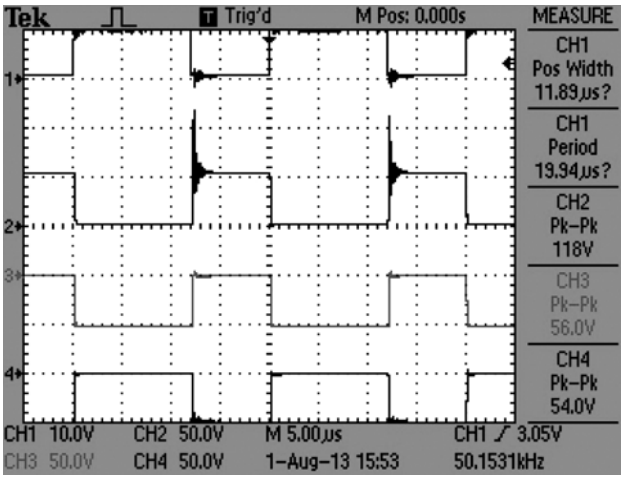

Figure 9c. Complementary Operation of Diodes D1 and D2.

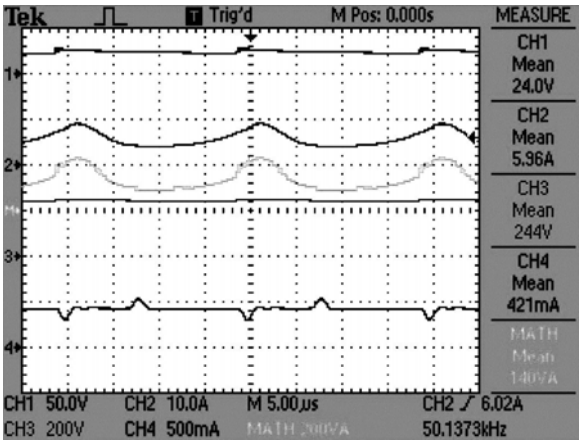

Figure 10a. Input Voltage, Input Current, Output Voltage, Output Current and Input Power Waveforms.

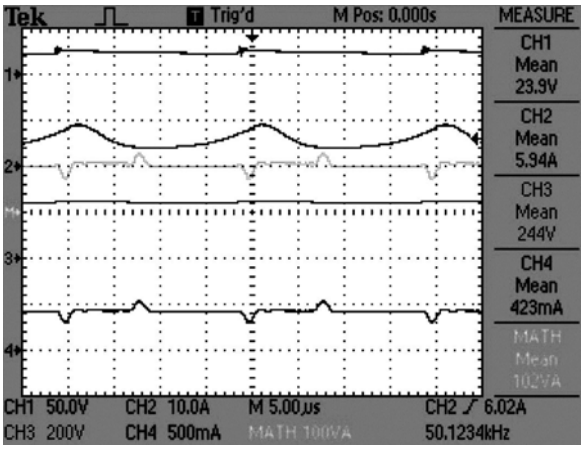

Figure 10b. Input Voltage, Input Current, Output Voltage, Output Current and Output Power Waveforms.

The hardware setup is shown in Figure 11. The inductor used had a value of 700µH and all capacitors are rated at 100µF/160V (aluminum electrolytic). The inductor is mounted on the same board as the power circuit. Power density of the converter can be improved by placing all the diodes around the inductor and removing the test points.

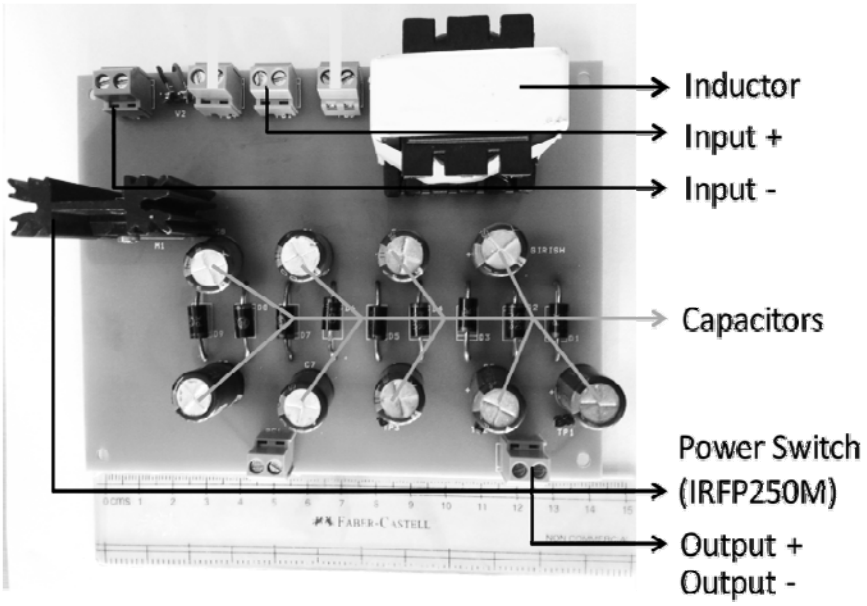

Figure 11. Experimental Setup.

5. CONCLUSION

The proposed converter has been designed, simulated and experimentally verified. The converter employs 5 stages in conjunction with the conventional boost converter which is operated at a duty cycle of 0.6. A voltage gain of 10 was obtained without using both a transformer or causing excessive device voltage and current stresses. The converter was designed to supply a load at 240V at 100W.

The output waveforms obtained from the simulation confirm the performance of the proposed converter. Experimental verification of the converter validates the results of the simulation as well as the feasibility of the converter. The converter is proposed to be used in applications with renewable sources in conjunction with multilevel inverters such as those found in distributed generations systems. The main

features of this topology are (i) transformer-less high gain; (ii) single switch design; (iii) continuous input current; and (iv) modularity.

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