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Multi-Port Current Source Inverter for Smart Microgrid Applications: A Cyber Physical Paradigm

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Abstract: This paper presents a configuration of dual output single-phase current source inverter with six-switches for microgrid applications. The inverter is capable of delivering power to two independent set of loads of equal voltages or different voltages at the load end. The control strategy is based on integral sliding mode control (ISMC). The cyber twin model-based test bench is developed to analyze the performance of the inverter. The cyber twin is a virtual model of the physical system to simulate behaviours. The performance of the inverter is analyzed with a cyber twin model and monitored through the remote system. Also, the inverter is analyzed with different voltage conditions.

Keywords: cyber physical systems; dual output inverter; rapid control prototype

1. Introduction

The distributed generation (DG) with photovoltaic, wind energy, fuel cell, and battery, termed as microgrid, can supply for low- and medium-voltage applications. The DC microgrid is capable of supplying both DC loads and AC loads with the inverter. The inverters for microgrid discussed in [1,2] are capable of supplying a single output. The inverters with reduced semiconductor switches and dual output are capable of feeding dual loads and less complexity in implementation. This enables the feeding of different types of loads using an inverter. The development of inverter with reduced power semiconductor devices makes the system economical and compact. The dual output inverters reduce the number of switches in a system and supplies energy to two AC autonomous loads. A four-switch inverter [3] is initially proposed with the reduced number of switches by replacing split capacitors for sharing between power converters. The dual output voltage source inverters discussed by Yu, Strake et al. [4] are dual phase single DC bus inverter with four-switches, three wire single-phase inverter with six-switches, dual phase dual DC bus inverter with four-switch, dual phase with four-switch and transformer. The inverter models discussed in [4] has the capability of operating only in half bridge configuration. The dual output single-phase inverter based on voltage source inverters (VSI) is proposed by Fatemi, et al. [5] explains about the half-bridge dual output inverter with the split capacitor as a sharing leg for both outputs and for the full bridge dual output with six-switches; the switch leg is common of for both outputs by sharing a row of switches for upper and lower outputs. The six-switch voltage source inverter delivers equal voltage at the output with open loop operation. The six-switch dual output with buck structure delivers dual output with the equal voltage at both output and operated in open loop is presented by Nguyen, et al. [6]. The dual output inverter with sharing of switch legs will results in the reduction of semiconductor switches by 25%.

From the literature, most of the researchers concentrate on dual output voltage source inverter rather than the dual output current source inverter. The current source inverters (CSI) have inherent short circuit protection owing to the presence of a dc link reactor which results in the low harmonic

distortion and better load voltage regulations [7,8]. The control of CSI is difficult compared to VSI due to the simultaneous regulation of DC link current and output voltage. The dynamic response of CSI is studied using a current controller [9] and continuous time-based control strategy is employed [10]. The sliding mode control (SMC) [8,11,12] provides a dynamic response to the nonlinear systems with the property of hysteresis. It offers stability to variations in system parameters and easy implementations. The sliding surface is created with reference to error variable of inductor current and capacitor voltage for single-phase single output CSI is proposed by Komurcugil, et al. [13]. The sliding mode control for voltage source inverter-based shunt active filter is presented in [14] for power quality improvements in the power system. The control of y source boost DC–DC converter controlled by cascaded sliding mode control is proposed by Ahmadzadeh et al. [15]. The control of power electronics equipment using sliding mode control is presented in the various literature for multi-terminal HVDC [16], induction motor control [17], h6 inverter [18], and modular multilevel converter [19]. The SMC [20] based control strategies are applied widely to single output inverters [1,2] rather than dual output inverters from the literature. To implement continuous time-based control strategies processors with high-speed data processing is required. Reconfigurable Input/Output (RIO) based processors are utilized effectively for these types of controllers [21].

The interfacing of the power electronics circuits to the smart environment [22,23] makes the system more efficient and controllable. This provides two-way communication between the target and the users (man to machine and vice versa) and results in cyber–physical systems (CPS) [24]. The CPS implementation will result in smart grids [25–27] and remote laboratories for educational purposes. The definition of CPS given by E.A. Lee [28] is that the integration of physical process with embedded computation, controlling and network monitoring along with the feedback loops for computations. In another way, CPS is defined as a controllable, credible and scalable network with the physical system. The CPS is stated as 3*Cs* (Computations, Communications, and Control). The basic concepts, method, and implementation of CPS is explained briefly by Liu, et al. [29]. CPS implementation for conveyor belt block pickup with application and platform level reconfiguration is in case of faults is presented by Andalam, et al. [30]. The CPS-based optimal power flow management in electric grid with energy demand management is proposed by Nguyen, et al. [31]. The remote monitoring of microgrid using LabVIEW and PLC has proposed in [32]. The researchers developed various CPS models for the physical systems with the utilization of wireless sensor network (WSN), radio frequency identification (RFID), Zigbee, CAN protocols [33–37]. The WSN can only sense signal but not capable of identifying the specific one from more sensors. Similarly, RFID also senses the data based on the perception of data. RFID is widely used in the Internet-of-Things (IoT). While IoT only has the perception of sensing alone, but CPS has the ability of the robust control to the target. The comparison of CPS for various applications is given in Table 1.

Table 1. CPS comparison.

Ref.	Sensors Type	Mode	Network/ Monitoring	Programming Platform
[33]	RFID Tag	Zigbee, CAN, RFID	XML	Multi domain
[34]	RTU	WSN	CC studio, SCADA/HMI	Multi domain
[35]	SenseLab Sensor	WSN	Cooja network simulator	Multi domain
[36]	Sensor nodes Green orbs	WSN, Zigbee	Green orbs host computer	Multi domain
[32]	Sensors PLC	WIFI	LabVIEW JIL server	Multi domain
Proposed	NI Sensors MyRIO	WIFI	LabVIEW VI Server	Single domain

As the growth in the CPS, the cyber twin (digital twin) [38] approach is introduced to realize the behaviour of the physical system with a virtual model. In the cyber twin approach, a virtual model realizes the behaviour of the physical system to predict the dynamic changes and respond to the system for better operation. The cyber twin approach has been proposed by various researchers; Kazi et al. [39] proposed fuzzy-based vehicle CPS system for driving assistance. To increase the feasibility in furniture production line Hao Zhang et al. [40] introduced the cyber twin approach. The comparison of cyber twin and big data for Industry 4.0 is anticipated by Qinglin et al. [41] to identify the possibilities and advantages of cyber twin for Industry 4.0.

In this paper, the modeling of dual output current source inverter with the capability of operating in equal voltage and different voltage modes at the output end for microgrid applications. The sliding mode control (SMC) strategies are introduced to control the dual output inverter and performance analysis of sliding mode and integral sliding mode control (ISMC) is performed. The comparative analysis of SMC and ISMC reveal the performance and better controller for a dual output current source inverter. The main advantages of ISMC are robustness of large variations, stability, and fast dynamic response. The integration of power electronics devices and cyber–physical systems (CPS) is introduced. The cyber twin model of the inverter is developed with LabVIEW and Multisim packages. The cyber twin model is the virtual model of the physical system; it operates by sensing the raw data for the analysis and control of the physical system. The cyber–physical test bench is developed with cyber twin model of the inverter. In literature for implementing cyber–physical test bench utilizing multidomain programming is given in Table 1. To avoid the complexity by utilizing the multidomain program, LabVIEW based single domain programming is used. The integration of this heterogeneous frame is needed to deploy on the single platform to reduce the data exchange error which occurs while using a different platform for each section. The cyber–physical test bench is developed based on LabVIEW, MyRIO, C-DAQ and NI-Web services. The interaction of cyber twin model by cyber integration layer with the physical device is needed for effective control of the system. The performance of the physical device is monitored by web services.

2. A Cyber Perspective Model

The Reconfigurable Input/Output (RIO)-based design of cyber–physical system RCP evaluation test bench is created for the evaluation of two switch dual output inverter with ISMC control. The experimental setup consists of three sections Physical layer, cyber–physical integration layer, and cyber layer. The CPS architecture consists of three layers: Physical layer, cyber–physical integration layer, and Cyber layer. Physical layer comprises of the physical device (target) which needs to be controlled and monitored by CPS. The cyber–physical integration layer has the sensors, controllers and software technologies with a host computer to collect the data from the physical device and to control the device based on the responses. In this layer the integration of cyber twin with physical model is initiated.

Cyber twin approach for power electronics systems is introduced and with cyber infrastructure. The virtual model of the physical model is developed to simulate the real behaviour and analyze the system. The Figure 1 displays the block diagram of the proposed cyber twin approach. The virtual model is developed in LabVIEW-Multisim packages. The physical device (inverter) voltage and current are sensed through data acquisition and analyzed with the virtual model in the host computer.

The data observed from this layer is monitored and the physical device is controlled by the control center through the internet. The data transfer between the physical device and control center is executed by cyber layer. Figure 2 shows the configuration of the proposed RCP evaluation of the inverter.

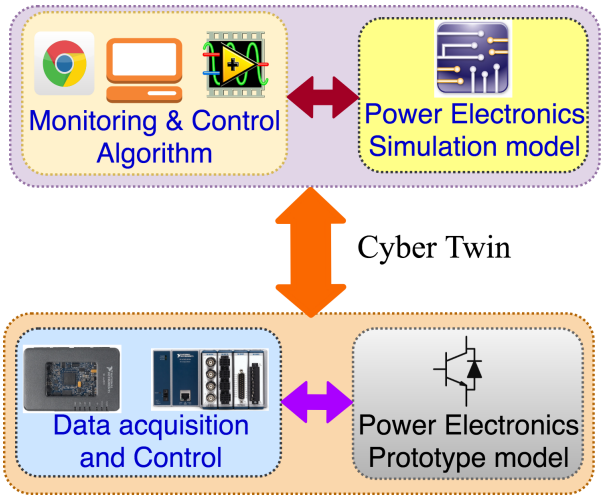


Figure 1. Block diagram of cyber twin.

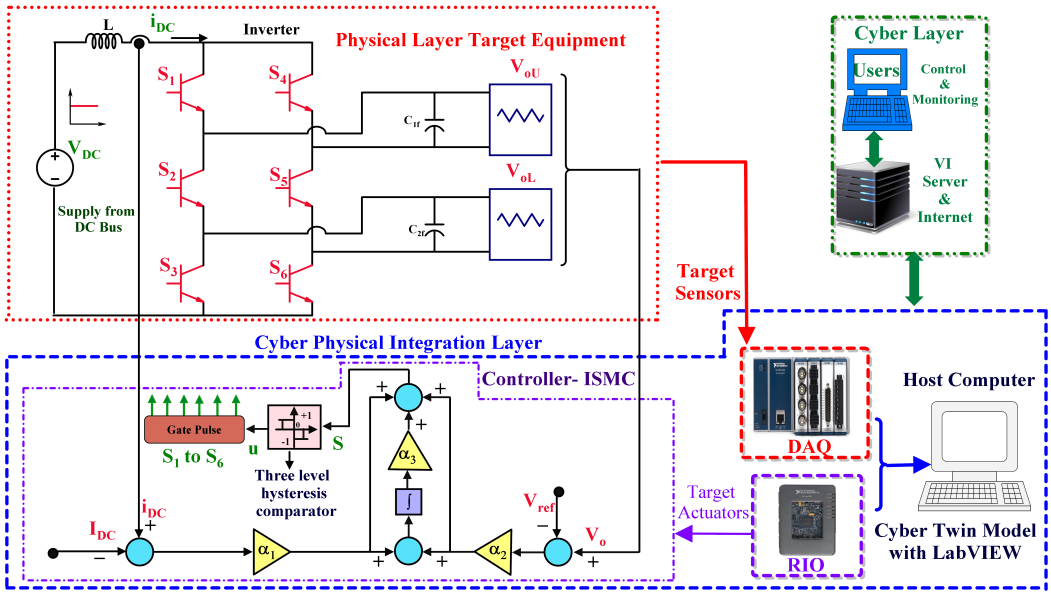


Figure 2. System Configuration.

Generalised CPS Model

The physical layer consists of the devices which are needed to monitor and control through CPS. Here the physical layer considered is inverter prototype with source and load. The generalised physical model is represented by Mulit-Input-Multi-Output (MIMO),

$$\dot{x}(t) = Ax(t) + Bu(t) \tag{1}$$

$$Y(t) = Cx(t) \tag{2}$$

where, A is the system matrix, B is the input matrix, C is the output matrix, $x(t)$ is the state vector, $u(t)$ is the control vector, $Y(t)$ is the observation vector.cyber–physical integration layer makes the interconnection between the physical layer and cyber layer. The devices which employed for integration are voltage/current sensor, driver circuits with an optocoupler, data acquisition system, and host computer. The control structure is given by,

$$u(t) = Kx(t) \tag{3}$$

where, $K \in R^{n_c x n_s}$ is the connection structure between controller and sensor. K_{ij} is non zero and shows the connection between controller (i_c) and sensor (j). The system with closed loop is given by,

$$\dot{x}(t) = \tilde{A}x(t) \tag{4}$$

$$\text{Closed loop matrix } (\tilde{A}) = A - BK \tag{5}$$

The dynamics of the system with delay between sensor and controller is represented by,

$$\dot{x}(t) \simeq \tilde{A}x(t) \tag{6}$$

$$\text{Matrix with delay } (\tilde{A}) = (I - BD_{i_cj}K)(A + BK) \tag{7}$$

$$\text{Delay Matrix } D_{i_cj} = \begin{cases} 1 \text{ if } j \text{ \& } i_c \text{ are conncected} \\ 0 \text{ if } j \text{ \& } i_c \text{ are not conncected} \end{cases} \tag{8}$$

The switching function of the system is given by,

$$\dot{x} = A_n x + B_n u; \quad t_{n-1} \leq t < t_n \tag{9}$$

To design the controller with the capabilities of cyber twin, the Sliding Mode Control (SMC) is identified due to modelling of control strategy based on mathematical model of the system.

3. Physical Layer: Dual Output Current Source Inverter

The microgrid schematic with proposed dual output inverter is shown in Figure 3. The proposed inverter is compared with the family of dual output inverters and given in Table 2. The configuration of the proposed dual output current source inverter is shown in Figure 2.

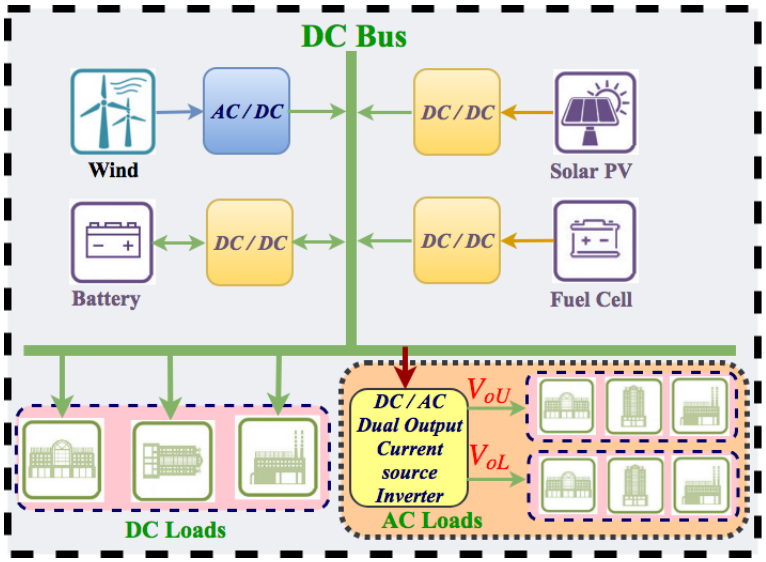


Figure 3. Schematic of Mircogrid.

It consists of a DC link reactor with six semiconductor switches. The inverter has two legs with three semiconductor switches and a sharing row of switches for upper and lower output. The inverter is capable of operating at equal voltages (EV) and different voltages (DV).

Table 2. Comparison of Inverters.

Inverter Type	Switches	Source Type	EV	DV
Dual phase with single DC bus with split Capacitor	4	Voltage	Yes	No
Dual phase with three wire	6	Voltage	Yes	No
Dual phase dual DC bus	4	Voltage	Yes	No
Dual phase with transformer	4	Voltage	Yes	No
Dual output VSI	6	Voltage	Yes	No
Single port conventional CSI	4	Current	Yes	No
Proposed	6	Current	Yes	Yes

3.1. Equal Voltage (EV) Mode of Operation

In this mode, the two AC outputs voltages are independent and equal. The inverter works similar to a full bridge with two parallel loads. The gate signals for upper (S_1, S_4) and lower (S_3, S_6) switches are generated by the control strategy. The control signals for sharing switches (S_2, S_5) is generated by the logical XOR of the upper and lower signals. The instantaneous output voltage (v_{on}) of the dual output inverter are same when it operates at EV mode is expressed in (10).

$$v_{on} = v_{oU} = v_{oL} = \sum_{n=1,3,5...}^{\infty} \frac{4V_{DC}}{n\pi} sin(n\omega t) \tag{10}$$

3.2. Different Voltage (DV) Mode of Operation

In this operating condition, the inverter is capable of delivering different voltage magnitude. The upper side will act as a full bridge and lower will act as a half bridge. The DV mode is in existence due to the presence of a DC link reactor. It will protect the inverter from short circuit and floating modes. If the inverter is operated at different voltage mode, the upper side voltage (v_{oU}) will be in full bridge mode as expressed in Equation (11) and the lower side (v_{oL}) will be in half bridge mode. The output equations for the half bridge are given by (11).

$$v_{oU} = \sum_{n=1,3,5...}^{\infty} \frac{4V_{DC}}{n\pi} sin(n\omega t), \quad v_{oL} = \sum_{n=1,3,5...}^{\infty} \frac{2V_{DC}}{n\pi} sin(n\omega t) \tag{11}$$

3.3. System Modelling

The dual output inverter is modeled based on CSI topology. It comprises the source voltage (V_S), a DC link reactor (L), IGBT switches, output capacitive filter (C) and a resistive load (R). The equation of the CSI is written as,

$$L\frac{di_{DC}}{dt} + ri_{DC} = V_S - V_{DC} \tag{12}$$

$$C\frac{dv_o}{dt} = i_o - \frac{v_o}{R} \tag{13}$$

where, u is the switching function, $V_{DC} = uv_o$ is the input DC voltage, $i_o = ui_{DC}$ is the output AC current, and r_{idc} the internal resistance of DC link reactor. In order to reduce the computational parameters of dual output inverter, it is assumed that $C = C_{1f} = C_{2f}$ as dual output capacitive filter and $v_o = v_{oU} = v_{oL}$ as the dual output voltage. The state space for the system operation is described in matrix form is given by (14),

$$\begin{bmatrix} \dot{v_o} \\ \dot{i_o} \end{bmatrix} = \begin{bmatrix} -r_{idc}/L & -1/L \\ -1/C & -1/RC \end{bmatrix} \begin{bmatrix} v_o \\ i_o \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} u + \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} v_o \\ i_o \end{bmatrix} \tag{14}$$

The transfer function for the system operation is represented in (15),

$$G(s) = \frac{\frac{1}{LC}}{S^2 - S\left(\frac{-L + RC(-r_{idc})}{RCL}\right) + \left(\frac{(-r_{idc}RC - L)LC + RCL}{RC^2L^2}\right)} \tag{15}$$

4. Cyber–Physical Integration Layer: Cyber Twin Model, C-DAQ, RIO with Sliding Mode Controllers

Cyber–physical integration layer in a CPS incorporates the algorithm to gather sensor information and issue control signals through actuators to the physical device. This layer has software and hardware coordination in-order to control and monitor the physical device. The cyber twin model of the inverter is developed for the integration with the physical device. The CPS should behave as, (A) Intelligent: To predict and understand the behaviour of the system using LabVIEW environment, (B) Real-Time: To gather the real-time data from physical device C-DAQ-9174 is utilised, (C) Adaptive & Predictive control: To respond and anticipate the changes in the physical systems the ISMC based control strategy is implemented in MyRIO-1900.

4.1. Sliding Mode Control (SMC)

The Sliding Mode Control (SMC) is an effective controller with switching nature of inverter derived from the system model. The advantages of SMC are, it has a better dynamic response, stability against the variations of the load and easy implementation. It consists of inner and outer control loops. The input inductor current and output capacitor voltage is considered as the state variables for controlling. The error variables are given by,

$$\text{Error Variables} = \begin{cases} x_1 = i_{DC} - I_{DC} \\ x_2 = V_o - V_{ref} \end{cases} \tag{16}$$

The sliding surface (S) of SMC is expressed by (17),

$$S = \alpha_1 x_1 + \alpha_2 x_2 \tag{17}$$

where, α_1 and α_2 are the sliding coefficients. The additional variable x_3 accumulates directly to the steady-state errors of x_1 and x_2. The time derivative of (17) is,

$$\dot{S} = \alpha_1 \dot{x_1} + \alpha_2 \dot{x_2} \tag{18}$$

The derivatives of x_1 and x_2 is given by (19) and (20),

$$\dot{x_1} = \frac{1}{L}\left(V_s - r_{idc} i_{DC} - u v_o\right) - \frac{dI_{DC}}{dt} \tag{19}$$

$$\dot{x_2} = \frac{1}{C}\left(u i_{DC} - \frac{v_o}{R}\right) - \frac{dV_{ref}}{dt} \tag{20}$$

By substituting (19) and (20) in time derivative Equation (18) gives (21),

$$\dot{S} = \left(-\frac{u\alpha_1}{L} - \frac{\alpha_2}{RC}\right) v_o + \left(-\frac{\alpha_1 r_{idc}}{L} + \frac{\alpha_2 u}{C}\right) i_{DC} + A \tag{21}$$

where A is given by (22),

$$A = \left(\alpha_1 \frac{V_s}{L} - \frac{dI_{DC}\alpha_1}{dt} - \alpha_2 \frac{dV_{ref}}{dt}\right) \tag{22}$$

The condition for stability $S\dot{S} < 0$ should be satisfied and the control variable is given by,

$$u = -signum(S) \tag{23}$$

To satisfy the stability condition, $u = 1$ and $u = -1$ is incorporated to Equation (21).
$if,\ S < 0 \Rightarrow \dot{S} > 0 \Rightarrow u = 1$

$$(S < 0) \Rightarrow (\dot{S} > 0) \Rightarrow \left[\left(-\frac{\alpha_1}{L} - \frac{\alpha_2}{RC}\right) v_o + \left(-\frac{\alpha_1 r_{idc}}{L} + \frac{\alpha_2}{C}\right) i_{DC} + A\right] > 0 \tag{24}$$

$if,\ S > 0 \Rightarrow \dot{S} < 0 \Rightarrow u = -1$

$$(S > 0) \Rightarrow (\dot{S} < 0) \Rightarrow \left[\left(\frac{\alpha_1}{L} - \frac{\alpha_2}{RC}\right) v_o + \left(-\frac{\alpha_1 r_{idc}}{L} - \frac{\alpha_2}{C}\right) i_{DC} + A\right] < 0 \tag{25}$$

From Equations (24) and (25) the simplified condition for stability is given by (26),

$$0 < \left(-\alpha_1 C + \alpha_2 \frac{L}{R}\right) v_o + (\alpha_2 L + \alpha_1 r_{idc} C)\, i_{DC} - LCA < 2\,(\alpha_2 L i_{DC} - \alpha_1 C v_o) \tag{26}$$

The equivalent continuous control variable u_{eq} is given by (27),

$$u_{eq} = \frac{LC}{v_o C \alpha_1 - \alpha_2 L}\left(-\frac{\alpha_2 v_o}{RC} - \frac{i_{DC}\alpha_1 r_{idc}}{L} + A\right) \tag{27}$$

The u_{eq} maintains the error variables of the systems. The problem with u_{eq} is complicated while implementing in analog controllers. For the easy implementation of sliding mode control instead of direct implementation of u_{eq}, the switching relay function is used. The switch relay function is given by (28),

$$u_{eq} = \text{-sign(S)} = \begin{cases} +1 & if\ \ S < 0 \\ -1 & if\ \ S > 0 \end{cases} \tag{28}$$

The switching function is realized by *signum* function and direct implementation of this function results in uncontrolled switching frequency and no steady-state errors. Operating of CSI in this condition leads to system failure in practical conditions. To operate CSI with limited frequency and controllable, hysteresis band with boundary layer is utilized. The hysteresis band is implemented instead of *signum* function and the function is given by (29),

$$u = \begin{cases} +1 & if\ \ S < -h \\ -1 & if\ \ S > h \end{cases} \tag{29}$$

The hysteresis bandwidth in S is used to control the dual output CSI with switching frequency, inductor current, and capacitor voltage. If $S = 0$, CSI cannot be controlled. To control dual output CSI, the switching should lie in $S = \pm h$. The performance plot for both inductor current and capacitor output voltage is given in Figure 4a,b. The parameters considered are $L = 10$ mH, $C = 20$ µF, $R = 50\ \Omega$, $\alpha_1 = 0.0002$, $\alpha_2 = 0.2$ and $\alpha_3 = 50$ and are simulated with Matlab.

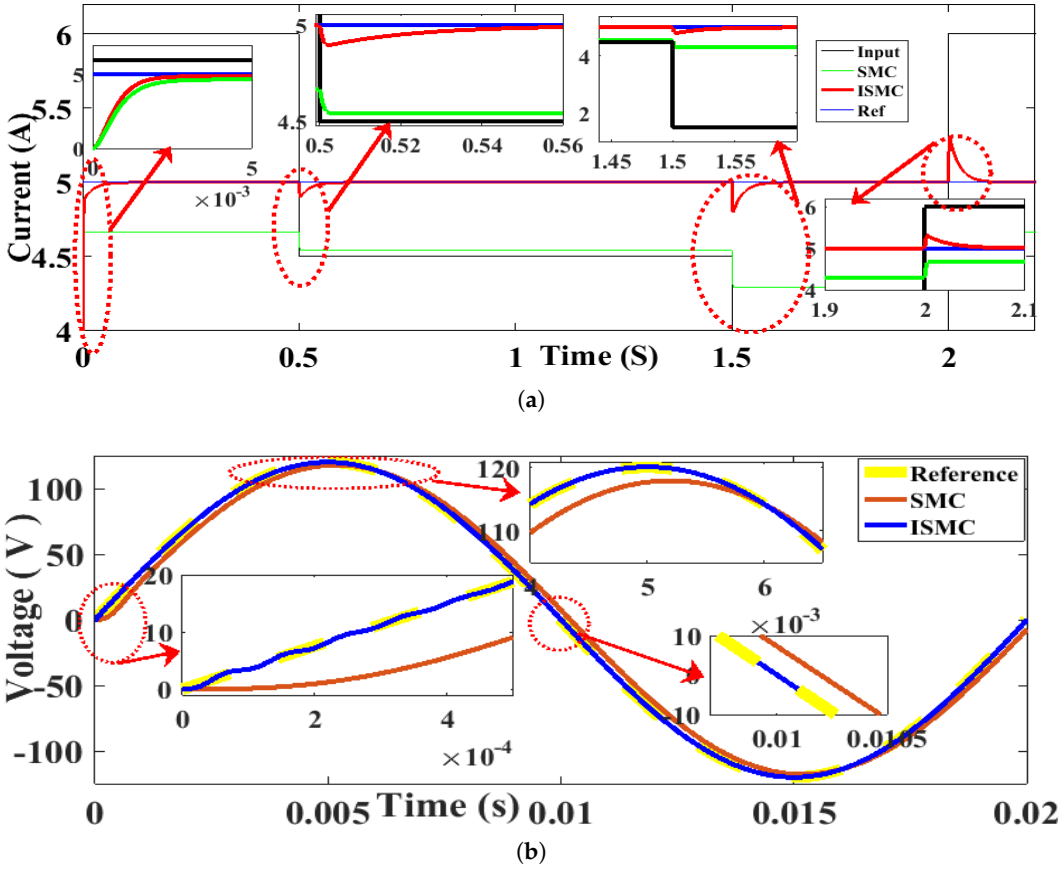


Figure 4. Performance comparision of SMC and ISMC: (**a**) Input current, (**b**) Output Voltage.

4.2. Integral Sliding Mode Control (ISMC)

The SMC-based control has steady-state errors in both capacitor output voltage and inductor current. It is observed from Figure 4b, that the capacitor output voltage is not tracked with the reference voltage and has a steady-state error of 10%. The steady-state error of the inductor current is about 5% as observed from Figure 4a. As a method to suppress the steady-state error of the inductor current and output voltage, an additional integral term of the state variables x_1 and x_2 are introduced to the sliding surface. The additional integral term of error variable is introduced into SMC as an additional control variable and stated as an integral sliding mode controller (ISMC). The additional variable x_3 is considered and it is obtained by integrating the state variables x_1 and x_2 is given by (30),

$$\text{Error Variable} = x_3 = \int (x_1 + x_2) dt \tag{30}$$

The sliding surface (S) of ISMC is expressed by (31),

$$S = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 \tag{31}$$

where, α_1, α_2 and α_3 are the sliding coefficients. The additional variable x_3 accumulates directly to the steady-state errors of x_1 and x_2. The time derivative of (31) is,

$$\dot{S} = \alpha_1 \dot{x_1} + \alpha_2 \dot{x_2} + \alpha_3 \dot{x_3} \tag{32}$$

$$\dot{x_3} = x_1 + x_2 \tag{33}$$

The derivatives of x_1, x_2 and x_3 is given by (34)–(36),

$$\dot{x_1} = \frac{1}{L}\left(V_s - r_{idc} i_{DC} - u v_o\right) - \frac{dI_{DC}}{dt} \tag{34}$$

$$\dot{x_2} = \frac{1}{C}\left(u i_{DC} - \frac{v_o}{R}\right) - \frac{dV_{ref}}{dt} \tag{35}$$

$$\dot{x_3} = \left(i_{DC} - I_{DC}\right) + \left(v_o - V_{ref}\right) \tag{36}$$

By substituting (34)–(36) in time derivative Equation (32) gives (37),

$$\dot{S} = \left(-\frac{u\alpha_1}{L} - \frac{\alpha_2}{RC} + \alpha_3\right) v_o + \left(-\frac{\alpha_1 r_{idc}}{L} + \frac{\alpha_2 u}{C} + \alpha_3\right) i_{DC} + B \tag{37}$$

where B is given by (38),

$$B = \left(\alpha_1 \frac{V_s}{L} - \frac{dI_{DC}\alpha_1}{dt} - \alpha_2 \frac{dV_{ref}}{dt} - \alpha_3 I_{DC} - \alpha_3 V_{ref}\right) \tag{38}$$

The condition for stability $S\dot{S} < 0$ should be satisfied and the control variable is given by,

$$u = -signum(S) \tag{39}$$

To satisfy the stability condition, $u = 1$ and $u = -1$ is incorporated to Equation (38).
$if,\ S < 0 \Rightarrow \dot{S} > 0 \Rightarrow u = 1$

$$(S < 0) \Rightarrow (\dot{S} > 0) = \left[\left(-\frac{\alpha_1}{L} - \frac{\alpha_2}{RC} + \alpha_3\right) v_o + \left(-\frac{\alpha_1 r_{idc}}{L} + \frac{\alpha_2}{C} + \alpha_3\right) i_{DC} + B\right] > 0 \tag{40}$$

$if,\ S > 0 \Rightarrow \dot{S} < 0 \Rightarrow u = -1$

$$(S > 0) \Rightarrow (\dot{S} < 0) = \left[\left(\frac{\alpha_1}{L} - \frac{\alpha_2}{RC} + \alpha_3\right) v_o + \left(-\frac{\alpha_1 r_{idc}}{L} - \frac{\alpha_2}{C} + \alpha_3\right) i_{DC} + B\right] < 0 \tag{41}$$

From Equations (40) and (41) the simplified condition for stability is given by (42),

$$0 < \left(-\alpha_1 C + \alpha_2 \frac{L}{R} - \alpha_3 LC\right) v_o + \left(-\alpha_3 LC + \alpha_2 L + \alpha_1 r_{idc} C\right) i_{DC} - LCB < 2\left(\alpha_2 L i_{DC} - \alpha_1 C v_o\right) \tag{42}$$

The equivalent continuous control variable u_{eq} is given by (43),

$$u_{eq} = \frac{LC}{v_o C\alpha_1 - \alpha_2 L}\left(-\frac{\alpha_2 v_o}{RC} + v_o\alpha_3 - \frac{i_{DC}\alpha_1 r_{idc}}{L} + i_{DC}\alpha_3 + B\right) \tag{43}$$

The information about the sliding mode is given by (42). In the proposed ISMC, the condition for stability in (42) is tested by the numerical computations of the sliding coefficients (α_1, α_2 and α_3). The stability is tested along with i_{DC} and v_o minimum and maximum values, and from (42) Equation (44) can be obtained based on the numerical computations.

$$2\left(\alpha_2 L i_{DC} - \alpha_1 C v_o\right) > 0 \tag{44}$$

Due to the stability requirement the sliding coefficients (α_1, α_2 and α_3) will be positive. In steady-state condition $i_{DC} = I_{DC}$. The condition for v_o is given by,

$$\frac{\alpha_2}{\alpha_1} > \frac{C v_o}{L i_{DC}} \tag{45}$$

The sliding coefficient (α_3) will be determined regardless of (α_1 and α_2) by fine-tuning to obtain the desired response. The block diagram for ISMC is shown in Figure 2. The switching function is defined by the hysteresis (h) block in the controller design. The hysteresis switching function has three levels ($-1, 0, +1$). Hysteresis band is fixed based on the reference output voltage (v_o). In general, the hysteresis band (h) will be fixed between 5–10%. The instantaneous hysteresis band is calculated based on the frequency (f) and expressed as (46),

$$\text{Hysteresis band } = \frac{1}{8fL}\left(V_{DC} - \frac{4v_o^2}{V_{DC}}\right) \tag{46}$$

In three-level hysteresis, for $+_{ve}$ operation voltage is $+V_{DC}$ when error reaches the lower hysteresis band ($h_{lower}, -h$) and '0' when reaches lower then '$-h$'. For $-_{ve}$ operation voltage is $-V_{DC}$ when error reaches the upper hysteresis band ($h_{upper}, +h$) and '0' when reaches higher than '$+h$'. In two-level hysteresis, the no existence of dead band (t_d) due to the direct transition of $+_{ve}$ to $-_{ve}$ The excursion of sliding surface (S) beyond the hysteresis band (h) results in a dead band (t_d) for semiconductor switches. In three-level hysteresis, the '0' level existence will result in the dead time for semiconductor switches and has less distortion in output voltage. The switching frequency (f_{sw}) for three-level hysteresis function [11] is calculated based on (47),

$$f_{sw} = \frac{\omega_o^2 V_{DC}}{h + t_d \omega_o^2 V_{DC}}\left(\frac{2}{\pi}m - \frac{1}{2}m^2\right) \tag{47}$$

where, $\omega_o = 2\pi f$, f is the line frequency, m is the amplitude of disturbance. The instantaneous switching frequency (f_{in}) is based on the transition between h_{upper} to h_{lower}. The average switching frequency is calculated with the dead-band of 3 µs and hysteresis width of 0.05 V µs resulted in the average switching frequency of 2.9 kHz and the line frequency is 50 Hz. The switching function for the inverter model shown in Figure 2 is given by (48),

$$\begin{aligned} u_{1,2} &= \begin{cases} +1 \;\; if \;\; S < -h \\ 0 \;\; if \;\; S > 0 \end{cases} \qquad u_{4,5} = \begin{cases} -1 \;\; if \;\; S > +h \\ 0 \;\; if \;\; S < 0 \end{cases} \\ u_{2,3} &= \begin{cases} +1 \;\; if \;\; S < -h \\ 0 \;\; if \;\; S > 0 \end{cases} \qquad u_{5,6} = \begin{cases} -1 \;\; if \;\; S > +h \\ 0 \;\; if \;\; S < 0 \end{cases} \end{aligned} \tag{48}$$

The sliding surface (S) is the input to the Schmitt trigger (hysteresis switching). The schmitt trigger is designed to operate as per the switching conditions (48) for generating control signals. The ISMC respond better than SMC and minimized the steady-state errors. The ISMC based control strategy is implemented for the dual output single-phase inverter. The controller is designed in reconfigurable input/output (RIO) processor. The experimental test bench is created and the performance of the inverter with the ISMC is analyzed. The performance of the SMC and ISMC is analyzed and shown in Figure 4a,b. The inner current control is analyzed by fixing the reference of 5 A and changing the input signal of 6 A, 4.5 A, 1.5 A, and 6 A. It is inferred from Figure 4a, the settling time for SMC is 0.01 s with a steady-state error of 10% and ISMC has 0.05 s with tracking to reference and alleviates the steady-state error in the inductor current. From Figure 4, it is observed that the SMC has the high steady-state error compared to ISMC. For the outer voltage control loop analysis, the reference voltage is 120 V. It is inferred from Figure 4b, then the steady-state error of SMC is 10% and not tracking the reference voltage and ISMC alleviates the steady-state error in the voltage and settles at 0.005 s with oscillations. The control based on SMC has higher steady-state error compared to ISMC. The host computer with LabVIEW, C-DAQ, and MyRIO comprises a cyber–physical integration layer as shown in Figure 2.

4.3. Cyber Physical Test Bench

The LabVIEW is a graphical programming tool with seamless integration of hardware for both data acquisition and controlling physical devices. The source voltage (V_{ABC}), source current (i_{DC}), output voltage (V_o), output current (i_o) is sensed from the physical device using the NI C-DAQ 9174 with voltage (NI-9225) and current (NI-9227) sensor. The voltage and current data collected from the physical layer are processed in LabVIEW. The acquired signals are monitored in the front panel. the control algorithm for inverter based on ISMC is modeled and block diagram is shown in Figure 2.

The controller (actuator) is based on NI-1900 MyRIO (Reconfigurable Input/Output) which has Xilinx Zynq-7010 with a combination of Artix-7 FPGA processor, dual-core ARM Cortex-A9 real-time processor and, onboard WIFI. As an advantage of RIO architecture and WIFI, the physical equipment at a remote location is easily controlled. The terminals are reconfigurable as per the requirements. This leads this test bench to be utilized for all power electronics prototype testing. The control algorithm is programmed in NI-My RIO 1900 and connected to the physical device gate driver TI SM72295. The experimental setup is shown in Figure 5.

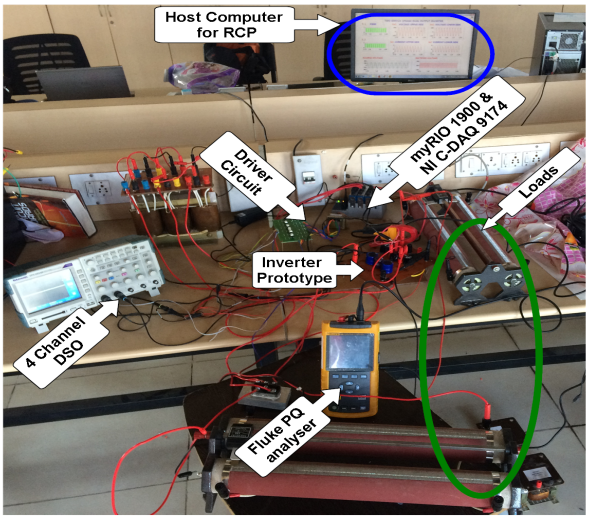


Figure 5. Experimental Setup.

5. Cyber Layer—LabVIEW Based CPS

The combination of the physical layer and the cyber–physical layer is integrated into the cyber layer. The cyber layer has a host computer with server and monitoring station (control center). The data transmission and security is the major concern in the cyber layer. The traditional data transmission is not sufficient to transfer large data in CPS. In order to satisfy the needs, the CPS must have the inbuilt transmission systems. The MyRIO has inbuilt Wi-Fi for data exchange between the host and target. While considering the security of the connection, It utilizes the TCP protocol with SSL.x.509 secured layer to enhance the security. The host computer with LabVIEW has the web service management tool for creating the secured URL. The URL mapping is given by https://localhost:portaddress/webservice.html. The LabVIEW has the inbuilt server for the data exchange with a secured network. The collected data from the target is monitored and controlled through the web browser. This method has good live data support, good interaction between the client and user. The network monitoring and active devices monitoring across the network is tracked using the total network monitor. Figure 6 depicts the network map of the system.

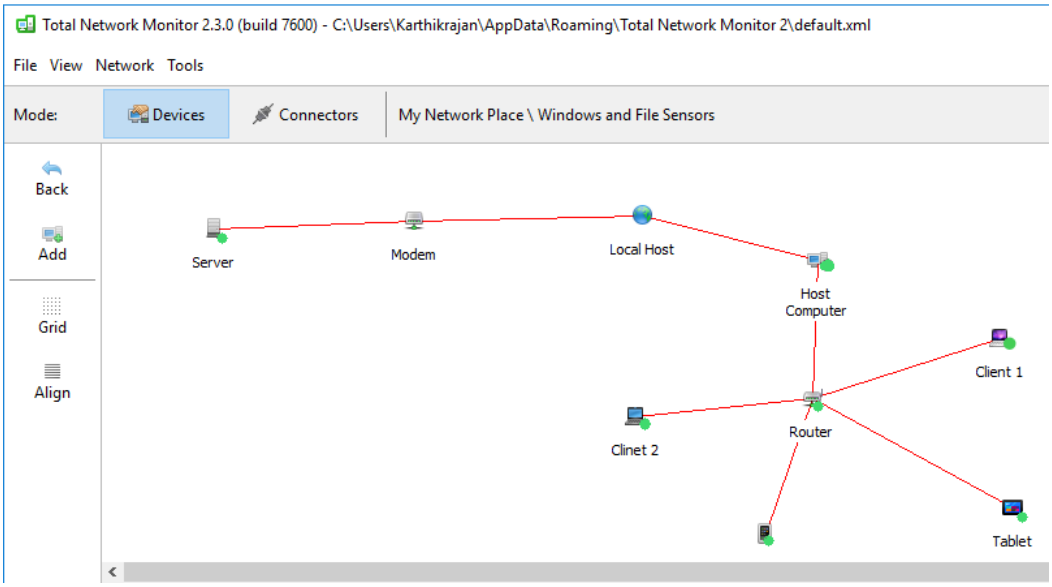


Figure 6. Network Monitor.

6. Results and Discussions

The performance of the proposed dual output inverter with ISMC control strategy is tested and monitored through the CPS system. The analysis was performed under various test conditions like equal output voltage at both the upper and lower side, the different output voltage in upper and lower side and inverter analyzed with and without load variations. The control strategy is implemented using a reconfigurable input/output (RIO) processor. The hardware prototype is fabricated to demonstrate the proposed inverter. The prototype specifications are given in Table 3.

Table 3. System Parameters.

Parameters	Values (Units)
Maximum Rated Power	1 kW
DC Voltage (V_{DC})	120 V
Inductor	10 mH
IGBT	IRG4BC30S
Controller	NI myRIO 1900
Data Acquisition Systems	NI C-DAQ 9174
Driver Circuit	Texas Instruments SM72295
Server	NI web server
Network Monitoring	Total Network Manager (TNM)
Oscilloscope	Textronix TPS 2024B four channel

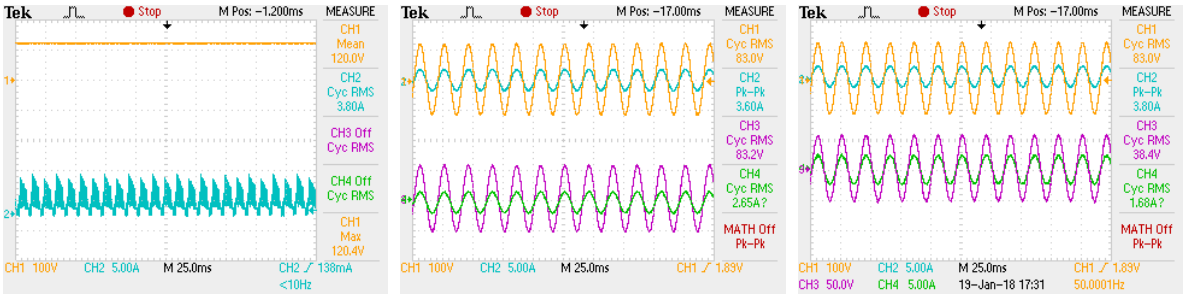
6.1. Steady State Performance

The steady-state performance of the dual output current source inverter is analyzed with an ISMC-based control strategy. The tracking performance of ISMC is discussed in Section 4.2 and performance the comparison of SMC with ISMC is plotted in Figure 4a,b. The IMSC alleviates the steady-state error and settles at 0.05 s. Figure 7 shows the performance of dual output inverter with ISMC.

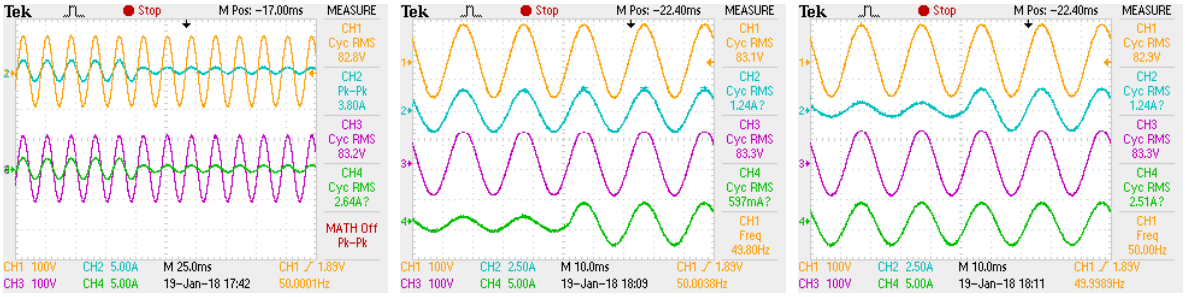
The DC voltage (V_{dc}) and current (I_{dc}) are shown in Figure 7a. Due to the current source inverter configuration, the DC link inductor limits the sudden changes in the current and the distortion will get reduced. Figure 7b depicts the dual output voltage and current for 50 Hz operation at EV mode. The dual output current source inverter delivers 83 V at both loads ends (V_{oU}, V_{oL}) due to the DC link of 120 V. The upper load current (I_{oU}) 3.60 A is observed and lower output current (I_{oL}) is 2.65 A.

The dual output CSI can deliver different voltages (DV mode). In this mode, the upper output voltage is similar to full bridge inverter and lower output voltage similar to a half bridge inverter.

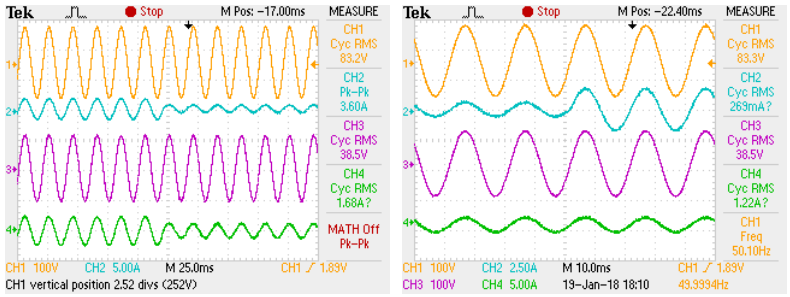
Figure 7c shows the upper output voltage (V_{oU}) as 83 V and lower voltage (V_{oL}) as 38.4 V. The upper load current (I_{oU}) observed is 3.80 A and lower load current (I_{oL}) observed is 1.68 A. The inverter is operated at both EV and DV mode with ISMC.



(**a**) $CH_1 - V_{dc}, CH_2 - I_{dc}$ (**b**) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$ (**c**) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$



(**d**) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$ (**e**) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$ (**f**) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$



(**g**) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$ (**h**) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$

Figure 7. Prototype Results: (**a**) DC voltage and current, (**b**) EV mode output voltage and load current, (**c**) DV mode output voltage and load current, (**d**) EV mode output voltage and load current with step change, (**e**) EV mode output voltage and load current with step change in lower load, (**f**) EV mode output voltage and load current with step changes in upper load, (**g**) DV mode output voltage and load current with step changes in load, (**h**) DV mode output voltage and load current with step change in upper load.

6.2. Response to Load Variations

Figure 7d depicts the step change in both upper and lower load of the dual output current source inverter when it operates in EV mode. The inverter operates at 50 Hz, the output voltage of upper (V_{oU}) and lower voltage (V_{oL}) is 83 V. The IMSC has a robust response to the load variation and maintains the voltage at the desired level. Figure 7e,f represent the dual output current source inverter waveforms

when a sudden step change in upper or lower load. Figure 7e shows the upper (V_{oU}) and lower voltage (V_{oL}) respectively. The change in upper load (I_{oU}) and current observed is 1.24 A and lower load current (I_{oL}) results in 597 mA and waveforms shows the change in load. From Figure 7f the EV mode operation with a step change in upper load is observed with 83 V in upper and lower. The load current is 1.24 A and 2.51 A respectively.

In Figure 7g, the performance of the inverter with ISMC is shown. The resultant waveform sohws the operation of the inverter at a different voltage (DV mode) with variations in load current. Figure 7g shows the upper voltage (V_{oU}) 83 V and lower voltage (V_{oL}) 38 V with variations in upper load current (I_{oU}) and lower load current (I_{oL}).

In Figure 7h, the performance of inverter in DV mode with a step change in upper load is analyzed and corresponding upper load current (I_{oU}) is 269 mA. The lower load current (I_{oL}) inferred is 1.22 A. The overall observations from Figure 7 shows that dual output current source inverter has the capability of supplying two independent loads of same (EV mode) and different voltage (DV mode). The dual output current source inverter has the capability of supplying two independent loads of equal (EV mode) and different voltage (DV mode). The dual output inverter can be used in renewable applications to simultaneously feed power to the grid and to the stand-alone load. In electric drive applications to operate two different machines of the same or different voltage level. The selection of DC link inductor should be concentrated more to obtain the maximum performance of the inverter. Gate pulse generation of the middle switches is critical due to dual operation.

6.3. Harmonic Analysis

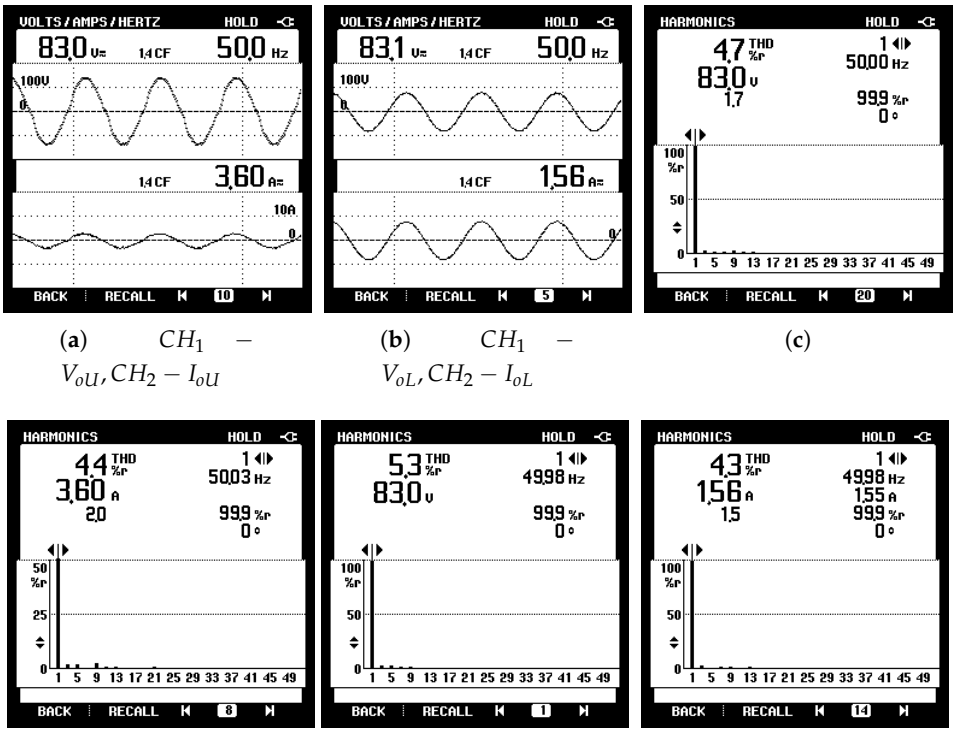
The performance of the inverter is analyzed with a single-phase power quality analyzer (Fluke analyzer). The harmonic analysis is performed at EV and DV mode. The THD is tabulated in Table 4.

Table 4. THD.

THD	Upper Side THD %		Lower Side THD %	
	EV	**DV**	**EV**	**DV**
Voltage THD	4.7	4.7	5.3	4.3
Current THD	4.4	5.4	4.3	4.8

Figure 8 depicts the output voltage and current of the Inverter in EV mode. From Figure 8a, the upper voltage (V_{oU}) and upper current (I_{oU}) are observed. Figure 8b shows the lower voltage (V_{oL}) and lower current (I_{oL}). The total harmonic distortion (THD) of upper load voltage and current is observed from Figure 8. Figure 8c depicts the THD of upper voltage (V_{oU}) is 4.7% and from Figure 8d it is observed that THD of upper current (I_{oU}) is 4.4%. The total harmonic distortion (THD) of lower load voltage and current is observed from Figure 8. From Figure 8e the THD of lower voltage (V_{oL}) observed is 5.3%. Figure 8f depicts the THD of lower current (I_{oL}) is 4.3%. The THD observed from the results depicts that the THD is under the acceptable limit as per standards IEEE519-2014.

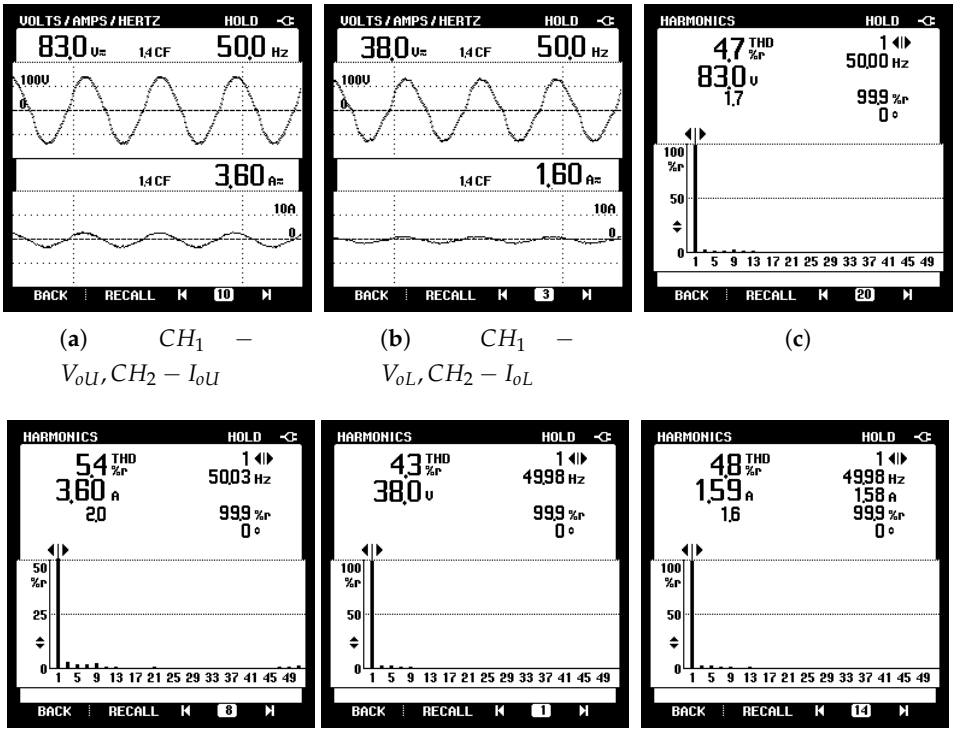
Figure 9 depicts the output voltage and current of the Inverter in DV mode. From Figure 9a the upper voltage (V_{oU}) and upper current (I_{oU}) is observed. Figure 9b shows the lower voltage (V_{oL}) and lower current (I_{oL}). The total harmonic distortion (THD) of upper load voltage and current is observed from Figure 9. Figure 9c depicts the THD of upper voltage (V_{oU}) is 4.7% and from Figure 9d it is observed that THD of upper current (I_{oU}) is 5.4%. The total harmonic distortion (THD) of lower load voltage and current is observed from Figure 9. From Figure 9e the THD of lower voltage (V_{oL}) observed is 4.3%. Figure 9f depicts the THD of lower current (I_{oL}) is 4.8%. The THD observed from the results depicts that the THD is under the acceptable limit as per standards IEEE519-2014.



(**a**) $CH_1 - V_{oU}, CH_2 - I_{oU}$ (**b**) $CH_1 - V_{oL}, CH_2 - I_{oL}$ (**c**)

(**d**) (**e**) (**f**)

Figure 8. Prototype Results: (**a**) Upper output voltage and load current, (**b**) Lower output voltage and load current, (**c**) Upper output voltage THD, (**d**) Lower output voltage THD, (**e**) Upper Current THD, (**f**) Lower Current THD.



(**a**) $CH_1 - V_{oU}, CH_2 - I_{oU}$ (**b**) $CH_1 - V_{oL}, CH_2 - I_{oL}$ (**c**)

(**d**) (**e**) (**f**)

Figure 9. Prototype Results: (**a**) Upper output voltage and load current, (**b**) Lower output voltage and load current, (**c**) Upper output voltage THD, (**d**) Lower output voltage THD, (**e**) Upper Current THD, (**f**) Lower Current THD.

6.4. Voltage Stress

The inverter model has six-switches S_1 to S_2. The voltage stress of the switches calculated by the peak voltage across the collector and emitter terminals. The voltage stress $V_{Sw_{1-6}}$ is given by,

$$V_{Sw_{1-6}} = \frac{V_{DC}}{2} \tag{49}$$

6.5. Loss Analysis

The total power loss (P_{loss}) of the IGBT is given by,

$$P_{loss} = P_{ON-H} + P_{ON-l} + P_{SW} \tag{50}$$

where, P_{ON-H} is the conduction loss of IGBT at high side, P_{ON-L} is the conduction loss of IGBT at low side, P_{SW} is the switching loss of IGBT.

6.5.1. IGBT Conduction Loss

The conduction loss occurs when the IGBT or free wheeling diode is in ON state. The conduction loss on high side P_{ON-H} of the inverter is given by,

$$P_{ON-H} = I_o^2 \times R_{ON-H} \times \frac{V_o}{V_{DC}} \tag{51}$$

The conduction loss on low side P_{ON-H} is given by,

$$P_{ON-L} = I_o^2 \times R_{ON-L} \times \left(1 - \frac{V_o}{V_{DC}}\right) \tag{52}$$

where, the R_{ON-H} and R_{ON-L} is the resistance of IGBT for high and low side respectively.

6.5.2. IGBT Switching Loss

The power loss occurred during the transition and based on switching frequency. The switching loss P_{SW} is calculated by,

$$P_{SW} = \frac{1}{2} \times V_{DC} \times I_o \times \left(t_r + t_f\right) \times f_{sw} \tag{53}$$

where, t_r and t_f is the high time and fall time of IGBT. f_{sw} is the switching frequency.

The total loss compared to a conventional current source inverter (CSI) is tabulated in Table 5. The total loss calculated for two conventional inverters to deliver dual loads is 22.064 W and proposed dual output CSI has 16.548 W. The proposed dual output CSI has the ability to supply two aindependent loads with the reduced number of semiconductor switches.

Table 5. Loss comparison.

Inverter Type	No of Outputs	No of Switches	Total Loss (w)
Conventional CSI	1	4	11.032
Two conventional CSI	2	8	22.064
Proposed dual output CSI	2	6	16.548

6.6. Online Monitoring

The CPS design is implemented to evaluate the performance of CSI dual output inverter. The control and monitoring of the target device are done through the internet browser. The connection is based on TCP protocol and SSL.x.509 secured layer is used to ensure the webpage security.

From Figure 10 the online monitoring of dual output CSC inverter performance is displayed. The resilient cyber infrastructure designed using single domain has the advantage of lower transport delay and easy implementation compared to other methods. The network monitoring of server and client is monitored by Total Network Monitor as shown in Figure 6. The incorporation of CPS in the inverter model leads to the development of smart grids, smart manufacturing in industries for controlling inverters in drives and smart learning with decentralized control of multiple systems.

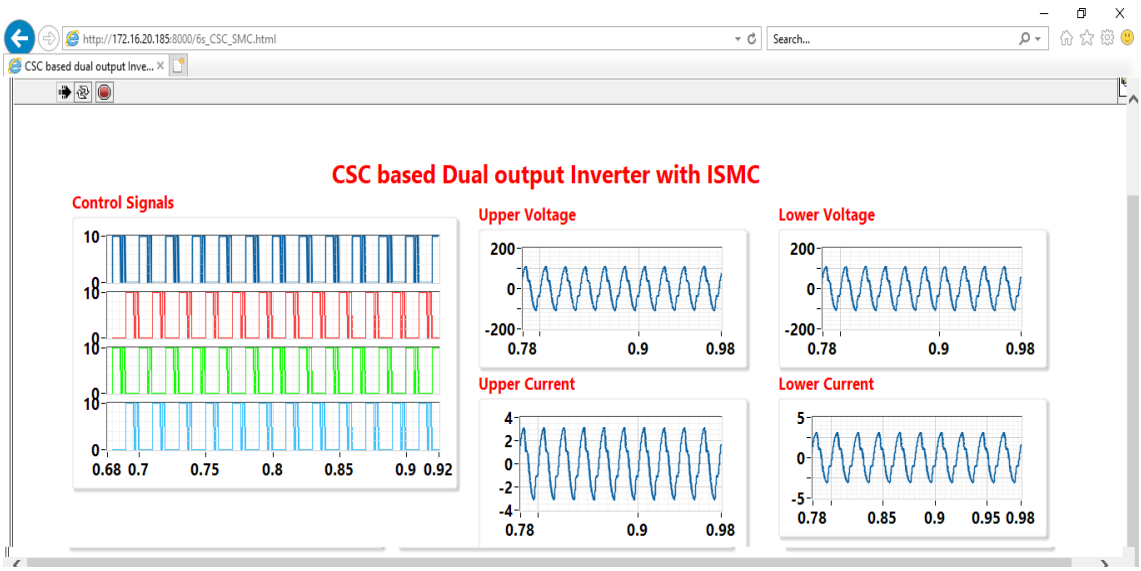


Figure 10. Monitoring Screen.

7. Conclusions

The dual output current source inverter topology operating in two different voltage modes is presented. A significant advantage of this topology is that it can supply power simultaneously to two different loads of equal (EV mode) and/or different (DV mode) voltages for microgrid applications. The control strategy based on sliding mode controllers is analyzed. The conventional sliding function has the steady-state error of 10% for voltage control and 5% for current control. To alleviate the steady-state error, an additional integral term is introduced and integral sliding mode control is derived for the dual output current source inverter. The cyber twin approach for the control of power electronics circuits is introduced and notable results are achieved. Reconfigurable Input/Output processors (MyRIO-1900) with cyber physical test bench is developed to implement continuous time-based control strategies, processors with high speed data processing is required. The development the cyber physical system for an inverter leads to the development of virtual laboratories and smart grids.

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