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Performance Analysis of 2N-N-2P Adiabatic Logic Circuits for Low Power Applications using FinFET

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Abstract

Novel area and energy efficient 2N-N-2P adiabatic logic with less leakage, switching noise and glitch free outputs is presented. FinFETs replace MOSFET for reduced short channel effects, lower leakage, less area and operating speeds. 2N-N-2P logic is validated using 32nm MOSFET and FinFET models and by comparison with 2N-2N2P and PFAL. FinFET circuits are compared with CMOS counterparts using benchmark inverters, Full adder, 512 inverter cascades and 4-bit CLA. The analyses also authenticate better performance under process parameter variations and demonstrate advantages of the use of FinFET for all the Evaluate, Hold and Recovery phases.

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Keywords: Adiabatic logic circuits; FinFET; Energy Recovery Circuits using FinFET;

1. Introduction

The growing demand for handy and portable devices steers the designer in opting for devices of smaller size and reduced transistor count towards realizing less silicon area. However, the high frequency of operations and the complex signal processing involved in high performance processors result in exponentially increasing power consumption. A unique logic design methodology, which is capable of reclaiming a part of energy from the nodal capacitance is popularly named as the Adiabatic or Energy Recovery Logic family. The adiabatic logic is broadly classified into two groups, namely, the quasi-adiabatic or partial energy recovery circuits and fully adiabatic circuits.

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Quasi-adiabatic logic design is a favorable choice of circuit design methodology for low power VLSI circuits since it consumes less energy consumption with tolerable circuit complexity design.Scaling the size of MOSFET has dramatically increased the performance and transistor density, which leads to the design of high speed and efficient IC. However, alarmingly increasing leakage current components are major drawbacks in such applications. Continuous shrinking of the source and drain diminishes the effective control of gate over the channel emphasizing the short channel effects such as drain induced barrier lowering and DIBL. The FinFET device replaces the traditional MOSFETs due to its design flexibility, superior capacity in regulating leakages, even while reducing the short channel effects. The FinFETs exhibit improved performance over the traditional MOSFETs due to their higher ON state current, effective control of the channel by a more efficient gate structure, resulting in lower leakage currents, reduction in short channel effects and fall in threshold voltages [1] [2].

The paper is organized as follows. Section 2 presents the overview of FinFET devices. Section 3 describes the FinFET based adiabatic logic buffer circuits. Section 4 presents the proposed novel 2N-N-2P adiabatic logic circuit. Power loss models of 2N-N-2P are discussed in Section 5 and design of Full adder using proposed circuit is detailed in Section 6. Section 7 presents the results of the simulations and discussions. Section 8 concludes.

Nomenclatures

L_{gate}	Channel Length, *n*m
H_{fin}	Fin height, *n*m
W_{fin}	Channel width, *n*m
T_{fin}	Fin thickness, *n*m
T_{ox}	Thickness of the oxide, *n*m
V_{thf}	Threshold voltage of the front gate, V
V_{thb}	Threshold voltage of the back gate, V
T_{box}	Thickness of the bulk oxide, *n*m
ε_{sib}	Permittivity of the bulk oxide, Fm^{-1}
ε_{ox}	Permittivity of the gate oxide, Fm^{-1}
I_{ds}	Drain to source current, A

2. Overview of FinFET

FinFET is a derived version of folded channel MOSFET. Structure of FinFET consists of a conducting channel enveloped by a “fin”. Fin is designed using thin silicon material. This acts as the body of the device. Source and drain are built at opposite terminals of the fin. This arrangement allows good control over the channel and hence short channel effects and leakage current are substantially reduced in FinFET when compared to the MOSFET. Effective channel length of the device is equal to the thickness of the fin. An additional gate in the FinFET device suppresses the short channel effects and improves the I_{on}/I_{off} ratios while increasing the electrostatic stability. Normally, the width of the gate is greater than the height of the fin, which wraps entirely over the fin [3].

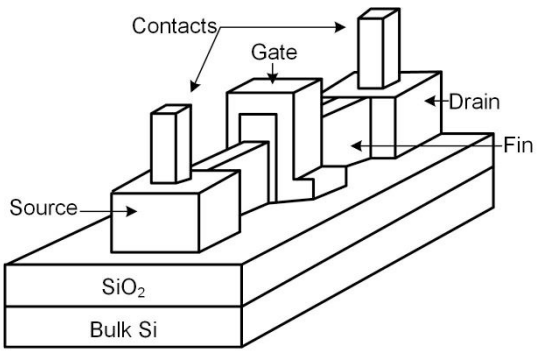

Fig. 1. Structure of FinFET

The three normally employed operating modes of the FinFET are 1) Shorted-gate mode (SG), 2) Reverse Bias or Low Power mode (RB) and 3) Independent Gate mode (IG). Figure 1 show the structure of FinFET model in 3D. The parameters associated with the FinFET are as follows. The L_{gate} is the channel length, H_{fin} is the fin height, W_{fin} is the channel width, T_{ox} is the thickness of the oxide, V_{thf} and V_{thb} are the threshold voltage of the front and back gates, ε_{ox} is the permittivity of the gate oxide and T_{box} is the thickness of the bulk oxide. Here, the H_{fin} is an important parameter, which makes the processing more complicated and this furthermore makes the device vulnerable for defects. Tables 1 and 2 show the primary parameters of the 32nm CMOS and FinFET PTM devices as made available in BSIMCMG.

Table 1. Primary Parameters of 32nm CMOS PTM models.

Device		Primary Parameters				
		L_{gate}	W_{fin}	T_{ox}	V_{thf}	ε_{ox}
CMOS	N-type	32nm	110nm	1.65e-9	0.508V	3.9
	P-type	32nm	100nm	1.75e-9	-0.45V	3.9

Table 2. Primary Parameters of 32nm FinFET PTM models.

Device		Primary Parameters							
		L_{gate}	H_{fin}	W_{fin}	T_{ox}	V_{thf}	V_{thb}	T_{box}	$\varepsilon_{sib}/\varepsilon_{ox}$
FinFET	N-type	32nm	40nm	80nm	1.4e-9	0.29V	0.29V	50µ	11.7/3.9
	P-type	32nm	50nm	100nm	1.4e-9	-0.25V	-0.25V	5x10e-7	11.7/3.9

3. FinFET based Adiabatic Logic Buffer Circuits

The conventional CMOS circuits do not recover the signal energy, and the power is dissipated in the pull-up and pull-down networks during the charging and discharging operations of the nodes, respectively. Hence, it leads to an inadvertent amount of the energy spent resulting in heat dissipation across the devices. In this direction, the energy recovery or adiabatic logic circuits find significant roles in low power applications and quantum computations. The adiabatic logic circuits are capable of providing substantial recovery of the energy stored at the capacitive output nodes during the energy recovery phase. In these circuits, the energy is supplied to the circuit nodes, or in other words, to the nodal capacitances of the circuit by the power-clock signal during the evaluation phase.

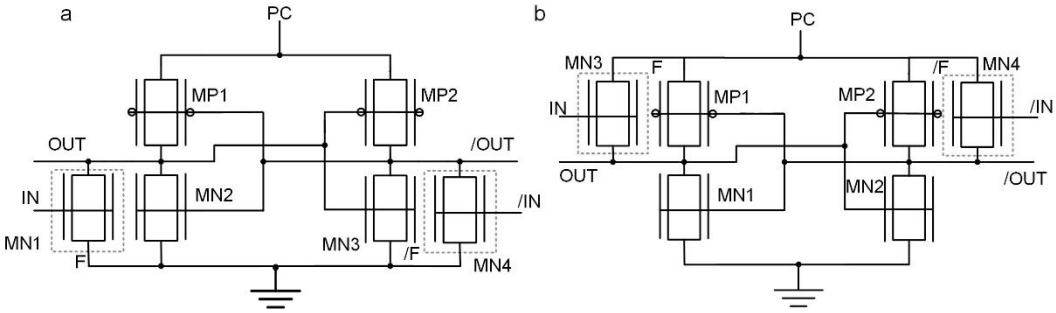

Fig. 2. (a) 2N-2N2P Adiabatic Logic Circuit; (b) PFAL Adiabatic Logic Circuit.

During the recovery phase, i.e., during the falling edge of the power clock, stored energy in nodes is recovered back from the nodal capacitances. The energy so recovered can be reused for subsequent computations [4]. The adiabatic buffer/inverter circuits designed using the 32nm FinFETs are shown in the Figures 2 (a) and (b) for the 2N-2N2P and PFAL [5] respectively. The dotted lines signify the FinFETs, which act as the functional block of the circuit. The double-gates are self-aligned to D/S and also with each other, which in effect reduces the resistance and the parasitic capacitance. Hence, the channel length can be controlled better [6].

4. 2N-N-2P Buffer Operation

The proposed circuit 2N-N-2P is shown in Figure 3(a). The dotted blocks in the logic circuit are the functional blocks. Any desired logic can be achieved by replacing with F and /F. During evaluation phase, when IN rises from 0 V and reaches the V_{th} of the nFin device, MN1 starts to conduct and this in turn pulls down the /OUT node low. /OUT is connected to the gate of the nFin device MN3 and pFin device MP2. This turns off MN3 and turns on MP2. OUT node is pulled up to PC (Power Clock). At this time /IN is low which turns off MN2 followed by MP1.

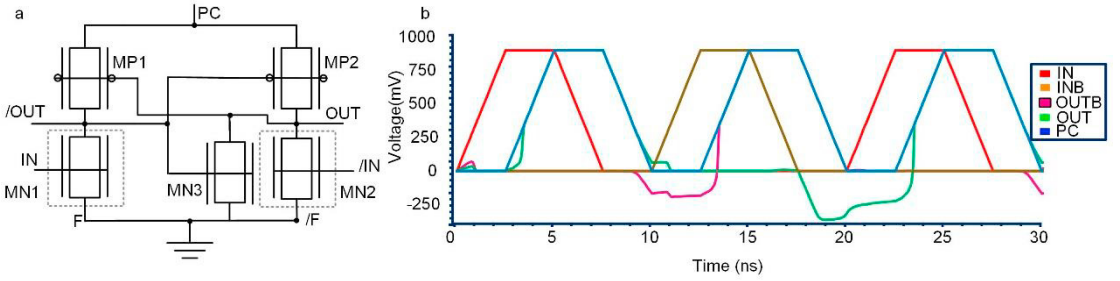

Fig. 3. (a) Proposed 2N-N-2P Adiabatic Logic Circuit; (b) 2N-N-2P Input-Output Transients.

During recovery phase, when the PC ramps down to a low value. MP2 which is still ON, creates a recovery path from OUT node to PC. This process persists until the power clock voltage is more than the V_{th} of the pFin MP2. MP2 remains off after this condition. Similarly, when MN2 is switched ON as /IN rises from 0V and reaches V_{th}, OUT node is pulled down to ground and this is connected to the gate of MP1. Hence, MP1 is switched ON and /OUT follows PC. This in turn is connected to the gate of MN3. MN3 is switched ON when PC rises above V_{th} of the device. During recovery, MP1 creates a recovery path from /OUT to PC till PC voltage is greater than V_{th} of the pFin MP1 device. Floating output node problem is minimized to a greater extent with less number of transistors when compared with the existing adiabatic logic circuits. Figure 3(b) shows the input output transients of 2N-N-2P.

5. Power Loss Models of 2N-N-2P Adiabatic Logic

Power loss of 2N-N-2P is the sum of the power loss due to adiabatic and non-adiabatic power. Non-adiabatic power loss models of 2N-N-2P are formulated due to the following reasons: 1) Dissipation by the latch formation, 2) Leakage current and 3) Incomplete charge recovery.

1) When the input remains same as the previous cycle, then one of the output nodes is connected to the ground while the other rises from $V_{th,p}$ to the V_{dd}. When there is a need for the change in the output as per input switching, $V_{th,p}$ discharges to the ground. The energy dissipated at this point is equal to $^1/_2\, C_L V_{tp}^2$.
2) Leakage component is mainly due to the subthreshold leakage current. When IN is HIGH and power clock remains in '0', no leakage occurs in MP1 and MP2. During evaluation phase, when PC rises from 0V and crosses the threshold voltage $V_{th,n}$ leakage occurs along the path MP1, MN3 and MN2. During the hold phase, leakage along MN2 and MP2 are low by the very nature of FinFETs. During the recovery phase, leakage current is small due to falling PC voltage. Figure 4 shows the energy components of 2N-N-2P.
3) Incomplete charge recovery at node OUT can happen when PC voltage is lower than the pFin MP2, and a floating output node can prevail during that point of time. Assuming that /IN goes High during the next cycle, node OUT will be shorted to Gnd through the conducting MN3 and MN2. Note that MN3 conducts with High level /OUT input connected to its gates.
4) Figure 4 shows the energy dissipation behaviour during subsequent cycles when the inputs are assumed to be alternating between logic 0 and 1. Due to the fact the OUT and /OUT nodes incur different nodal capacitances due to diffusion and the number of device terminals connected at the node, the energy dissipation and recovery vary accordingly.

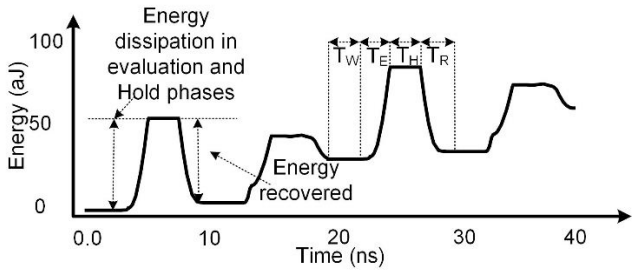

Fig. 4. Energy components of 2N-N-2P.

6. Design flow of 2N-N-2P

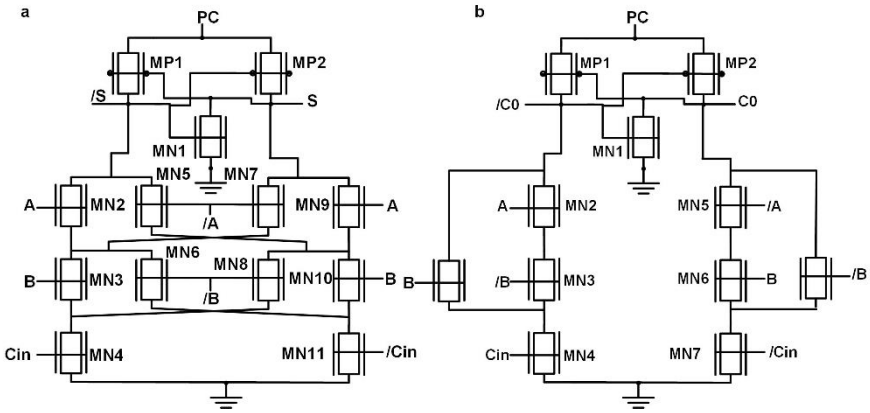

Fig. 5. (a) 2N-N-2P Logic Sum block and; (b) 2N-N-2P Logic Carry block of Full Adder Input-Output Transients.

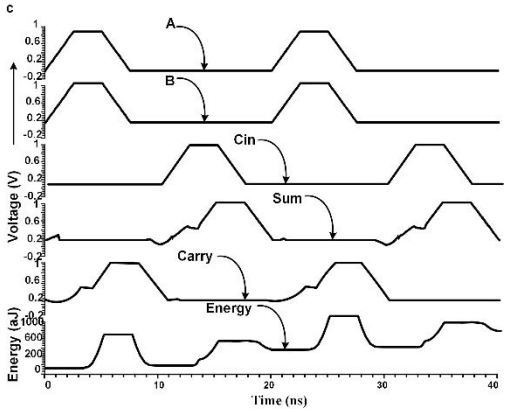

Fig. 5. (c) A, B, C_{in} and Sum, Carry signal transients of 2N-N-2P logic Full Adder. .

A one bit full adder is designed using the proposed 2N-N-2P adiabatic logic with three complimentary inputs A, B and Cin. The corresponding sum and carry outputs along with their complements are S, /S, C0 and /C0. Figures 5(a) and (b) show the sum and carry structure of a full adder designed using the 2N-N-2P adiabatic logic structure. Consider inputs *A, B, Cin* are HIGH. Then, MN2, MN3, MN4 become ON and pull down the node */S* to ground and S is disconnected from the ground. During evaluation phase, when the power clock ramps up, latch pulls up the *S* node to a higher value. Hence, when all the inputs of the full adder is HIGH, sum and carry outputs are high. When *A, B, Cin* are LOW, output *S* is pulled down to ground through MN11, MN6, and MN7. This turns on MP1 and the

PC gets connected to */S*. During the recovery phase, when PC falls down from V_{dd} to ground, the charge stored in output load capacitances flow back to PC through MP1 and MP2. Figure 5(c) exhibits the inputs and output transients. When input *A* and *B* are HIGH and *C* is LOW, Sum is LOW and Carry is HIGH. Energy dissipation for the corresponding input-output is also shown. 2N-N-2P utilizes 16.05nJ energy, which is very less when compared with the other adiabatic logic families.

7. Results and Discussion

In this section, various analyses have been made for proving the efficiency of the proposed 2N-N-2P. Figure 6 compares the power dissipation of 2N-N-2P inverter against CMOS inverter across a range of frequencies.

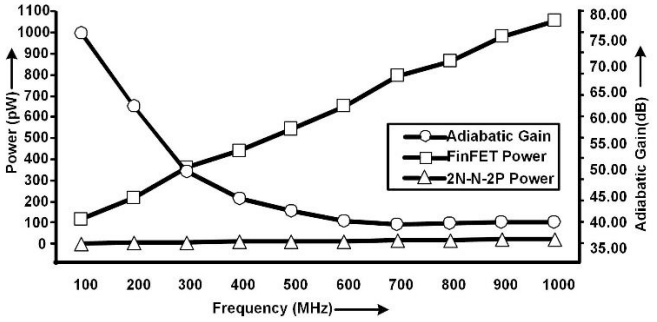

Fig. 6. Power dissipation of 2N-N-2P and FinFET based inverters and the adiabatic gain of 2N-N-2P.

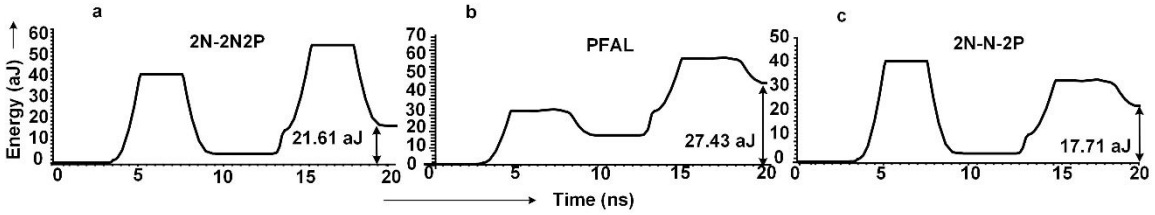

Fig. 7. Energy Comparison of (a) 2N-2N2P (b) PFAL and (c) 2N-N-2P at 100MHz frequency.

Adiabatic gain factor which is the ratio between the power dissipation values incurred by the conventional FinFET gate against the 2N-N-2P based adiabatic logic gate, across a frequency band of 100MHz to 1GHz was found to be from 75.7dB at 100MHz to 39.8dB at 1GHz. However, the FinFET power rises linearly with the increase in the frequency up to 1GHz. However, 2N-N-2P acquires better control over the non-adiabatic power components and hence results in moderate rise in power. Figure 7 presents energy comparison for buffers designed using 2N-2N2P, PFAL and 2N-N-2P. 2N-2N2P and PFAL at 100MHz has an energy of 21.61aJ and 27.43aJ respectively. 2N-N-2P consumes an energy of 17.71aJ which is too less when compared with the energy of other adiabatic circuits. Table 3 depicts the comparisons made among the power dissipation incurred by the adiabatic logic families under consideration, which have been designed using CMOS and FinFET device counterparts individually. The proposed 2N-N-2P CMOS adiabatic circuit utilizes 38.66 nW, while the 2N-N-2P logic circuit constructed using the FinFET device counterparts consume 1.39aW of power.

Figures 8 (a) to (c) present the energy dissipation during the Evaluate, Hold and Recovery phases of the FinFET based adiabatic circuits. The 2N-N-2P circuit operates efficiently with very low energy dissipation, of the order of 2.01E-21J while operating at 0.9V and 500MHz frequency. This is much lower than 2.52E-18J and 9.27E-19J of 2N-2N2P and PFAL adiabatic logic circuits, respectively, operating at 0.9V and 500MHz. Table 4 depicts the energy dissipation of buffer/inverter counterpart circuits across a range of frequencies. It can be observed that 2N-N-2P logic dissipates very less compared to 2N-2N2P and PFAL circuits. The proposed 2N-N-2P dissipates 1.126fJ, while the 2N-2N2P and PFAL utilise 32.27fJ and 35.67fJ respectively at 1GHz.

Table 3. Power dissipation comparison of the adiabatic buffer logic.

Adiabatic Logic Family	CMOS Power (nW)	FinFET Power (aW)
2N-2N2P	44.26	2.029
PFAL	45.18	2.26
2N-N-2P	38.66	1.39

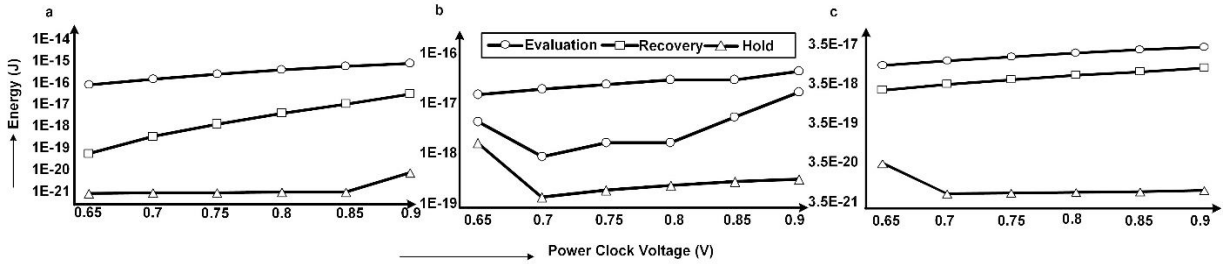

Fig. 8. Energy dissipation in various phases of operation in (a) 2N-2N2P, (b) PFAL and (c) 2N-N-2P FinFET Adiabatic circuits.

Table 4 Energy dissipation of various adiabatic buffer logic across a range of frequency.

Frequency(MHz)	Energy Dissipation(fJ)		
	2N-N-2P	2N-2N2P	PFAL
10	0.01522	1.15	1.203
100	0.1165	2.392	2.474
200	0.2478	3.781	3.885
500	0.608	17.62	17.6
800	0.9641	30.17	31.52
1000	1.126	32.27	35.67

Table 5. Power and Energy dissipation of 512 cascaded inverters designed using various adiabatic logic families.

Adiabatic Logic Family	Power (W)	Energy(J)
2N-2N2P	1.71E-6	3.77E-14
PFAL	2.31E-5	1.38E-13
2N-N-2P	8.78E-7	7.82E-15

Table 5 shows the power and energy dissipation of cascaded 512 inverters designed using 2N-2N2P, 2N-N-2P and PFAL at 500MHz frequency and 0.9V. 2N-N-2P incurs 3.77E-14J whereas 2N-2N2P and PFAL utilises 1.38E-13J and 7.82E-12J respectively. Figure 9 depicts the energy dissipation of full adder designed using 2N-N-2P, 2N-2N2P and PFAL operating at 500MHz frequency and 0.9V. It is clear from the graph that the 2N-N-2P dissipates less energy when compared with 2N-2N2P and PFAL full adders. Table 6 shows the power dissipation of Carry Lookahead Adder designed using 2N-2N2P, PFAL and 2N-N-2P at 500MHz frequency and 0.9V. CMOS based 2N-N-2P incurs 8.317E-6W whereas 2N-2N2P and PFAL utilizes 10.84E-6W and 12.06E-6W respectively.

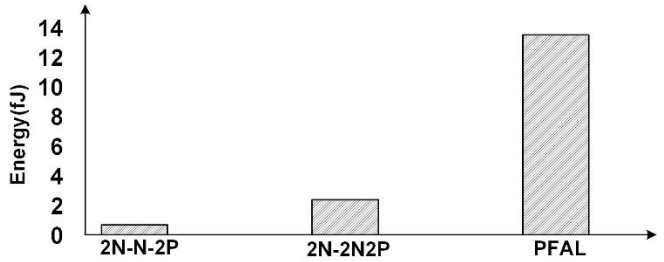

Fig. 9. Energy dissipation of FinFET based full adders designed using 2N-N-2P, 2N-2N2P and PFAL

Table 6. Power dissipation of 4 bit Carry Lookahead Adder designed using various adiabatic logic families.

Adiabatic Logic Family	CMOS Power (W)	FinFET Power(W)
2N-2N2P	10.84E-6	4.308E-6
PFAL	12.06E-6	6.233E-6
2N-N-2P	8.317E-6	2.608E-6

8. Conclusion

In this paper, the FinFET based 2N-N-2P adiabatic logic circuit has been proposed. This logic dissipates comparatively very less energy, which is realized by the low leakage current and lower device counts employed in the design. Elimination of one of the floating nodes that leads to incomplete charge recovery from the particular node reduces the leakage current and charge sharing issues. Furthermore, the 2N-N-2P logic achieves less power dissipation with respect to device count, low leakage current and improved charge recovery capability.

Validation of the proposed logic is carried out by comparing the design against 2N-2N2P and PFAL inverter/buffer circuits designed using both MOSFET and FinFET. The FinFET based 2N-N-2P inverter circuit dissipates 31% and 38% lower power than the 2N-2N2P and PFAL inverter circuits, respectively. Furthermore, the 2N-N-2P CMOS based inverter circuit dissipates 12% and 14% lower power when compared with CMOS based 2N-2N2P and PFAL inverter circuits, respectively. Elimination of floating output node in 2N-N-2P transforms it as one of the enhanced energy recovery circuits in low power VLSI design. The application of FinFET for the widely-discussed CMOS based adiabatic circuits has been analyzed and the advantages of the use of FinFET over CMOS have been highlighted.

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