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Original Article

Performance analysis of HfO_2/InAlN/AlN/GaN HEMT with AlN buffer layer for high power microwave applications

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We present a performance enhancement evaluation of n + doped graded InGaN drain/source region-based HfO_2/InAlN/AlN/GaN/AlN on SiC metal-oxide-semiconductor high electron mobility transistor (MOS-HEMTs) with a T-shaped gate. Impact on the device characteristics with the inclusion of a HfO_2 surface passivation layer and an AlN buffer layer in the MOS-HEMT structure as a performance booster has been analyzed for the HEMT device with 30 nm gate length using Silvaco ATLAS TCAD. The proposed MOS-HEMT exhibits an outstanding performance, with an enhanced power gain cut-off frequency (f_{max}) of 366 GHz, a current gain cut-off frequency (f_t) of 426 GHz, and a off-state breakdown voltage (V_{br}) of 81 V. The high-*k* (high permittivity) HfO_2 based metal oxide semiconductor HEMT device experiences a low off-state gate leakage current ($I_g \sim 10^{-11}$A/mm) and a high I_{on}/I_{off} ratio of 10^9. The InAlN/GaN/AlN heterostructures demonstrate improved two-dimensional electron gas (2DEG ~ 5.3×10^{13} cm^{-2}), carrier mobility (μ) of 1256 Cm^2/V-s and drain current density of (I_{ds}) 2.7 A/mm. A large signal analysis performed at 30 GHz yielded a maximum of 28% power-added efficiency. The high JFoM of 34.506 THz V (Johnson Figure of Merit = $f_t \times V_{br}$) and $(f_t.f_{max})^{1/2}$ of 394.86 GHz indicate the potential applicability of the HfO_2/InAlN/GaN MOS-HEMTs in high-frequency and high-power applications.

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1. Introduction

III-Nitride based power transistors are attractive devices for millimetre-wave high-power and high-frequency applications. AlGaN/GaN-based high electron mobility transistors have demonstrated an outstanding power performance of 30 W/mm at 4 GHz [1]. Recent challenges in III-Nitride based HEMT are their poor operating frequencies in sub-millimeter wave frequencies for satellite, advanced radars, and broadband wireless communications. The realization of ultrathin-barrier based AlGaN/GaN heterostructures has remained a challenging task because of surface depletion effects [2] and physical damage in the recessed gate [3]. To achieve high frequency and high voltage operation of GaN-based HEMTs, a trade-off between current gain cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) for breakdown voltage must be considered. $In_{0.17}Al_{0.83}N$/GaN-based lattice-matched heterostructures have demonstrated a stronger polarization, good thermal stability, and a high drain current density [4–6]. InAlN barrier based III-Nitride HEMT possessed cut-off frequencies (f_T and f_{max}) of more than 300 GHz [7]. Ultra scaled InAlN barrier layer (3 nm) based HEMTs have shown an excellent thermal stability [8] and InAlN/GaN-based HEMTs reported in the last decade, reached a 5 W/mm output power at 35 GHz [9] and 40 GHz [10].

In spite of the remarkable improvement in the operating frequency, InAlN based HEMTs suffer from leakage currents and low breakdown voltage [11], severe short channel effects, and contact

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resistances [12]. In particular, InAlN based HEMTs have shown high buffer leakage currents at high temperatures. InAlN/GaN HEMT on SiC substrate has shown the higher performance compared to HEMTs on other substrates. Despite the high-frequency performance of GaN-based HEMT demonstrated in refs [13,14], the devices experienced severe short channel effects and gate leakage current for the sub-50 nm gate length. Several research groups have investigated metal oxide semiconductors high electron mobility transistors (MOS-HEMTs) using various oxide layers such as SiO2, Al_2O_3, HfO_2, MgCaO and La_2O_3 for improving the device performance by suppressing gate leakage currents [15–22].

At high drain bias, the device performance gets degraded from its dynamic on-resistance, also known as current collapse and surface traps, which act as a "virtual gate" in the gate to drain access region. This prevents a proper operation of the device and reduces the available current swing as well as degrades the knee voltage [23]. For the nano-scale device dimension, the device experiences more current collapse due to the reduced gate-drain distance, which magnifies the surface traps effects. It is also very difficult to maintain uniform electric field distribution between the drain and gate space for obtaining a proper breakdown voltage as the device dimension scaled-down. A field plate gate structure effectively reduces the dispersion phenomena [24]. The field plate structure reduces the current collapse and enhances the breakdown voltage of the device by maintaining a low electric field at the gate to drain edge [25]. However, the field plate increasing the parasitic capacitance (C_{gd}), indicates the high-frequency performance (the current gain cut-off frequency f_t and the power gain cut-off frequency f_{max}) of the device are limited due to $(R_s + R_d)C_{gd}$ parasitic charging delay [26–28]. Therefore, the field plate technique limits the design of power amplifiers and MMICs for high-frequency bands such as V and W bands.

The objective of this work is to optimize the device structure for a simultaneous improvement of f_t/f_{max} and the breakdown voltage (V_{br}). In this article, we propose a T-gate HfO_2/InAlN/GaN/AlN on SiC substrate. The device surface is passivated by a high-*k* HfO_2 layer for improving the breakdown voltage of the device by reducing the parasitic capacitance (C_{gd}). The graded InGaN n + source/drain region reduces the contact resistances. Introduction of high-*k* (high permittivity) passivation layer smoothens the electric field between the drain and the gate access region. The introduction of the AlN back-barrier suppresses the off-state subthreshold gate and drain leakage currents, thereby enhancing the breakdown voltage of the device.

2. HfO_2/InAlN/GaN/AlN MOS-HEMT device description and band diagram

The cross-section view of the proposed HfO_2/InAlN/AlN/GaN MOSHEMT is shown in Fig. 1(a). The MOSHEMT consists of 350 nm AlN buffer, 30 nm GaN channel, 6 nm $In_{0.13}Al_{0.83}N$ barrier and 3 nm high dielectric constant HfO_2 as an oxide layer (*k*~20–25). The HfO_2 oxide layer is used in this MOS-HEMT for controlling the gate leakage current and for the high breakdown voltage [29]. The near lattice-matched $In_{0.13}Al_{0.83}N$/GaN heterostructures offer a high two-dimensional electron gas density with high mobility [30]. An 1 nm AlN wide-bandgap (6.02 eV) spacer layer is sandwiched between the barrier and channel layer for improving the electron concentration in the two-dimensional electron gas (2DEG). The alloy scattering is lowered because of the AlN binary compound and also the quantum well depth is increased. As a result, the electron mobility in the channel is increased, thus improving the current [31]. The large bandgap AlN binary compound used as a buffer in this work, which provides larger polarization fields and an effective band offset, allowing for the aggressive scaling of the device dimensions and maximum 2DEG confinement, as compared to a conventional GaN or an AlGaN buffer. The high thermal conductivity (~340 W/mK) of AlN provides a good thermal management [32]. A 50 nm graded n + InGaN (Si ~ 2×10^{19} cm^{-3}) source and the drain region are formed for low contact resistances. A distance between the source and the drain is 270 nm, and a Ti/Au (50/50 nm) metal stack is used as ohmic contacts. A T-shaped gate with 30 nm foot length (L_g) and 2×20 μm gate width (w), 140 nm stem height and 400 nm head size is designed, which lift-off a wide cross-sectional gate area with small gate lengths for alleviating the gate access resistance [33], and Schottky contact is made for the gate using a Ni/Au (50/50 nm) stack. A 40 nm HfO_2 passivation layer is deposited over the device surface for low parasitic capacitances. A high ~ *k* passivation layer unfastens the dispersion effects which provides a root to achieve the good transport property in the 2DEG.

A TCAD simulation-based energy band diagram is shown in Fig. 1(b). As shown in the band diagram, the InAlN/AlN/GaN/AlN quantum well creates a high conduction band-offset and increases the quantum well depth for formation at the top of AlN/GaN heterojunction. The high-*k* HfO_2 insulating layer creates a 2.3 eV conduction band-offset (CBO) with InAlN, which helps in suppressing the gate leakage current more effectively as compared to other low-*k* insulator based MOS-HEMTs. AlN back-barrier mitigates the buffer leakage currents by offering large barrier height. At room temperature the simulation results have shown 2DEG (n_s) of 5.3×10^{13} cm^{-2} and carrier mobility (μ) of 1256 $cm^2V^{-1}s^{-1}$ for the proposed HEMT structure.

3. Results and discussion

The drain current (DC) characteristics of the 30 nm gate length HfO_2/InAlN/GaN/AlN based heterostructure are shown in Fig. 2(a). The simulated device delivers a peak current density of 2.7 A/mm for $V_{gs} = 0$ V. The output conductance (g_{ds}) of 35 mS/mm extracted from the saturation region of the output characteristics. The obtained result is superior to that of a rectangular gate SiO_2/InAlN/GaN HEMT without back-barrier structure [34], as shown in Fig. 2(b). The simulation results for the transfer characteristics of the proposed HfO_2/InAlN/GaN/AlN HEMT and the experimentally fabricated SiO_2/InAlN/GaN MOS-HEMT [34] are shown in Fig. 3(a) and Fig. 3 (b), respectively. The extracted threshold voltage (V_{th}) of the proposed HEMT device is −5.8 V from the linear scale plot. At $V_{ds} = 3$ V, the proposed T-gate HfO_2/InAlN/GaN/AlN HEMT yielded 2.5 A/mm at a zero gate bias, whereas the 1.7 A/mm drain current density was demonstrated by a rectangular gate SiO_2/InAlN/GaN MOS-HEMT without back-barrier [34].

High power operation of the nano-scale III-Nitride at millimetre-wave spectrum can be ensured by suppressing the leakage currents in the device. This prevents the device from sub-optimal breakdown and helps the device achieve a higher breakdown voltage. Buffer leakage current is reduced by the AlN blocking layer (buffer) and HfO_2 high-*k* gate dielectric minimizes the gate leakage current. The proposed HfO_2/InAlN/GaN/AlN MOS-HEMT breakdown analysis is shown in Fig. 4. The device exhibited an off-state breakdown voltage of 81 V for L_g ~30 nm. Rectangular gate SiO_2/InAlN/GaN MOS-HEMT without back-barrier exhibited a 61 V breakdown voltage for L_g ~30 nm.

The off-state leakage current for the proposed ultra scaled HfO_2/InAlN/GaN/AlN MOS-HEMT is reduced to ~10^{-11} A/mm using a high-*k* dielectric HfO_2 insulator, as shown in Fig. 5(a) and a subthreshold slope (SS) of 35 mV/decade is extracted from the log-scale plot at $V_d = 3$ V and V_g swept from −6 V to 0 V. A good I_{on}/I_{off} ratio of 10^9, which is superior to that of a conventional GaN channel based MOS-HEMT [34] shown in Fig. 5(b), resulting from the ultra-thin InAlN barrier (6 nm) with AlN superlative back-

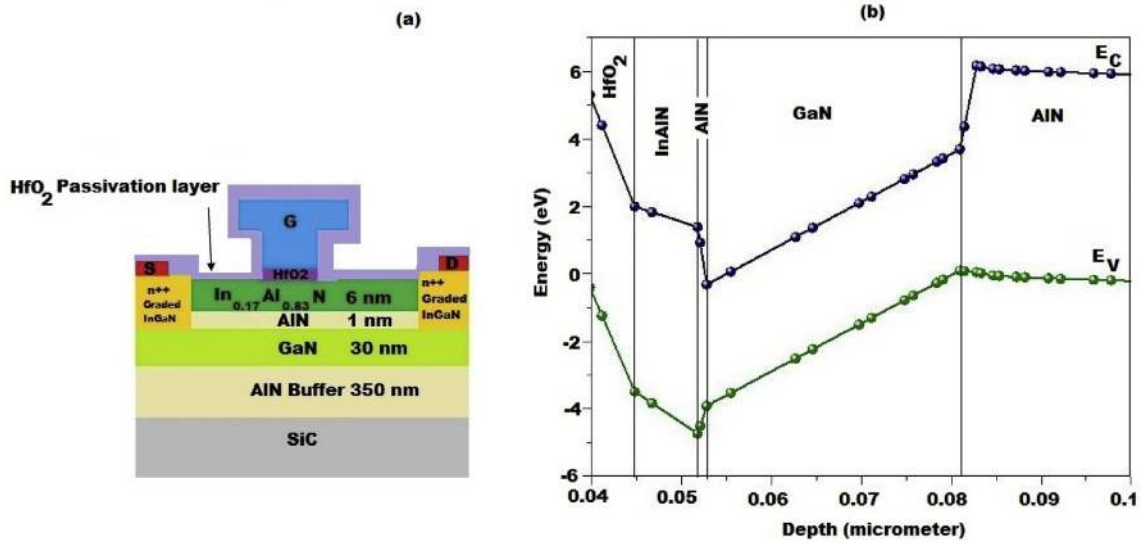

Fig. 1. (a). A HEMT structure; (b) Bandgap diagram.

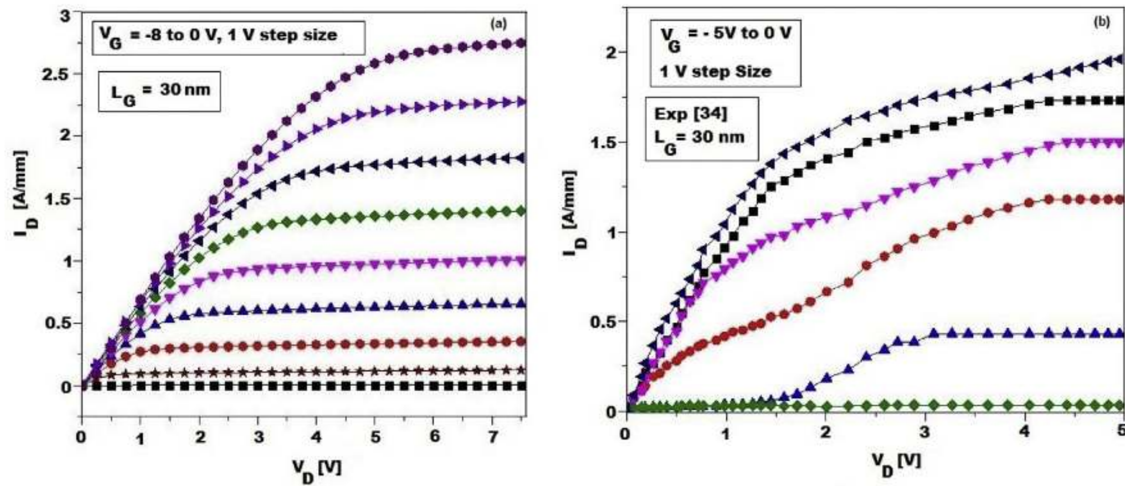

Fig. 2. (a) Drain current characteristics of the proposed HfO_2/InAlN/GaN/AlN MOS-HEMT. (b) Drain current characteristics of the experimentally reported SiO_2/InAlN/GaN MOS-HEMT [34].

barriers. Whereas, the rectangular gate structure SiO_2/InAlN/GaN MOS-HEMT without back-barrier [34] experienced an off-state gate leakage current of ~10^{-7} and I_{on}/I_{off} ratio of 10^7 [34].

Despite tremendous research progresses that have been made during recent years, further increasing the frequency of the GaN-based HEMT for next-generation high speed and high power sub-millimeter wave device applications is still needed. The current gain frequency (f_t) and the power gain (f_{max}) cut-off frequency of the FET are expressed as follows [35]:

$$f_t = \frac{\frac{g_m}{(2\pi)}}{\left[C_{gs} + C_{gd}\cdot\left[1 + \frac{R_s+R_d}{R_{ds}}\right] + C_{gd}.g_m.(R_s + R_d)\right]} \tag{1}$$

$$\tau = \frac{1}{2\pi f_t} = \frac{C_{gs} + C_{gd}}{g_m} + C_{gd}.(R_s + R_d).\left[1 + \left(1 + \frac{C_{gs}}{C_{gd}}\right)\frac{g_{ds}}{g_m}\right] \tag{2}$$

$$f_{max} = \frac{f_t}{2\sqrt{(R_s + R_g)g_{ds} + 2\pi f_t R_g C_{gd}}} \tag{3}$$

For high power gain with high-frequency operation, f_{max} is a primary source. For enhancing f_{max}, the parasitic resistances such as gate resistance (R_g), drain resistance (R_d), source resistance (R_s), gate to drain capacitance (C_{gd}), and gate-source capacitance (C_{gs}) need to be reduced.

An ultra-scaled device with the T-gate HfO_2/InAlN/GaN/AlN heterostructure with HfO_2 passivation is beneficial for enhancing transconductance and high-frequency operation of GaN-based HEMTs by minimizing the parasitic resistances (R_g) and capacitances (C_{gs} + C_{gd}). The simulation result of the transconductance variation with gate bias is displayed in Fig. 6 (a) and the maximum of 0.92 S/mm reached at $V_g = -1.8$ V, whereas, the rectangular gate structure SiO_2/InAlN/GaN MOS-HEMT without back-barrier recorded 0.653 S/mm [34] is depicted in Fig. 6 (b).

The extracted parameters from the small-signal equivalent circuits of HEMT, transconductance (g_m), drain conductance (g_{ds}),

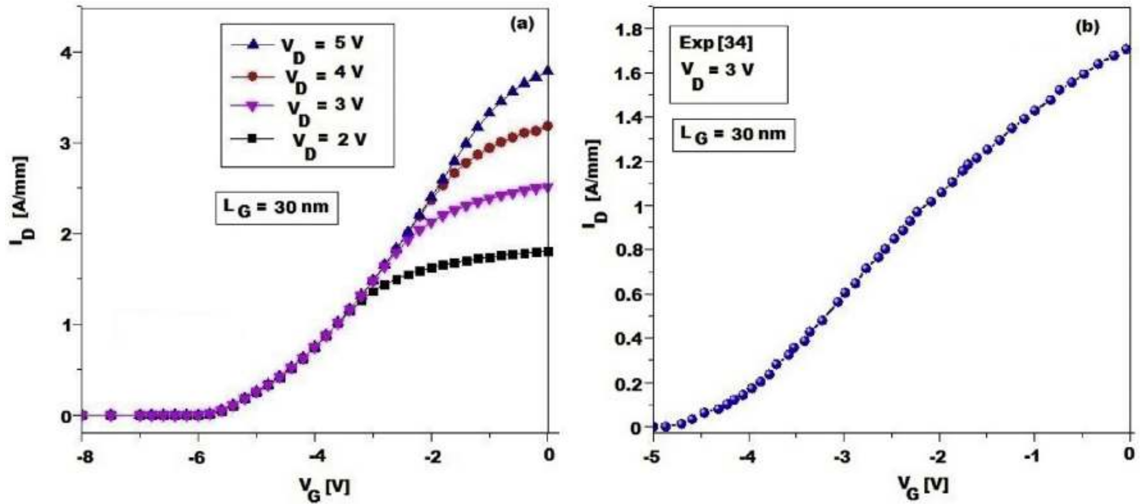

Fig. 3. (a) Transfer characteristics of the proposed HfO_2/InAlN/GaN/AlN MOS-HEMT; (b) Transfer characteristics of the experimentally reported SiO_2/InAlN/GaN MOS-HEMT [34].

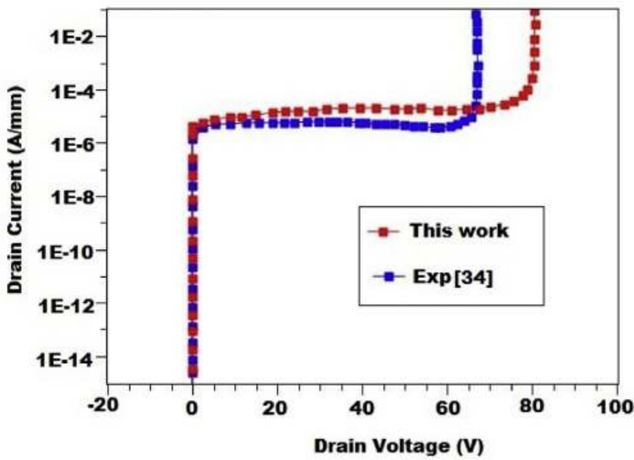

Fig. 4. Simulation result of the breakdown characteristics of the proposed HfO_2/InAlN/GaN/AlN MOS-HEMT in comparison with the breakdown characteristics of SiO2/InAlN/GaN MOS-HEMT [34].

gate-source capacitance (C_{gs}), gate-drain capacitance (C_{gd}), source resistance (R_s), drain resistance (R_d), Sheet resistance (R_{sh}) and on resistance (R_{on}) of the 30 nm T-gate HfO_2/InAlN/GaN/AlN MOS-HEMT with n + source and drain regions are 0.92 S/mm, 35 mS/mm, 572 fF/mm, 84 fF/mm, 0.12 Ω-mm, 0.15 Ω-mm, 421 Ω/sqr and 0.32 Ω-mm, respectively.

The small-signal gain characteristics of the T-gate HfO_2/InAlN/GaN/AlN MOS-HEMT is displayed in Fig. 7(a) at a peak g_m gate bias. A maximum cut-off frequency f_t/f_{max} of 426/366 GHz obtained by extrapolating current gain and power gain. The rectangular gate structure SiO_2/InAlN/GaN MOS-HEMT without back-barrier demonstrated f_t/f_{max} of 400/33 GHz [34], as shown in Fig. 7(b).

The large-signal analysis of the T-gate HfO_2/InAlN/GaN/AlN MOS-HEMT is performed for 30 GHz, and the corresponding input power (dBm), output power (dBm), and power gain (dB) relationship are displayed in Fig. 8(a). The rectangular gate structure SiO_2/InAlN/GaN MOS-HEMT large-signal characteristics are also displayed in Fig. 8(b) for comparison.

The power-added efficiency (PAE) (%) variation with input power is displayed in Fig. 9 for the T-gate HfO_2/InAlN/GaN/AlN MOS-HEMT. Simulation results show that the maximum power-added

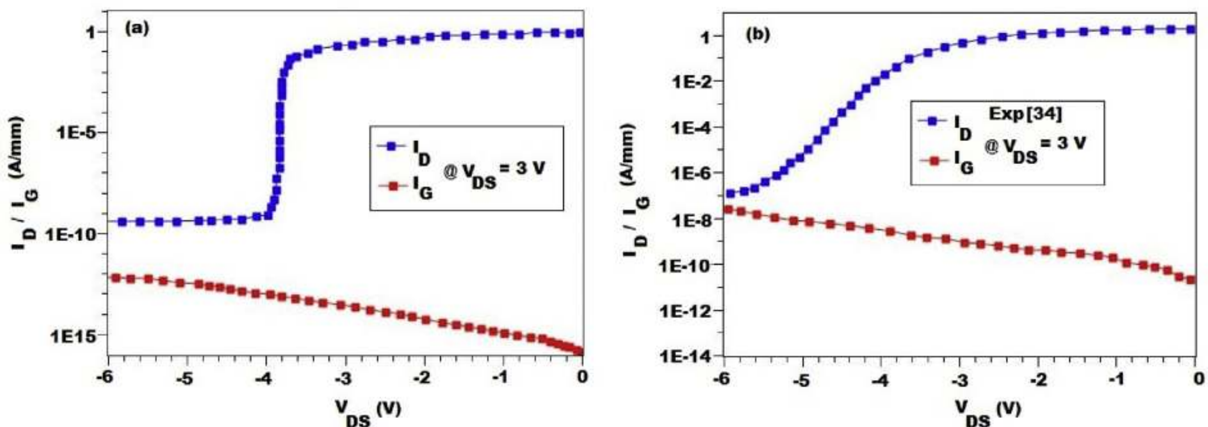

Fig. 5. (a) Gate leakage and drain leakage current characteristics of the proposed HfO_2/InAlN/GaN/AlN MOS-HEMT. (b) Gate leakage and drain leakage current characteristics of the experimentally studied SiO_2/InAlN/GaN MOS-HEMT [34].

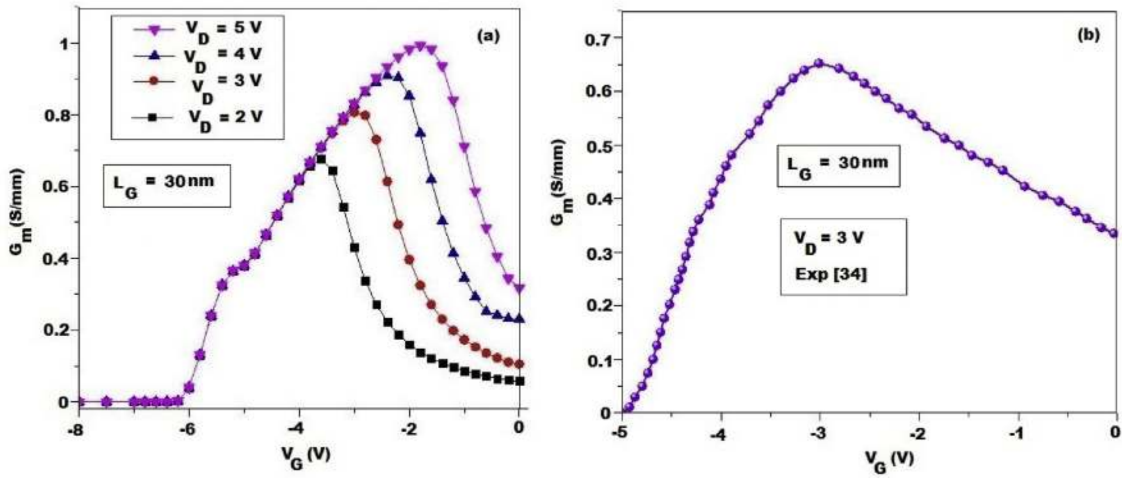

Fig. 6. (a) Transconductance variation with gate bias for the proposed HfO_2/InAlN/GaN/AlN MOS-HEMT. (b) Transconductance variation with gate bias for the previously reported SiO_2/InAlN/GaN MOS-HEMT [34].

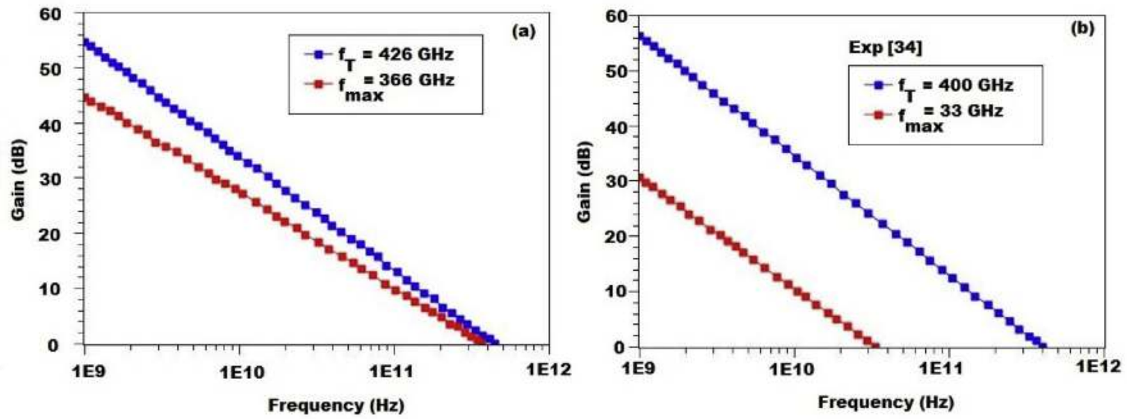

Fig. 7. (a) Small-signal characteristics of the proposed HfO_2/InAlN/GaN/AlN MOS-HEMT. (b) Small-signal characteristics of the experimentally reported SiO_2/InAlN/GaN MOS-HEMT [34].

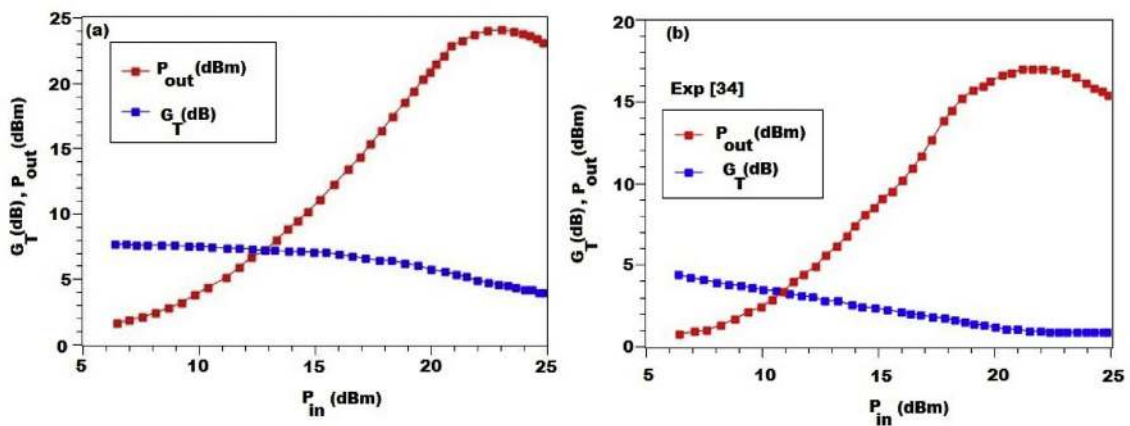

Fig. 8. (a) Large-signal performance of the proposed HfO_2/InAlN/GaN/AlN MOS-HEMT. (b) Large-signal performance of the SiO_2/InAlN/GaN MOS-HEMT [34].

efficiency of 28% demonstrated by the proposed MOS-HEMT. 21% of power added efficiency (PAE) was obtained from the SiO_2/InAlN/GaN MOS-HEMT [34].

The proposed T-gate HfO_2/InAlN/GaN/AlN MOS-HEMT enables very low output conductance (g_{ds}), suppressed short channel effect (SS), good I_{on}/I_{off} ratio, improved breakdown voltage (V_{br}), low

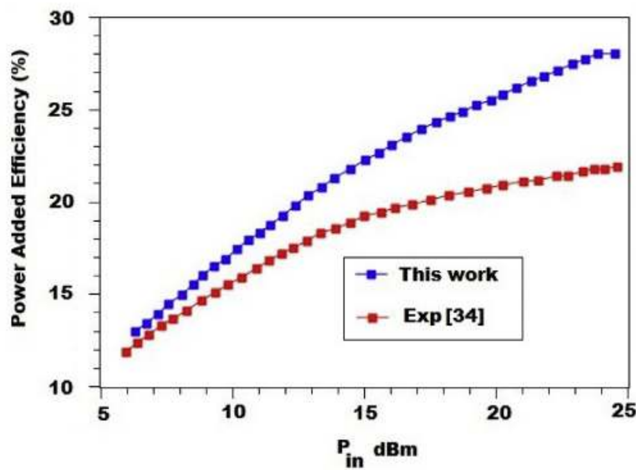

Fig. 9. Power added efficiency of the proposed HfO_2/InAlN/GaN/AlN MOS-HEMT in comparison with that of SiO_2/InAlN/GaN MOS-HEMT [34].

leakage current (I_g), and a significant improvement in small signal and large signal characteristics. Moreover, the current collapse and kink effects are not found in the DC characteristics of the proposed MOS-HEMT. The cut-off frequencies are enhanced by T-shape with a tall stem gate structure, which offered additional gate structure and reduced gate resistance and capacitance.

4. Conclusion

The HfO_2/InAlN/AlN/GaN MOS-HEMT for high power millimetre-wave applications has been proposed, and its DC, RF and high power characteristics have been analyzed using the physics-based Silvaco ATLAS TCAD. The T-gated InAlN/GaN HEMT with AlN back-barrier improves the device performance as a result of the enhanced breakdown, small-signal and large-signal characteristics. The optimized device structure achieved the high current density, low leakage current and high I_{on}/I_{off} ratio. The power and frequency characterization of the device proved its exemplary performance through the achievement of the excellent off-state breakdown voltage of 81 V, and f_t/f_{max} of 426/366 GHz. The large signal analysis of the HEMT stack performed at 30 GHz yielded a maximum power-added efficiency of 24%. The high-performance simulation results (JFoM = 34.506 THz V and $(f_t.f_{max})^{1/2}$ = 394.86 GHz) indicate that the proposed HfO_2/InAlN/GaN/AlN based III-Nitride HEMT is a suitable device for modern high power millimeter-wave electronics.

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