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Power Domain, Physical Aware Scan Chain Allocation and Reordering

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Abstract

Objectives: An algorithm is proposed to allocate the scan cells to form a particular set of scan chains. The proposed algorithm reduces wire length and number of multi-voltage cells. This also maintains the balance of the chain. **Methods**: The proposed algorithm was implemented in Tool Command Language (TCL) and it works on the post placed database. The developed algorithm was tested on some of the industrial designs. **Findings:** The proposed algorithm was tested on some of the industrial designs and a reduction was observed in the scan chains wire length (about 10%) and a much greater reduction in the count of the lockup latches (about 90%). **Improvements/Applications**: This will ensure a reduction in congestion as well as reduced area requirements.

Keywords: Design for Testability (DFT), Multi-Domain Mixing, Scan Allocation, Scan Segments

1. Introduction

Structured DFT methods are used for the purpose of controlling and observing the internal states of the sequential circuits[1]. Using the ad-hoc approaches it takes exponential number of clock cycles to check the internal states through the external pins. Scan designing is the most popular structured DFT technique used. In scan design, the normal Flip-Flops (FF) are reconfigured to form scan cells. Two sources of inputs are presented for a scan cell[2]: 1. The output of the combinational logic (functional input) and 2. The output of the preceding scan cell in the chain. The output of the scan cell can have either two separate functional pins or a pin with merged functions. The two pins are: 1. A functional output pin and 2. A scan output pin which will be connected to the subsequent scan flop.

There are three functional modes in scan operations: 1. Normal; 2. Shift and 3. Capture mode. In normal operating mode, all the test signals are disabled whereas in other two modes test signals are enabled. Shift operation mode connects the scan FFs as a chain, the scan enable is high and the required inputs can be shifted into the scan FFs. Capture mode forces the shifted inputs into the combinational logic and the output captured gets shifted out which will be compared with the expected response later.

There are three different types of scan cells which can be used[1]: 1. Muxed – D scan cell, 2. Clocked scan cell, 3. LSSD scan cell. In our experiment, we have used a muxed – D scan cell. There are two types of scan architectures were reported, they are: Full scan design and partial scan design are two of the scan architectures used. In case of full scan, all the normal cells have to be converted to a scan cell. The advantage is that combinational Automatic Test Pattern Generation (ATPG) is sufficient for the testing of sequential logic. In partial scan, only some normal cells are converted to scan cell. The need for partial scan arises due to the fact that a scan flop occupies more area than a normal flop[2]. But there are drawbacks: sequential ATPG which increases the complexity have to be used and also there will be a decrease in the percentage of fault coverage.

While forming the scan chains, the scan flops from different clock or power domains can be connected together. In such cases, we need to use some special cells in between them. In case of clock mixing, a lockup latch is inserted. Figure 1 shows the need for using lockup latch.

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Clock_a and Clock_b are the different clocks applied to the consecutive flops. If the combinational delay is less, the data launched at 1st edge of Clock a may be captured at 1st edge of Clock_b which is incorrect. In the presence of lockup latch, the latch is enabled when the Clock_a has a negative level and hence the data will reach Clock_b at the 2nd edge ensuring correct operation. Similarly isolation cells are used when two flops belonging to two different power domains are connected. It is to ensure that no unknown values get propagated from the off domain to on domain.

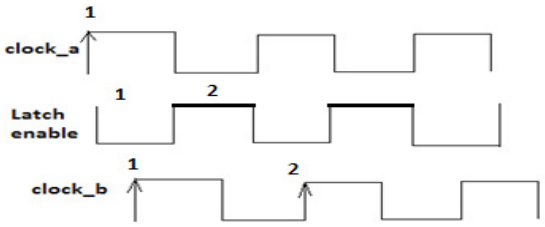

Figure 1. Waveforms to show the operation of lockup latches.

A partitioning algorithm is proposed where the scan cells are divided into some partitions with equal number of flops but with varying layout area[3]. These partitions are ordered based on physical information of the scan in and scan out pins as well as the aspect ratio of the layout. Here the importance was given to reduce the number of level shifters. The occurrence of segments in scan chains was not considered. A linear time approach to optimize the scan chains in two steps[4]; 1. Coarse optimization was done with flops are grouped recursively into *q* groups of elements. The *q* is defined by a 3-way optimization in top-down approach. 2. Fine optimization of the scan chains is performed by flattening and slicing into groups of size (*q+1*). Though the results were relatively good compared to Nearest Neighbor (NN) technique, it considers scan chains with single clock domain only which is not correct in case of real designs.

The efficiency of testing is directly related to the toggle rate which leads to an increased switching activity compared to the normal functional operation[5]. Here the authors have proposed a two-step method: 1. FFs in chains are arranged to minimize transitions in shifting operations with the consideration of the test vectors and its responses. 2. The position of input and output flops are determined considering weighted transition such that the least transitions get propagated to the output. Though this method reduces power, there could be an increase in wire length. To minimize the wire length, ordering of chains can be done with respect to routing[6]. An Advanced Travelling Salesman Problem (ATSP) solver works on the cost matrix which was generated by the algorithm. The wire length using this was less compared to the one based on placement ordering. But the effectiveness is dependent on the routing tool.

To improve further, scan reordering is considering layout information also[7]. The scan FFs are chosen by determining the distance to other scan FFs within a neighborhood range. This method consumes less computation time. It also considers the formation of segments in the scan chains. In order to reduce the length of scan chains and the power, a Genetic Algorithm (GA) based method was proposed[8]. Here the FFs are considered as the chromosome's gene and the numbers of FFs determine the length of the chromosome. Selection, crossover and mutation are the three genetic operations used. Weighted parameters are used to determine the preference for wire length or power reduction.

A stable marriage approach is applied for multi-chain assignment problems[9,10]. In this method, scan FFs gets assigned to one of the ideal chains. The ideal chains are formed by joining scan input to scan output pin based on their mutual preferences. For ordering further, Simulated Annealing (SA) is applied to each of the chains[11,12]. The major issue with this is the run time, O (n^2) which increases with the number of flops (n).

From the literature review, it was concluded that when multiple domains are present, there can be possibility for the improvement in overall test performances. In the presence of multiple domains, scan chains are formed of segments. Due to this segmentation, chain reordering is limited and also there will be an increase in the count of special cells like lockup latches, isolation cells[13]. Thus an algorithm which reduces the number of segments as well as the scan chain wire length is proposed in this paper.

2. Methodology

The methodology followed for developing the algorithm is mentioned in Figure 2. The proposed algorithm will work on the post placed database. The primary input is Scandef file, which contains the information regarding the scan chains. The secondary inputs are: 1. Netlist file, which contains the logical information related to the

design; 2. DEF file, which contains the physical information; 3. UPF file, which contains information related to power specifications.

The implementation of the algorithm was carried out using TCL scripting. The algorithm developed is expected to optimize the wire length and to reduce the number of multi voltage cells.

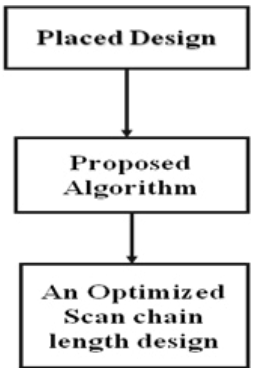

Figure 2. Methodology used.

3. Algorithm

The proposed algorithm for scan allocation without clock mixing and with clock mixing is discussed in the following paragraphs. From the existing scandef file, total scan cells and number of scan cells for each partition are collected. Using this, ideal number of FFs required per chain, also the left and right limit for the chain length are determined. Then the user can set these limits as certain percentage of ideal chain length.

3.1 Without Clock Mixing

- For each of the partitions, divide the scan FFs by the ideal number of elements.
  - If it's greater than zero, then set the chain covered to the quotient of the division.
  - Find the number of leftover cells after this allocation i.e. partition count - (chain covered * ideal_ele).
- If the leftover cells is not equal to zero, for any partition, then:
  - Find the extra number of elements to be added to each chain of the partition using the left over cells.
  - Still anymore elements are left, that is added to the last chain of the partition.

3.2 With Clock Mixing

- Find out the half left limit and the half right limit.
- An array chain info is formed where the array names are each of the available partitions.
- The value is in the format: <number of chains><length of the chains><flag1><flag2>.
- Here if flag1 is 1, then single clock mixing was allowed to form the chain.
- For each of the partitions and for each i^{th} element of chain info, check if i is odd, the value is not equal to 0 or 1 and the value of $(i+1)^{th}$ is not equal to 1 (This is to restrict only one clock mixing)
  - Combine half elements and check
  - Check if the i^{th} element is > = half_left_limit and < = half_right_limit.
  - If yes, then check the leftover cells for each of the partitions.
  - Find sum = i^{th} element value + leftover cells (iteration 2).
  - Check if the sum is greater than or equal to left_ limit and less than or equal to right_limit.
  - If yes, then replace the ith element with the sum and change $(i+1)^{th}$ element to 1.
  - Set the array covered to 1 so that this partition is not taken again.
  - Write down to a file to show which elements were added to form the chain. This is to help in forming the scandef file.
  - Combine diff % from the partitions to form the chain
  - Check if the i^{th} element is > = half_left_limit and < = half_right_limit.
  - Check if ith element is < = (50 % of ideal_element) and also if that partition has been covered yet.
  - If yes, then check the left over cells for each of the partitions taking either 100% or upto 50% of total elements for that leftover cells.
  - Get the sum and check if its > = left_limit and < = right_limit.
  - If yes, then replace the ith element with the sum and change $(i+1)^{th}$ element to 1.
  - Set the array covered to 1 so that this partition is not taken again.
  - Since we are not taking the whole leftover cells, modify the count of the leftover cells. Round

((1-($j*0.01)) * $leftover($itr1) where j is the % of cells used.
- Set the array covered to 1 and append the data to above mentioned file
- Combine diff % from the partitions to form the chain:
- Same as b.
- Only diff is here we check if ith element is > = (50 % of ideal_element) and leftover cells is between 50% to 5% of total elements.
- Combining only leftover cells:
- Check if the i^{th} element ha value < ($1/4^{th}$ of ideal_ele).
- For each partitions, take the leftover cells and combine with some % of leftover cells of another partition.
- Combination is sum and should be > = left_limit and < = right_limit.
- Check if the sum is > = left limit and < = right_limit.
- Replace the i^{th} element (which is the chain length) with this sum. Also add the previous i^{th} element to the leftover cells for that particular partition. And change the count of the leftover cells of the used partitions.
- Append the data to the output file.
- Write down to a file to show which elements were added to form the chain. This is to help in forming the scandef file.

- After doing all the above mentioned steps, check if any leftover cells are present for each of the partitions.
- If no, close the file and exit.
- If yes, find the elements of the array for each of the partitions which are = ideal_ele and whose (i+1) element is! = 1, then take the some of the ith element and the leftover cells and check if the sum is > = left_limit and < = right_limit.
- If yes, then append to chain_info of that partition, the extra chain (value 1), its length followed by 1 and 0. And reduce the previous chain count by 1. Write out the information to the file.

After the scan chain allocation, an output file containing all the information of the new chains formed is created. Using this output file and the old scandef file as the input, a new scandef is generated which contains the modified scan chain information. In order to integrate the new scan chains into the design, the earlier scan chain connections were disconnected and new chains were formed by connecting the flops in the same order as described in the new scandef file.

4. Results

The results obtained using the proposed algorithm is discussed in this section. Without allowing clock mixing, the scan chain allocation for Industry design 1 is shown in Figure 3. The design has 6 partitions and the scan flops allotted for each partition is printed corresponding to the partition name. In this method, there is no additional segments created but there is a large imbalance in the chain length varying from 15 to 659 though the ideal chain length is around 460.

Scan chains formed after allowing clock mixing for the Industry design 1 is shown in Figure 4. The data corresponding to the partition name shows the allocation of scan flops. Consider the partition clk_2. The data corresponding to clk_2 indicates that a chain of length 479 is formed, since the flag field is 1, the chain is formed by mixing two clock domains. Figure 5 shows scan flops allocated to the chains for another Industrial design.

We attain a good chain balancing with the addition of minimal number of lockup latches. But one more issue is that the maximum chain length is more compared to the original algorithm, this can lead to an increase in the number of ATPG cycles. So the algorithm was modified to take this factor also into consideration. The allocation is shown in Figure 6.

The maximum chain length is less than the previous one. Hence here there is good chain balancing with reduced ATPG cycles. One of the scan chain formed after applying the algorithm is shown in Figure 7.

```
clk_2 : 1 15
clk_3 : 48 469 1 505
clk_0 : 1 462
clk_4 : 1 218
clk_1 : 1 658 1 659
clk_5 : 9 488 1 491
~
```

Figure 3. Scan chain allocation without clock mixing for Industry design 1.

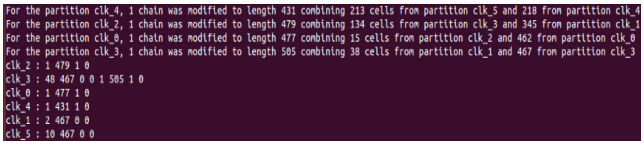

Figure 4. Scan FFs allocation without clock mixing for Industry design 1.

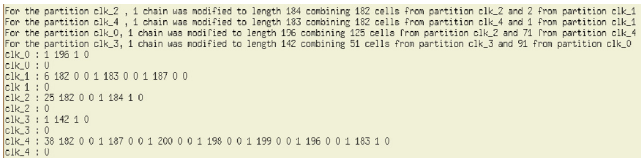

Figure 5. Scan FFs allocation without clock mixing for Industry design 2.

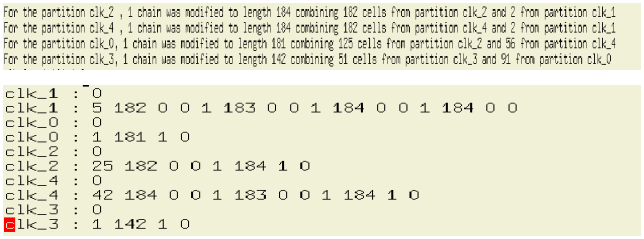

Figure 6. FFs allocation considering ATPG cycles for Industry design 2.

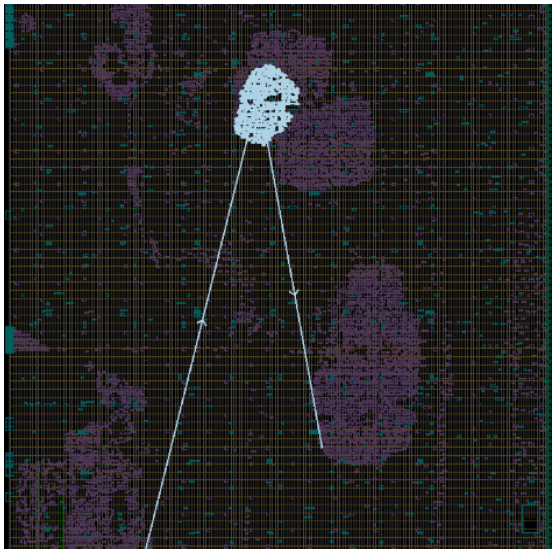

Figure 7. One of the scan chains formed after applying the algorithm.

5. Conclusions

An algorithmic method is proposed to allocate the scan cells to form a particular set of scan chains which reduces wire length and number of multi-voltage cells. This also maintains the balance of the chain. The proposed algorithm was implemented in Tool Command Language (TCL) and it works on the post placed database. The developed algorithm was tested on the industrial designs as given in Figure 3 to Figure 7 and it reveals that the wire length reduced about 10% and the count of the lockup latches to a much greater reduction about 90%.

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