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Power Efficient 3D Clock Distribution Network Design with TSV Count Optimization

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Abstract

This paper mainly focuses on power efficient and low skew clock network design for three-dimensional ICs based on through-silicon via (TSV). Clock tree synthesis is carried out in two major steps; 1) 3D Abstract clock tree generation; 2) buffering with skew and slew consideration. Firstly we design abstract clock tree by using(3D-MMM) followed by skew and slew aware buffer insertion. We analyze how the inclusion of TSVs will affect RC parasitic of an otherwise 2D clock network design by studying Elmore Delay model for 3D topology. We propose extension to the Exact Zero Skew (EEZE- Extended Exact Zero Skew) algorithm by Dr. Tsay for 3D topology which considers TSV resistance-capacitance. This algorithm designs the clock tree by using optimum number of TSVs suitable for the circuit. This is accomplished by merging cost comparison between sets obtained after 3D MMM implementation. This showed 19% to 23% reduction in wire-length. Spice analysis of the obtained clock network resulted in 16% to 18% reduction in clock power dissipation. This indicates that, 1) With optimum TSV count, wire-length of the clock tree reduces by the considerable amount, 2) Small trade-off between optimal TSV count and wire-length, reduces power dissipation.

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Keywords: through silicon via (TSV); merging cost; 3D abstract clock tree; buffering.

1. Introduction

According to Moores law, the number of transistors on an IC, double approximately every two years. Aggressive technology scaling has increased transistor number per IC to a whopping billion. Due to this, clock routing has become too complex and power per unit area has increased excessively. Therefore as physical limits have been put on technology scaling; moving into third dimension for IC design gives us a way to move beyond Moores law. 3D IC has emerged as a promising player in technology scaling. It reduces area while increasing number of transistors per die. Multiple approaches are being followed for stacking purpose, such as 1) die to die, 2) die to wafer and 3) wafer to wafer. 3D IC basically consists of number of dies stacked on top of each other, where inter-die connection is achieved

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with use of through silicon via (TSV)[2]. In 3D ICs. Primary focus is on controlling clock skew in 3D IC design. Also, to avoid setup and hold time violations, clock network latency must be low[3]. Clock distribution network drives higher load capacitance. Large amount of chip power dissipation takes place through the clock network[4].

Through silicon via (TSVs) are used to provide clock signals to all the dies stacked vertically. TSVs are larger compared to logic gates. At 45nm technology node footprint of TSV is comparable to approximately 50 gates. Also TSV reliability issues are important factor for their industrial use[5]. As shown in figure 1, multiple TSV holds obvious advantage that overall wire-length reduces by great extent[6,9]. Also, there are smaller sub trees when multiple TSV is incorporated, which helps in reducing clock skew without higher order buffer, hence the low power. Different types of TSVs such as via first, via middle and via last[12] are studied according to their merits and demerits. There are very few industry standards available for TSV based IC design, manufacturing and packaging. Hence not much of work is done in this area yet.

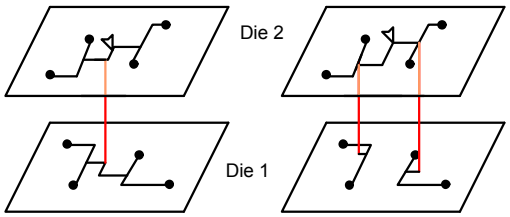

Fig. 1. A two die stack 3D IC clock network distribution with a. single TSV b. Multiple TSV; wire-length is shorter in b.

In 3D clock distribution network, it is very important to understand how the number of TSVs used and TSV resistance and capacitance (RC) affect the performance of the network. More TSVs result in less wire-length, but at the same time TSVs possess higher capacitance, which increases dissipated power if TSV count is not monitored.

Methodology followed in this paper is as follows

1)We design delay model for 3D design embedded with through silicon via (considering TSV resistance and capacitance) based on Elmore delay model.

2)We propose an effective algorithm, to design 3D clock distribution network with optimum TSV count utilization.

3)Buffering and embedding is performed on clock network for slew and skew control[17].

2. Previous work

In power efficient 3D clock network design, TSV placement planning plays a pivotal role. Minz et al.[6] presented one of the early significant works in 3D clock routing. They studied thermal effects on 3D clock network. Kim and Franzon proposed that 3D ICs key player when it comes to speed up the performance without increase in power[10,11]. Kim et al.[9] presented an embedding algorithm DLE-3D for 3D abstract tree topology generation. But they did not provide in skew, power related SPICE simulations. 3D clock network design for pre bond testing was presented by Zhao[7] et al. Due to considerable amount of area covered by TSV dimension, it is important to work on maximum possible TSV count. Liu[18] et al. proposed an algorithm for 3D clock network design based on sink point density for TSV placement. Also TSV capacitance affects power dissipation[15]. Therefore detailed study of TSV count and capacitance is needed.

3. Problem formulation

3.1. Notations in our algorithm

Set of clock sinks as given in the benchmark is represented by ‘S’. An ‘x-y cut’ is made when partitioning through x or y direction is made, whereas ‘z cut’ is made when die contents are partitioned vertically. Input nodes of binary clock tree are defined as ‘$child_1$(X)’ and ‘$child_2$(X)’ where X is the parent node. ‘α’ and ‘β’ are resistance and

capacitance per unit length as specified in technology library. 'L' is total Manhattan distance between the two sink points and 'x' is ratio if distances from tapping point to the children nodes. 'C_i' and 'C_{tsv}' are sink point capacitance and TSV capacitance respectively. 'R_{tsv}' is TSV resistance. Arithmetic difference between die index is represented as 'Z'. '$Cost_i$' represents merging cost between two clock sinks, it is a function of sink point capacitance, wirelength capacitance and TSV capacitance. Root of the clock tree is presented by 'Clk'.

3.2. Objectives of 3D clock tree synthesis

In 3D clock tree synthesis, main objective is 1) to design clock tree such that TSV count should be optimized so as to control power in the circuit, 2) To connect all the sink points in all the vertically stacked dies with a single clock tree, 3) to minimize clock skew and slew rate to avoid setup and hold timing violations, 4) to reduce wire-length and power dissipation.

Clock skew is the difference in time of arrival of clock signal at the sink points. We have designed Elmore delay model considering TSV placement at upper die (considering a two die 3D IC).

3.2.1. Elmore delay model of 3D clock distribution network

In this paper, 3D clock tree is designed as an RC network. In the given benchmark, sink points which are flip flop clock input points are modelled as load capacitance. Through silicon vias are considered as another type of wire which has its own resistive and capacitive properties. Our 3D Elmore delay model is shown in figure 3. Wire segments and through silicon via are modelled using model[16].

Elmore delay model zero skew equation is presented as,

$$\alpha x l\left\{\frac{\beta x l}{2}+Ca\right\}+t1=t2+R_{tsv}\left\{\frac{C_{tsv}}{2}+\beta(1-x)l+Cb\right\}+\alpha(1-x)l\left\{\frac{\beta(1-x)l}{2}+Cb\right\} \quad (1)$$

Equation for tapping point can be formed by solving the above equation for x.

Also, equation to calculate merging cost is given as,

$$cost=\beta l+Ca+Cb+C_{tsv}\times|Z| \quad (2)$$

Merging cost is a function of capacitances as it contributes major power consumption in the chip.

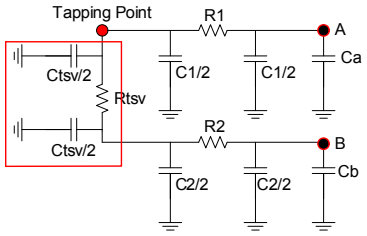

Fig. 2. Electrical model for a pair of sink points residing in two different dies.

4. 3D clock tree synthesis

4.1. Overview

In our paper, clock tree synthesis is completed in two steps. 1) Generating 3D abstract clock tree topology, 2) Buffer insertion for slew and skew control. Generating abstract clock tree topology takes place is two steps viz. a) 3D MMM algorithm[14]; this algorithm is used for dividing clock sink points over vertically stacked dies considering x-y geometry, as directed in figure 4. Once all the sink points are sorted using this algorithm; b) Our EEZE skew

(Extended Exact Zero skew for 3D) algorithm is used for merging the clock sink points. This merging can take place in two different ways, 1) in same die, 2) in different dies.

4.2. 3D abstract tree generation

It is the first step in synthesizing clock distribution network. It is very important to make sure that all the clock sinks are connected by a single clock tree. The tree is constructed in bottom to up fashion. This abstract tree represents information regarding clock sinks, which act as children nodes, their parent nodes and TSVs. Wire-length estimation model used for 3D clock routing is Minimum Steiner tree model.

Consider S is a set of sinks given in the circuit. According to MMM 3D[14] algorithm, firstly this set is divided ran-

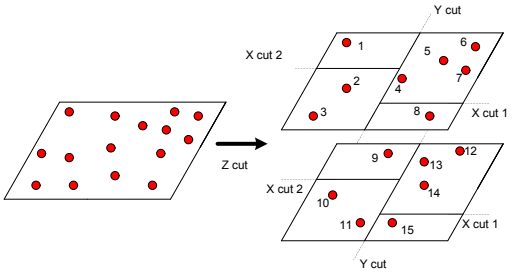

Fig. 3. MMM 3D algorithm for sorting sink points

domly into two equal sets. All the sinks of set S have x, y and z locations. Z being the die number in which sink point belongs to. While ignoring their z location for the time being, we apply our 3D-EEZE skew algorithm for merging. Merging is done on the basis of merging cost. If a pair is from different dies, then those two points will be connected with the help of TSV, else without TSV.

4.3. Buffer insertion algorithm

3D abstract tree topology generation is followed by buffer insertion. Goal of this step is to find out exact location of buffers. If the load capacitance of a sink point exceeds predefined C_{max} value, then a buffer is added that location. Same procedure is carried out for all stages in the clock tree[13, 14]. Effect of C_{max} on clock network power and slew is described later in section V.

Main objective of adding buffers to the clock distribution network is to reduce the slew rate of clock signal at the clock sink points.

4.4. Brief introduction to the 3D EEZE skew algorithm

Our EEZE skew algorithm can be represented as a rooted binary tree with clock source at its root. Here we assume clock source to be in one of the dies to start off with clock network design.

This algorithm is repeated till all the sink points are connected by a single clock tree. In the end we get a clock tree connected by through silicon vias (TSVs) at the various stages of embedding. And we get a clock tree in the form of a rooted binary tree.

To better understand the algorithm, let us consider sink point distribution as shown in figure 4. Sink points consist of x-y location and load capacitance at that locations. We distribute these sink points randomly in two sets to get figure 1b. Now, every sink point has a z-location too. Die index is represented by z location. For each region, R1 through R8, merging cost for all the pairs in that region is computed using Eqn. 2. and compared with each other. For example, in R7, sink points 6 and 7 have lower merging cost when compared with merging cost between sink points 5 and 6 or 5 and 7. Hence we merge sink points 6 and 7. Similar process is followed for all the regions. In case of

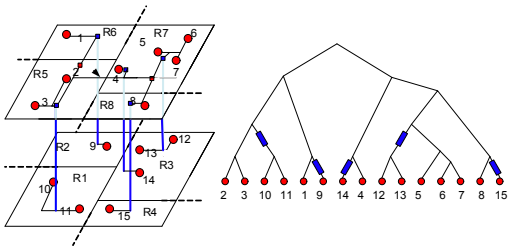

Fig. 4. 3D clock network generated by EEZE skew algorithm and same clock network topology represented as a rooted binary tree

Input: Clock sink points as given in benchmark, number of dies=2
Output: 3D abstract clock tree in form of a rooted binary tree with clock source at its root

1: 3DAbstractTree (Sink point set, number of dies);
2: S_1 and S_2 = two subsets of clock sink set (as we have considered two vertically stacked dies)
3: If |S|==1; return S_i as the clock source of the circuit
4: else if |S|>1, apply 3D MMM algorithm to sort sink points in smaller sets;
5: Consider S_t (Outcome of 3D MMM) and re-arrange them in their increasing x location order;

EEZE Skew Algorithm:
6: For each S_t, $cost_i = C_i + C_{i+1} + \beta*(l) + z*C_{tsv}$ for every pair of clock sinks;
Now assume there are 3 points in a sorted set $S_t=(S_1,S_2,S_3)$;
7: If $cost_{(S1,S2)} > cost_{(S1,S3)}$ then swap inputs S_2 and S_3 so as to merge S_1 with S_3, while S2 being left to merged at a later stage, hence now $S_t=(S_1,S_3,S_2)$;
8: Repeat this process for all S_t;
Now we have got sink points in order that they are supposed to be merged in
9: If $Z_i = Z_{i+1}$; #TSV=#TSV+0;
10: else if Z_i != Z_{i+1}; #TSV=#TSV+1
Repeat EEZE Skew algorithm;

Fig. 5. The proposed 3D EEZE Skew Algorithm

merging in between two different dies, i.e. TSV embedding, the tapping point is always considered in 2nd die. This simplifies designing clock tree in later stages. Finally we get a clock tree as shown in figure 5(a). Whereas figure 5(b) represents the whole clock tree in a form of a rooted binary tree.

5. Simulations and analysis

5.1. Simulation settings

In this paper, we implement EEZE skew algorithm on a two-die stack to analyse effect of TSV count and its electrical properties on clock skew and clock power consumption. We use benchmarks provided by International Symposium of Physical Design (ISPD09f22) and IBM (r1)[20]. Clock tree is designed using MATLAB. We validate our designs for clock skew, slew and power using NGSPICE.

Our clock frequency operates at 1GHz. 45nm Predictive Technology Model[19] is used for technical parameters. Resistance per unit length is 0.1Ω/μm and capacitance per unit length is 0.2fF/μm. TSV resistance is 35mΩ and TSV capacitance is considered as 15fF. The supply voltage is set at 0.9 Volts. For better skew control, C_{max} is set at 300fF.

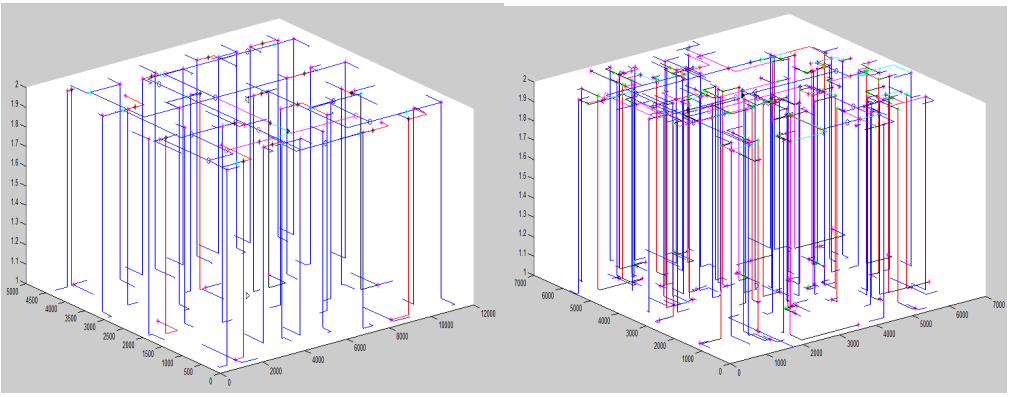

Fig. 6. Clock network design for benchmarks ISPD09f22 and IBM R1

Table 1. Previous work on TSV count, wire-length(m), clock skew (ps), power (mW) and buffer count for multiple TSV usage for 2-die stack in ISPD'09f22 and r1 benchmarks

Benchmark	No. of Sinks	Existing Work				
		TSV	WL	Skew	Power	Buffers
ISPD'09f22	91	31	76909	22	35.60	100
R1	267	91	221142	14.6	125	292

Table 2. Our work on TSV count, wire-length(m), clock skew (ps), power (mW) and buffer count for multiple TSV usage for 2-die stack in ISPD'09f22 and r1 benchmarks

Benchmark	No. of Sinks	3D EEZE Skew Algorithm				
		TSV	WL	Skew	Power	Buffers
ISPD'09f22	91	38	75185	22.14	33.16	82
R1	267	94	218190	18.20	125.62	231

5.2. Analysis and discussion

5.2.1. Effect of TSV Count and TSV RC Consideration

As observed in previous work, use of multiple TSV indeed reduces overall wire-length and power dissipation. We observe that, our algorithm for finding out optimum number of TSV count gives better results in lowering wire-length and power dissipation more than existing works. Also we have considered TSV RC properties which were not considered in some literature. This gives us more prominent way of verifying power and skew in SPICE simulations.

5.2.2. Results

3D clock routing for both ISPD'09f22 and r1 benchmarks is shown in figure 7. Observations made from 3D clock tree synthesis are noted in tables 1 and 2, where table 1 represents work done till now whereas figure 2 represents our work. We have used 3% to 7% more TSVs without any trade-off whatsoever in power consumption and reduced wire-length at the same time. Our slew rate has been constrained to less than 8% of the clock period whereas slew rate up to 10% of clock period is permissible under aggressive clock tree synthesis. Our design restricts clock skew below 25% of the clock period and satisfies the condition directed by ITRS projection committee. Our skew is 10% to 12% more than the designs presented till now. Poorer skew is result of maintaining the design power efficient. Our design is 18% to 20% more efficient than other design when compared to buffer usage. This helps in maintaining lower slew rate without increasing power.

5.2.3. Impact of C_{max} on buffer design

Upper limit of C_{max} is defined at 300fF, results in less power consumption. When we analysed clock power at load capacitance limit of 180fF-250fF, we noticed that we got much better slew control. But it increases power dissipation in the circuit beyond desirable range. Hence with a bit higher load capacitance limit, both slew rate control and low power design is obtained.

6. Conclusion and Future Scope

In this paper, we analysed different techniques to design a power efficient, low skew 3D IC clock tree. We saw that at higher TSV capacitance, TSV count in the circuit plays important role as higher capacitance increases power. Hence we found the need to develop an effective algorithm which could address TSV count optimization. We proposed EEZE (Extended Exact Zero) Skew algorithm for 3D ICs which gave us simpler way to find out optimum TSV usage permissible for a circuit, while maintaining skew well within industry standards. Our algorithm proves to be reliable, simple and more accurate for power efficient 3D clock network designs. In this paper, we have not considered minimum distance permissible between two neighbouring TSVs sighting large footprint area making it potential background for future work

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