Solar fed DC-DC single ended primary inductance converter for low power applications

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Solar fed DC-DC single ended primary inductance converter for low power applications

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Abstract. This paper presents 34 to 36 volts. SEPIC converter for solar fed applications. Now days, there has been tremendous increase in the usage of solar energy and this solar energy is most valuable energy source available all around the world. The solar energy system require a Dc-Dc converter in order to modulate and govern the changing output of the panel. In this paper, a system comprising of Single Ended Primary Inductance Converter [SEPIC] integrated with solar panel is proposed. This paper proposes SEPIC power converter design that will secure high performance and cost efficiency while powering up a LAMP load. This power converter designed with low output ripple voltage, higher efficiency and less electrical pressure on the power switching elements. The simulation and prototype hardware results are presented in this paper.

1. Introduction

Now a days due the depletion of non-renewable energy resources like fossil fuels and coal. We need to look after for renewable energy resources like solar, wind, geothermal. Out of which solar is more and plentiful available energy around the world and the conversion from solar to electrical energy, technology is also available[1, 2]. Now a day's solar energy is becoming the most advantages and helpful for household and agricultural appliances .This paper mainly emphasis on solar energy for electrical requirements for low power applications like lamp loads While using the applications of renewable energy we need the converters to get the output without fluctuating and ripple free outputs. We have different converter topologies for our applications like Buck, Buck-Boost, Cuk, SEPIC[3-4]. Out of these different topologies we considered SEPIC Converter because it is basically Buck-Boost converter and its main advantage is no polarity reversal at its output terminals and low ripple voltage and higher efficient[5-6]. The objective of this paper is to produce an output voltage of 36 volts DC from converter with an input of 34 volts DC from a solar panel and used for running low power applications.

2. Circuit Topology and operating modes

The circuit diagram of the suggested power converter is shown in Figure 1. There are 2 modes of operation, being the continuous conduction mode and the discontinuous conduction mode. The SEPIC Single Ended Primary Inductor converter can produce an output voltage greater or lesser than input

voltage without changing input polarity reversal. It has more advantages compared to Cuk, buck boost converters. As SEPIC converter produces output voltage with same polarity with low ripple current because of more energy storage components like inductors and capacitors present in circuit [7-8]. SEPIC converter is having more advantages for low power application because the output voltage will be in the range input.

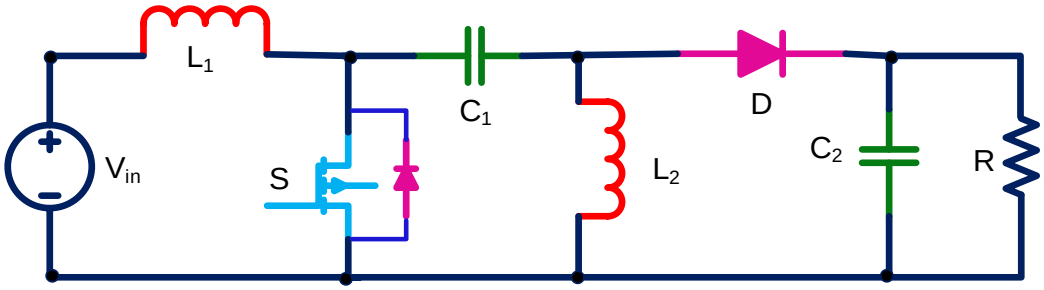

Figure 1. SEPIC converter

$$L_1 \frac{di_{L1}}{dt} = V_{in} \tag{1}$$

When switch is closed, shown in Figure 2. The inductor L_1 is charged through the input source voltage. The inductor L_2 is charged through the capacitor C_1, capacitor C_2 is discharged through the resistor R load. So during switch closed both inductors are charging, both capacitors are discharging. Diode D is reverse biased

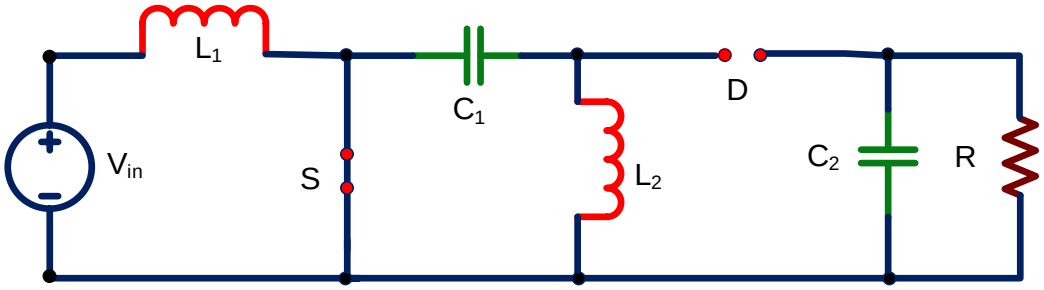

Figure 2. Circuit diagram for Switch S is closed

$$L_1 \frac{di_{L1}}{dt} = -V_o \tag{2}$$

When switch S is Open, Shown in above Figure 3. inductor L_1 is discharged through capacitor C_1 and inductor L_2 is discharged through capacitor C_2. Both capacitors are charging, and inductors are discharging during turn off condition.

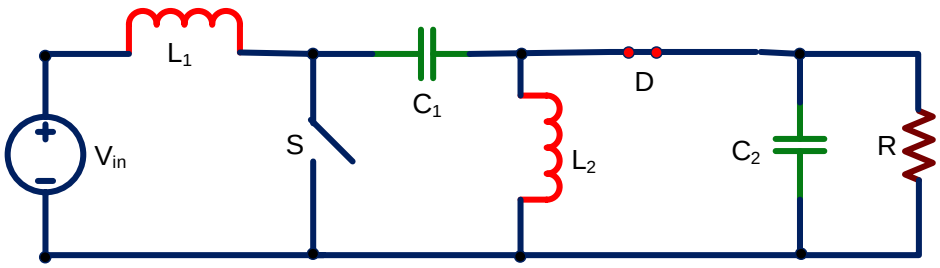

Figure 3. Circuit diagram for Switch S is closed

$$D = \frac{V_o}{V_o + V_s} \tag{3}$$

3. Block diagram

The block diagram shows the overall setup as shown in Figure 4. Where the input to the converter was provided by the Programmable Solar simulator which delivers to the SEPIC converter .The power converter provides the lamp loads at 36 V by suitable energy conversion (step up/boost operation).The switching pulse for the power converter is induced by dSPACE 1104 which can be merged to the MATLAB.

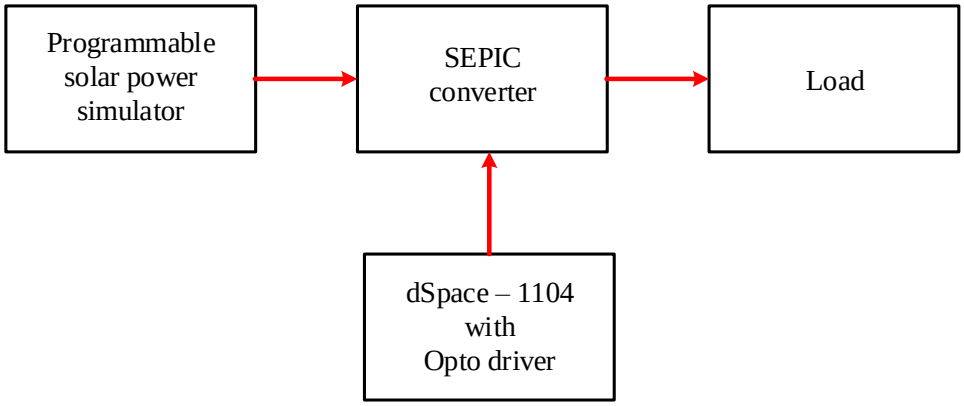

Figure 4. Block Diagram for propose system

4. Mathematical design

The inductor L_1 is the smoothing inductor in the SEPIC converter. This inductor decreases the input ripple current. The value of L_1 is calculated by help of the formula mentioned below.

$$L_{1\min} = \frac{V_{IN}\, D}{f\, \Delta I_{L1}} = \frac{34 \times 0.514}{100 \times 1000 \times 0.554} = 315\ \mu H \tag{4}$$

The input side capacitor C_1 is basically selected by considering both current ripple and voltage ripple. In the presented design of SEPIC converter capacitor C_1 value is calculated by using the formula given below.

$$C_{1\min} = \frac{V_O D}{f R \Delta V_C} = \frac{36 \times 0.514}{100 \times 1000 \times 1.08 \times 12.96} = 13.22 \mu F \tag{5}$$

The output side inductor is selected in order to limit the ripple in output current as much as possible. The value of output side inductor is calculated as follows:

$$L_{2\min} = \frac{V_{IN}\, D}{f\, \Delta I_{L1}} = \frac{34 \times 0.514}{100 \times 1000 \times 0.554} = 315\ \mu H \tag{6}$$

The capacitor at the output side is responsible for limiting ripple in the voltage as well as current. Output side capacitor value is calculated using the following formula

$$C_{2\min} = \frac{V_O D}{fR\Delta V_C} = \frac{36 \times 0.514}{100 \times 1000 \times 1.08 \times 12.96} = 13.22\mu F \quad (7)$$

The following tabulation shows the various parameters used during the hardware testing of the presented SEPIC converter. The pulse for the MOSFET switch is generated using dSPACE keeping the duty ratio as 0.514 for testing of the presented converter.

Table 1. Design specification

Parameters	Values
Input voltage	34 V
Output voltage	36 V
Switching frequency	100 kHz
Duty cycle	0.5
Output power	100 W
L_1	500 μH
L_2	500 μH
C_1	20 μF
C_2	20 μF
Output Ripple Current	(20-30)% load current
Output Ripple Voltage	(1-3)% load voltage

5. Results

The SEPIC converter is simulated with the Simlink software and prototype hardware model demonstrated in the hardwar. The gate pulse for the MOSFET switch is generated with the help of dSpace 1104 real time hardware kit. The pulse is isolated with the help of opto-coupler diver circuit.

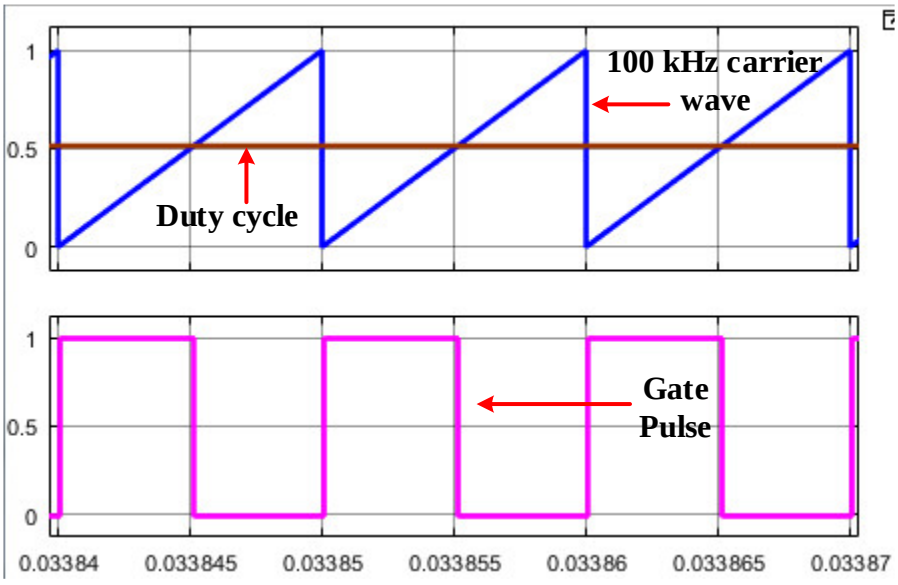

Figure 5. Simulation results of carrier wave, duty cycle and gate pulse

The simulation results of carrier wave, duty cycle and gate pulse are shown in Figure 5. The Figure 6. shows the simulation results obtained at input and output side. The Figure 7(a) and 7(b) are shows the hardware setup. The Figure 8. depicts the hardware setup and Figure 9(a) and Fig 9(b) shows the results are taken at the V_{GS}, I_D and V_{DS}, I_D. The results are matching with minimum ripple in the input current and output voltage.

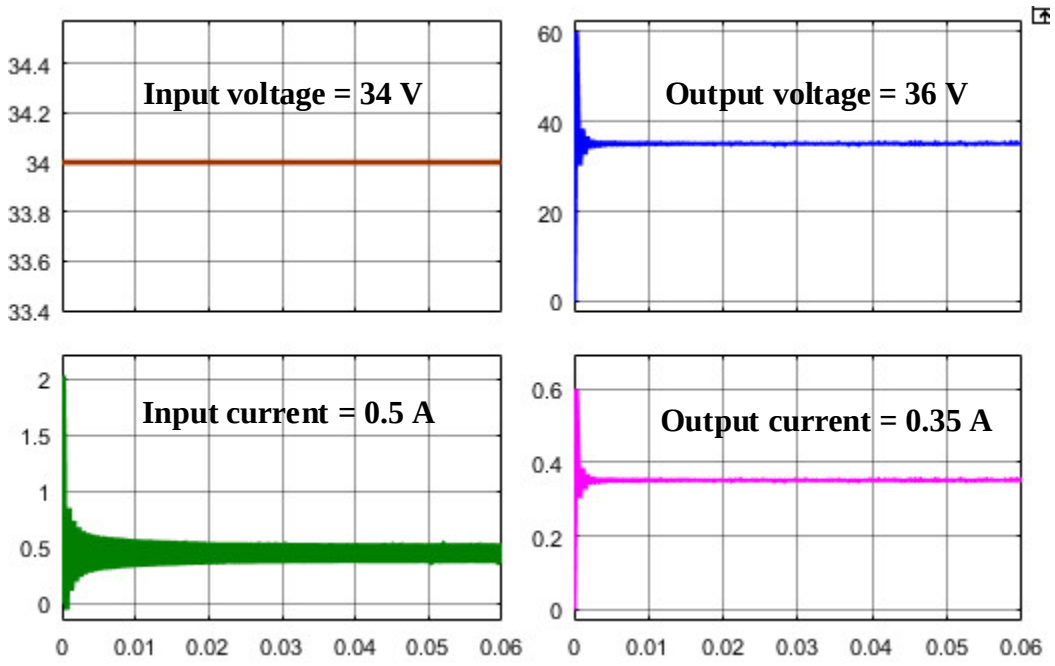

Figure 6. Simulation results of V_{in}, I_{in}, V_{out}, and I_{out}

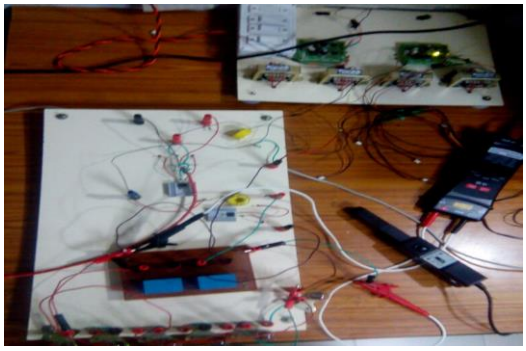

Figure 7 (a). Hardware Setup

Figure 7 (b). Hardware setup with ON condition

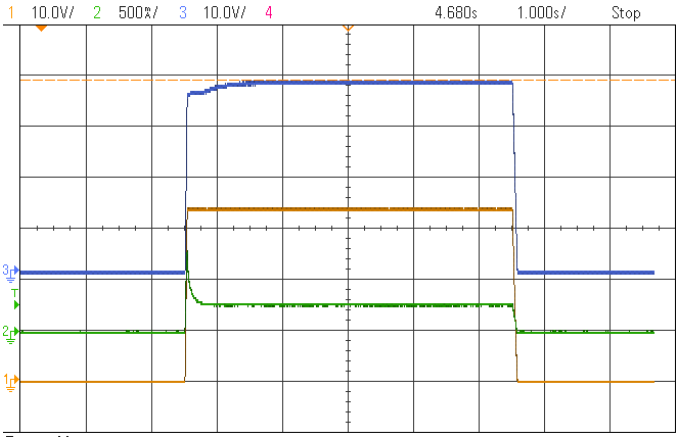

Figure 8. Hardware results of V_{in}, I_{in}, V_{out}

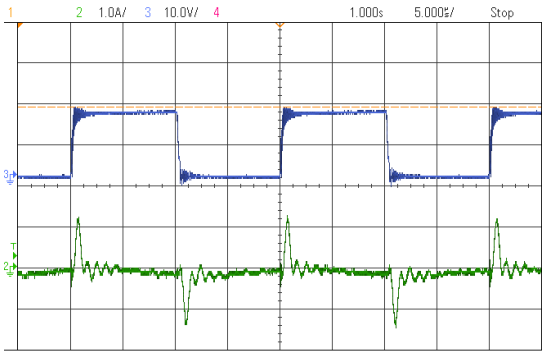

Figure 9(a). Hardware results of V_{GS} and I_D

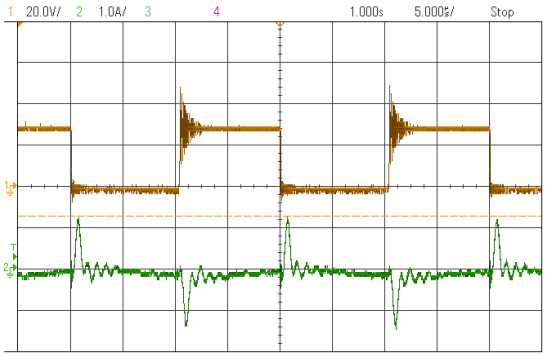

Figure 9(b). Hardware results of V_{DS} and I_D

6. Conclusion

A single ended primary inductance converter is Design for energizing the LAMPS utilizing solar power. The working operation of the power converter is simulated in MATLAB with the voltage of 34 V input and gives the voltage of 36 V output. Hardware circuit is constructed for the same and is tested for 90 W gives an efficiency of 98.84%.

References

[1] Falin and Jeff 2016 Designing DC – DC Converters Based on SEPIC Topology, *Analog Instrumentation Journal*. Texas Instruments Web **12** 18-16

[2] Al Gabri A M, Fardoun A A and Ismail E H 2015 Bridgeless PFCmodified SEPIC rectifier with extended gain for universal input voltage applications *IEEE Trans. Power Electron.* **30(8)** 4272–4282

[3] Duran E, Sidrach-de-Cardona M, Galan J and Andujar J M 2014 Comparative Analysis of Buck-Boost Converters used to obtain I-V Characteristic Curves of Photovoltaic Modules *IEEE power electronics* **12** 2036-2041

[4] Maglin J R, Ramesh R and Vaigundamoorthi 2014 Design and Analysis of SEPIC Converter Based MPPT for Solar PV Module with CPWM *J Electr Eng Techno*. **9(4)** 1269-1276

[5] Shimizv T, Hirakata M, Kamezawa T and Watanabe H 2001 Generation circuit for photovoltaic modules, *IEEE Trans.Power Electronics* **16(3)** 293-300

[6] Banaei M R, Shirinabady and Mehdi Mirzaey 2014 MPPT Control of Photovoltaic Using SEPIC Converter to Reduce the Input Current Ripples, *Journal of Engineering Research and Applications* **4(1)** 160-66

[7] Adhikari, Neha, Bhim Singh and Vyas A L 2011 Performance Evaluation of a Low Power Solar-PV Energy System with SEPIC Converter *IEEE PEDS* 763-769

[8] James Dunia and Bakari 2013 Performance Comparison between CUK and SEPIC Converts for Maximum Power Point TRacking Using Incremental Conductance Technique in Solar Power Applications *International Journal of Electrical, Electronics and Communications Engineering* **7(12)** 1683-1643