Indian Journal of Science and Technology, Vol 10(13), DOI: 10.17485/ijst/2017/v10i13/87202, April 2017
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Tunnel Field Effect Transistors for Digital and Analog Applications: A Review

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Abstract

Objectives: This paper presents the review of Tunnel FET (TFET) to overcome the major challenges faced by the conventional MOSFET. **Analysis**: Various device structures and characteristics of TFET along with different material and doping to improve efficiency are discussed in detail. In recent years, TFET seems to be an attractive device for analog/mixed-signal applications due to their advantages such as high ON current (I_{ON}), low leakage current (I_{OFF}), reduced values of threshold voltage (V_T) and low Subthreshold Swing (SS).

Keywords: Asymmetric Gate Oxide, Band-to-Band Tunneling, Double Gate, Gate on Drain Overlap, Subthreshold Swing, Tunnel FET

1. Introduction

As MOSFET's size scales down, the low power dissipation in the circuit is maintained by reduced supply voltage. The electrical parameters such as Subthreshold Swing (SS) and threshold voltage (V_t) should be very less. But the SS is limited to 60 mV/decade in MOSFETs[1]. To overcome this, several novel devices with various transport mechanism have been reported. Tunnel Field Effect Transistor (TFET), which is one such novel device, employs the carrier transport mechanism of Band-to-Band Tunneling (BTBT).

TFET is a gated p-i-n diode which is turned on by applying necessary gate bias. At sufficient bias the BTBT takes place, allowing the electrons to tunnel from valance band of p-region to conduction band of intrinsic region, resulting in flow of current across the device. TFETs are widely preferred due to their least SS, less leakage current (I_{OFF}) and low threshold voltage (V_T)[2–4].

In this paper, a review on TFETs is presented. Section 2 deals with the characteristics of TFET. Various design consideration and optimization of the TFETs are analyzed in Section 3. The conclusion is given in Section 4.

2. Characteristics of TFET

Figures 1 (a) and (b) illustrate the general schematic of TFET and its energy band diagram. TFET comprises p^+ source, intrinsic channel and n^+ drain. During the OFF-state ($V_g = 0$ V), the width of the tunneling barrier is large enough to provide low I_{OFF} values. In the presence of gate voltage ($V_g = 1$ V), the band bending in the intrinsic region causes the barrier width to get reduced, allowing the electrons to tunnel from source to channel.

2.1 Subthreshold Swing (SS)

Subthreshold Swing (SS) is one of the most important characteristics of TFET. It is defined as the change in gate voltage required for one order of magnitude change in drain current. The SS of MOSFET is limited and cannot be reduced below 60 mV/decade at room temperature. The Subthreshold Swing for MOSFET and Tunnel FET (TFET) at room temperature is defined as follows[5].

$$S_{MOSFET} = \ln(10)kT/q \ (mV/dec) \quad (1)$$

$$S_{TFET} = \frac{V_{gs}^2}{5.75(V_{gs} + Const)} \quad (2)$$

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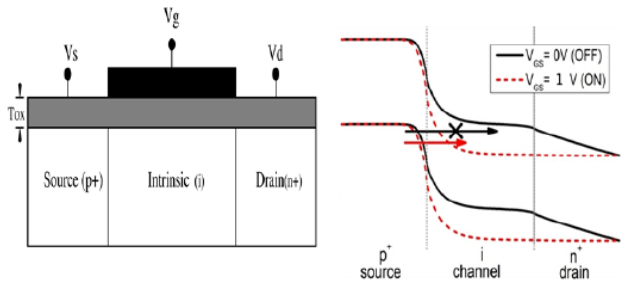

Figure 1. **(a)** Schematic view **(b)** Energy band diagram.

Where k is Boltzmann constant, T is temperature (300 K), q is electron charge, V_{gs} is applied gate-to-source voltage, Const is determined by the device dimensions. The SS value became smaller as gate oxide thickness, Silicon on Insulator (SOI) layer thickness are decreased in TFET[6]. The effective subthreshold slope (reciprocal value of SS) has been reduced by lowering the channel length and using high k materials as gate dielectrics, which is shown in Figure 2[7]. The TFET device is made without junctions called Junctionless Field Effect Transistor (JLTFET)[8,9] to achieve steep slope. A vertical Si based nanowire TFET with source side dopant segregated silicidation has been fabricated with low SS of 30 mV/dec[10].

2.2 Improved I_{ON}/I_{OFF} Ratio

Due to reduced leakage current (I_{OFF}), TFET is found to be more suitable for low power applications. Furthermore, Krishna K. Bhuwalka et al. reported that drive current (I_{ON}) and very low I_{OFF} in TFET can be achieved with gate work function engineering[11]. I_d – V_g characteristic of Silicon (Si) based SINGLE GATE (SG) SOI TFET is shown in Figure 3. It can be inferred that drain current (I_d) increases exponentially with increasing gate voltage at constant drain bias [12] and this is due to high electron tunneling at the source side.

For TFET, I_{ON} is directly proportional to the tunneling probability T(E) and it is given by:

$$T(E) = \exp\left[\frac{4\sqrt{m^*}E_g^{3/2}}{3|e|\hbar(E_g + \Delta\varphi)}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}}t_{Si}t_{ox}\right]\Delta\varphi \qquad (3)$$

where m* is the carrier effective mass, E_g is the band gap, e is the electron charge, ΔΦ is the potential difference between source valence band and channel conduction band, and t_{ox}, t_{Si} are the oxide and silicon film thickness and ε_{ox}, ε_{Si} are dielectric constants of oxide and silicon, respectively. From the above equation, it is evident that

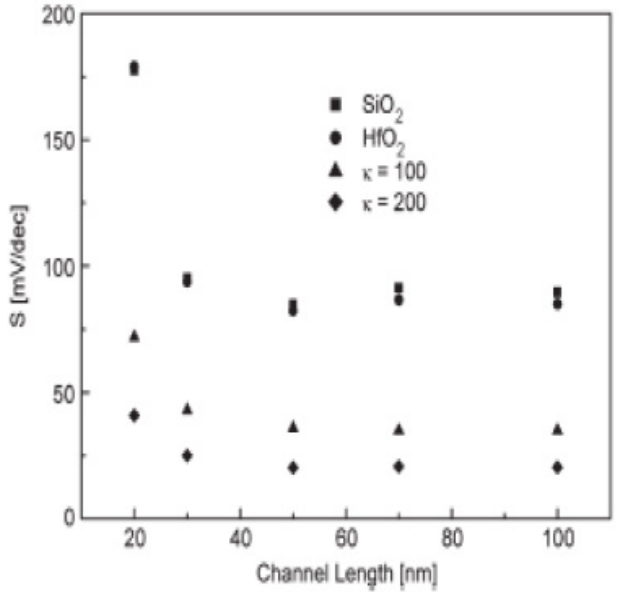

Figure 2. Effective subthreshold slope for different L_{ch} and high k dielectrics[7].

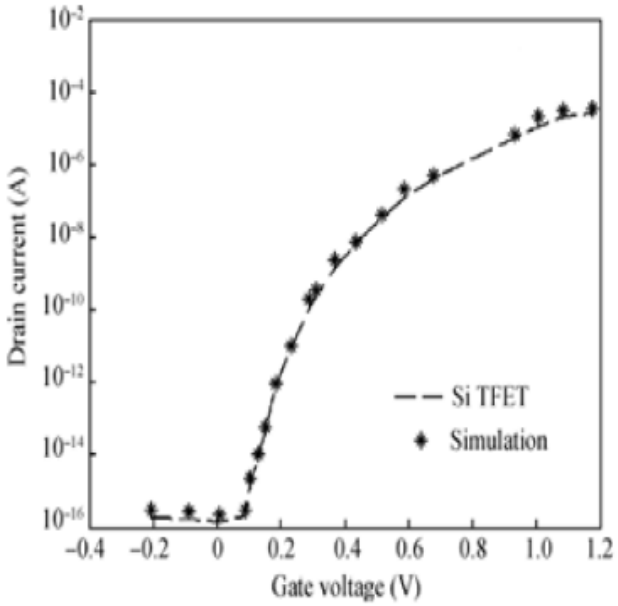

Figure 3. I_d – V_g characteristics of Si based single- gate SOI–TFET[12].

reducing t_{ox}, increasing ε_{ox}, and reducing E_g, will enhance the device performance [13]. Sweta Chander et al. reported that Silicon Germanium on Insulator (SGOI) TFET of gate length (L_g) 30 nm offers more I_{ON}/I_{OFF} ratio[14] up to 3.4×10^9. Higher I_{ON}/I_{OFF} ratio is also obtained for dual material gate TFET and p-n-i-n TFET[15,16].

2.3 Threshold Voltage (V_T)

Threshold voltage (V_T) plays an important role in determining the device performance. Many approaches were developed for the enhancement of V_T. Gate All Around (GAA) vertical n-type and p-type TFETs offers reduced V_T in the range of 0.13–0.22 V[2]. A vertical TFET with SiGe delta doped layer offers less threshold voltage with increasing mole fraction (x). The V_T variation with respect to V_{DS} is shown in Figure 4. V_T is extracted by using constant current method. It can be observed from the graph that, V_T is dependent on V_{DS} in the initial state later exhibiting the saturation behavior[17].

3. Design Consideration and Optimization of TFETs

3.1 Single Gate and Double Gate TFETs

Single gate TFETs possesses low I_{OFF} and also low I_{ON}[18–20]. Increasing the number of gates in the device offers better electrostatic control over the channel. In order to improve I_{ON}, second gate is created at the bottom of single gate TFETs[21–25]. Figure 5 shows the structure of nTFET. Double Gate (DG) TFETs Strained DG TFET

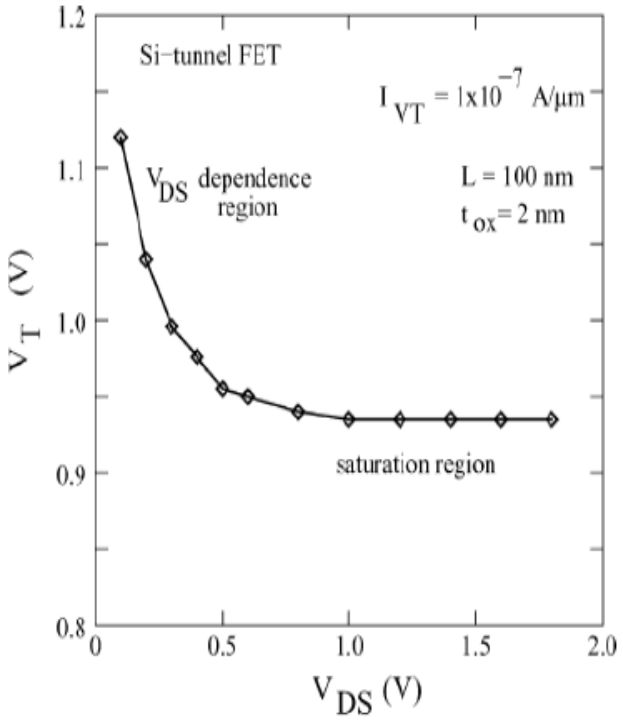

Figure 4. V_T as a function of V_{DS}[17].

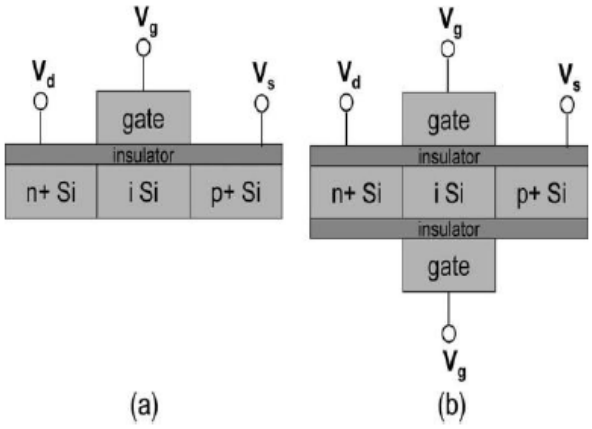

Figure 5. Simulated structure of Tunnel FETs **(a)** Single-gate **(b)** Double gate[5].

reported in[26] has been designed with strained silicon with fractional germanium content for circuit applications. The double gate increases the performance by offering improved transconductance and reduced threshold voltage[27]. Comparing to conventional MOSFET, DG TFETs offers very low threshold voltage roll-off[28], higher I_{ON} and decreased I_{OFF} by careful selection of a gate dielectric[5]. Vertical architecture provides an added advantage in terms of reduced Short Channel Effects (SCE)[29]. For circuit application, the supply voltage was limited to 0.5 V when using Ge based TFET[30].

Compared to 7T TFET SRAM design, 6T TFET SRAM design offers better noise margin and improved performance. Figures 6(a) and (b) represents the DG TFET structure and the 6T SRAM design. The graphical representation shown in Figure 6(c) denotes the standby leakage comparison between TFET and CMOS SRAM design. TFET based SRAM design have reduced leakage over CMOS based SRAM[31]. Since the performance of TFET devices are mainly focused for digital applications, the analog performances are investigated by introducing gate stack architecture shown in Figure 7[32]. TFET devices are now becoming a promising candidate for analog applications[33–36].

3.2 III-V Material based TFET

Enhancement in I_{ON} and SS of DG TFET can be achieved by introducing Dual Material Gate (DMG) in the device by using different work functions to the gates[37]. The device is also found to be immune to DIBL effects. Figure 8 represents the top and bottom gates comprising of two different work functions. The gate nearer to source is called as tunnel gate while the gate nearer to the drain is called as auxiliary

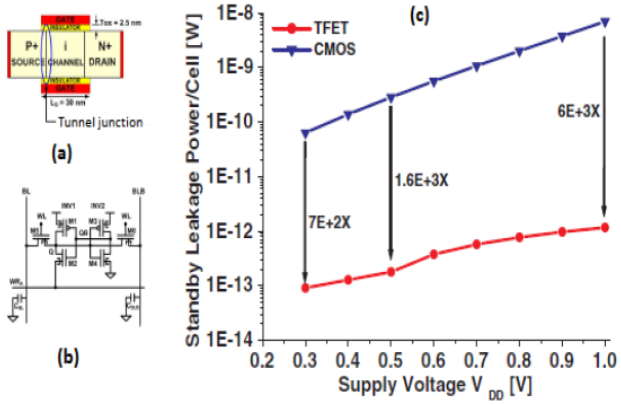

Figure 6. **(a)** DG TFET structure **(b)** 6T SRAM design based DG TFET **(c)** Standby leakage comparison of DG TFET over CMOS SRAM design[31].

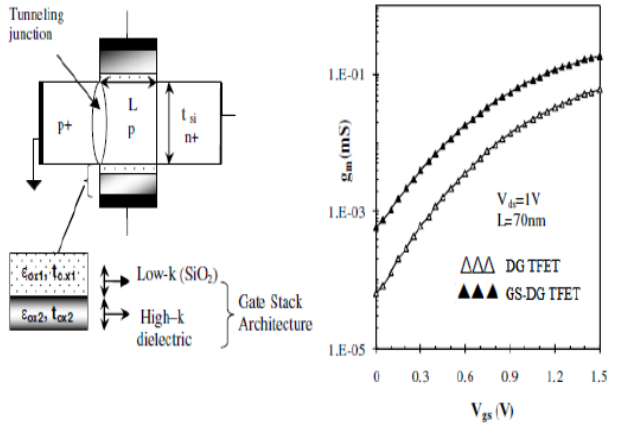

Figure 7. **(a)** Gate stack DG TFET structure **(b)** Transconductance g_m variation with V_{gs} of GS-DG TFET over DG TFET[32].

gate. Due to indirect bandgap material and lower tunneling probability, Silicon (Si) based DG TFETs[38] suffers from lesser I_{ON}, which can be further improved by using lower band gap material like Silicon-Germanium (SiGe)[39-42]. $Si_{1-x}Ge_x$ TFET exhibited the better performance with low SS by optimizing the mole fraction (x)[43]. Small band gap materials were used to improve the carrier tunneling by reducing the width of the tunneling barrier[44]. Additionally, a smaller bandgap material, In GaAs is used at the source of Si-based p-TFET to boost the ON current[45].

3.3 Asymmetric Gate Oxide

Rakhi Narang et al. had reported that the performance enhancement of an asymmetric gate oxide DG TFET is observed with a high-k dielectric at the source and low-k

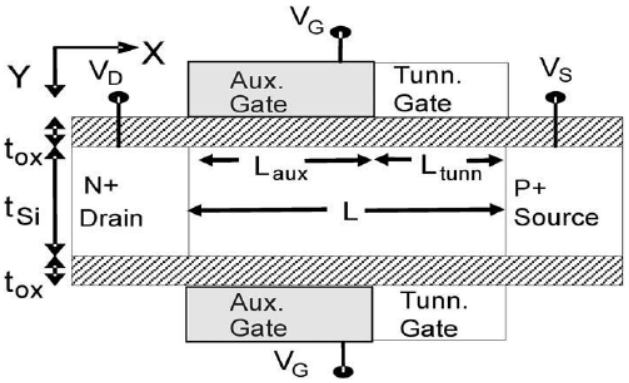

Figure 8. Structure of dual material DG TFET[41].

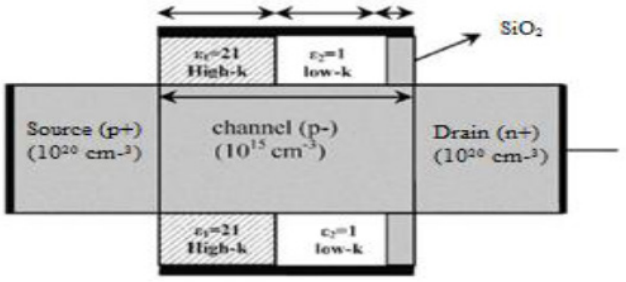

Figure 9. Structure of an asymmetric gate oxide DG TFET[46].

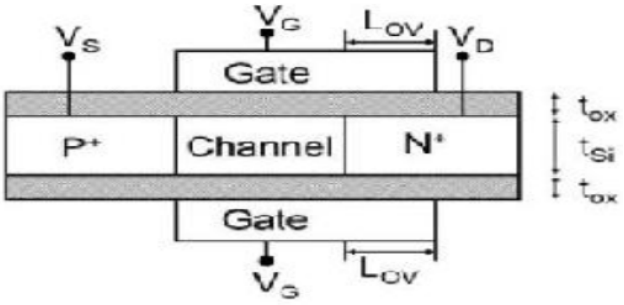

Figure 10. Gate on drain overlap structure of DG TFET[48].

material at the drain. Further to control the high gate drain capacitance problem, low oxide material (SiO_2) is replaced by air (k = 1) at the drain side of the device and thereby resulting in improved cut off frequency. Further the energy dissipation per cycle and the reduced propagation delay obtained from circuit level performance results in better switching characteristics and thereby making the asymmetric gate oxide DG TFET more suitable for low power digital applications. Figure 9 shows the structure of an asymmetric gate oxide DG TFET[46].

3.4 Gate on Drain Overlap

The ambipolar conduction is suppressed by incorporating TFET with gate-drain overlap even at higher drain doping levels ($1\times10^{19}\,cm^{-3}$)[47]. Band bending of the device remains unchanged after $1\times10^{19}\,cm^{-3}$ doping due to gate potential in the overlapped region[48]. Figure 10 shows the gate on drain overlap structure of DG TFET.

4. Conclusion

In this paper, the benefits of TFET over the conventional MOSFET are discussed in detail. Various device structures of TFET dealing with the performance enhancement such as higher I_{ON}, lower values of I_{OFF}, V_T and SS are investigated thoroughly. Hence TFETs are considered to be superior to that of MOSFETs and future work involves the designing of DG TFET with different materials to make it more suitable for RF/ analog or mixed signal circuit applications.

5. Acknowledgement

This work is supported by Department of Science and Technology, Government of India under SERB scheme (Grant No: SERB/F/2660).

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