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A computationally efficient finite state model predictive control for cascaded multilevel inverter

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Abstract This paper investigates a new scheme for Finite State Model Predictive Control fed five level Cascaded Multilevel Inverter. This proposed method uses 19 voltage vectors out of totally 125 voltage vectors of the Cascaded Multilevel inverter. Since this inverter has many switches, reducing the average switching frequency is the matter of great importance for high voltage applications, as they contribute to significant switching losses. Two schemes of Finite State Model Predictive Control (FSMPC) are proposed i.e. FSMPC1 employing the current control of the Cascaded Multilevel inverter with less (19) voltage vectors and FSMPC2 aiming the control of inverter load current as well as reducing the average switching frequency using 19 vectors. The performance of the proposed schemes is compared with conventional 61 voltage vector scheme of the Cascaded multilevel Inverter. The results show that both the proposed schemes perform well for steady state and dynamic operating conditions.

1. Introduction

Multilevel inverter (MLI) has become popular and attracted considerable interest in recent years. MLI includes a group of power semiconductor devices and capacitor as voltage sources generating a stepped voltage waveform which has reduced harmonic distortion. The various advantages of MLI are its capability of reducing voltage stress on power switches, dv/dt ratio and common mode voltage, thus increasing the quality of the output [1]. There are number of different topologies of MLI such as Cascaded MLI (CMLI), Diode Clamped MLI (DCMLI) and Flying Capacitor MLI (FCMLI). Out of which cascaded MLI has various advantages such as modularity, flexibility, extendibility and reliability. Cascaded MLI can also be realized by using a single Dc source instead of multiple separate DC sources [3]. Various other topologies of MLI have also been explored [2]. However they have various disadvantages such as increase in number of components such as diodes and capacitors and other problems such as maintaining the common mode voltage which complicates the controller.

MPC in recent years, has received significant attention and has gained popularity in the power electronics and drives

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community. MPC, developed for process control applications, in the 1970s, is used commonly in industry, with numerous applications reported [4]. The basic concept of all predictive control techniques is that decision of the controller is not centered on past state of system but on predicted behavior of the state variables and proper selection of the controlled variables either offline or online. MPC is also referred as receding horizon control, as where its main concept is to imitate an infinite prediction horizon by constantly sliding the prediction horizon. The recent developments and new trends in the area of MPC theoretical study and applications, are summarized in [5].

Even though the concept was simple, MPC was seldom used to control the power converters because of its computational complexity which was a burden to the processors. Therefore with the evolution of new high speed processor, the usage of MPC became a reality. In [6] the MPC is used to control a VSI, where a discrete-time model of VSI was used to predict the future value of the load current for all possible voltage vectors generated by the inverter. Since then, MPC has been used in various applications in power electronics such as controlling DC–DC converters [7], in matrix converters [8]. They are also used in the speed control of an induction motor [9] and Permanent magnet synchronous motor [10] where the model of the machine is based on a linearized state-space representation that describes the dynamics. Neural network based model predictive control has also been reported for improving power system dynamic performance over a wide range of operating conditions [11]. A multi-objective MPC (MOMPC) strategy for controlling VSI in high-power applications is presented in [12]. The various objectives used here along with optimizing current are reducing switching losses, controlling the real and reactive power, etc. The controller here uses the system model to predict the system behavior in each sampling interval for each voltage vector, and the most appropriate vector is then chosen according to an optimization criterion. The foresaid literatures show that MPC can be used effectively for a VSI. Even though the algorithm is effective, since filter is not used here, the THD of the output voltage is more as it is the inherent characteristics of a two level inverter.

Therefore MLIs have been considered for the MPC control in the place of VSI. MPC can be used to control MLI such as CMLI, DCMLI and FCMLI. In [13] a MPC controlled DCMLI has been proposed, where the DCMLI in addition to controlling the current has to incorporate an additional objective which is to maintain its common mode voltage constant, thus increasing the controller's complexity. In addition to this, the topology has more number of devices in the form of diodes. In [14], a FCMLI has been considered, where the topology has more number of flying capacitors. Even though this inverter has many advantage such as its modularity and the usage of lower number of voltage sources even for increased number of level, controlling the voltage of the capacitors increases the complexity of the controller. Therefore a CMLI is chosen in this paper as the inverter using MPC as the controller. Since for a five level inverter each phase has to generate five voltage levels, a five level inverter has 125 voltage vectors out of which many voltage vectors are redundant. 61 non-redundant voltage vectors have been used for the control algorithm in [15]. In applications requiring very high performance, the sampling time is often very small. In those
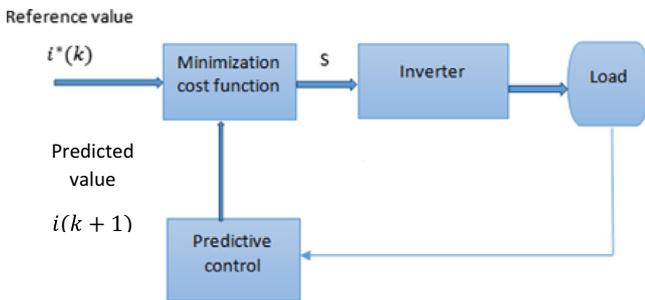

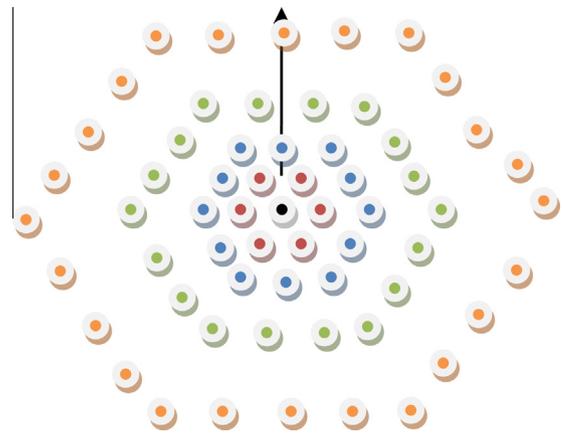**Figure 1**   Block diagram of the MPC controller.

Figure 3   Representation of the Switching states. The number of redundancies: 0•, 1•, 2•,3•, 4• for a 61 voltage vector scheme.
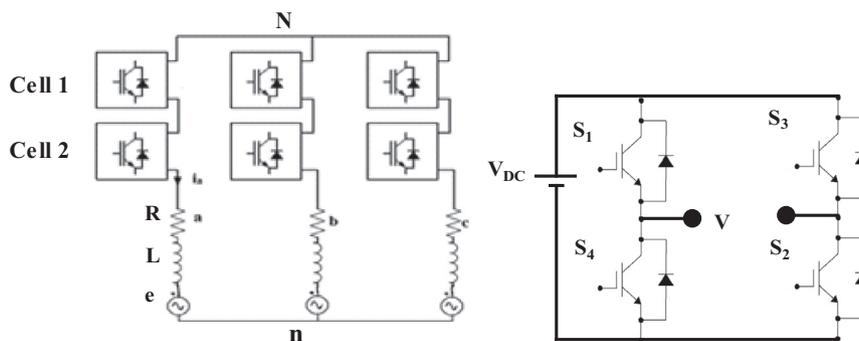

Figure 2   (a) Three phase cascaded H bridge inverter and (b) internal structure of a single cell.

situations, checking the prediction for all the 61 vectors in a very small sampling time becomes cumbersome. The proposed work here minimizes the voltage vectors further to 19 vectors for the control of the MLI, reducing the calculation burden of the controller.

This work has been divided as follows: Section 2 briefs about the MPC concepts followed by Section 3 which describes about the predictive current control of CMLI. Section 4 explains the proposed work and the results and discussion are described in Section 5. Finally Section 6 gives the conclusion.

2. Proposed work

A five level inverter has 125 voltage vectors. The large number of voltage vector increases the amount of calculation and therefore the burden of the processor. Since there may be delay because of this, the prediction horizon should also be increased. These problems can be minimized, if the number of the voltage vectors is reduced. In [15], the 125 voltage vec-

tors of a five level CMLI have been reduced to 61 by eliminating redundant voltage vectors and using only the 61 non-redundant voltage vectors. A comparison is made with 125 voltage vector scheme and is proved that the 61 voltage vector scheme works satisfactorily for a five level CMLI.

In this paper, a FSMPC technique that reduces the 61 voltage vectors to 19 voltage vectors is proposed. This reduces the amount of calculations in each sampling period without compromising on the performance of the CMLI, thus making it fit for application in a standard control platform. This technique can be implemented to any multilevel inverter with a higher levels and switching states. The following are the two cases proposed viz. FSMPC1 and FSMPC2.

2.1. Case 1

Here, the proposed FSMPC1 fed five level CMLI aims to control the inverter load current using a reduced number of voltage vectors i.e. 19 vectors. This method is compared with the
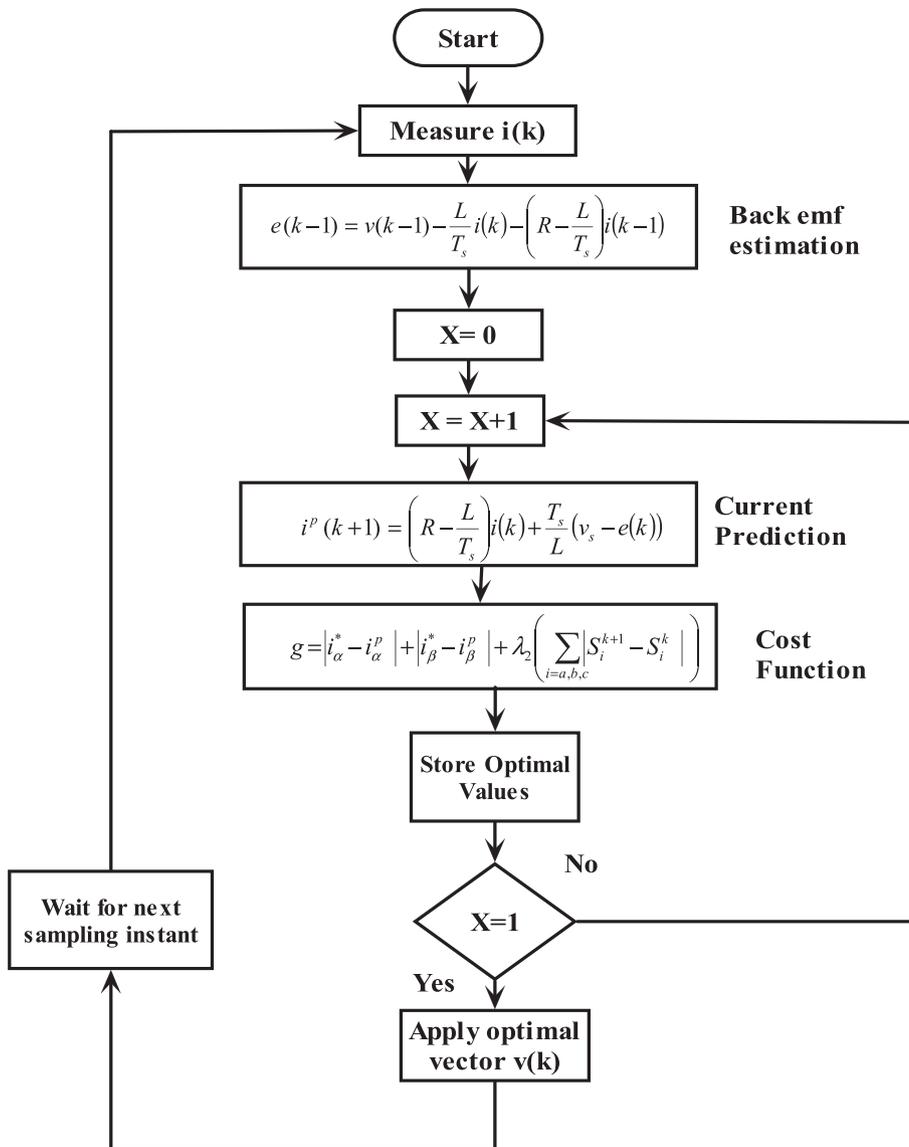

Start

Measure i(k)

$$e(k-1) = v(k-1) - \frac{L}{T_s} i(k) - \left(R - \frac{L}{T_s} \right) i(k-1)$$ **Back emf estimation**

X = 0

X = X+1

$$i^p(k+1) = \left(R - \frac{L}{T_s} \right) i(k) + \frac{T_s}{L} (v_s - e(k))$$ **Current Prediction**

$$g = \left| i_\alpha^* - i_\alpha^p \right| + \left| i_\beta^* - i_\beta^p \right| + \lambda_2 \left(\sum_{i=a,b,c} \left| S_i^{k+1} - S_i^k \right| \right)$$ **Cost Function**

Store Optimal Values

Wait for next sampling instant

X=1   No

Yes

Apply optimal vector v(k)

Figure 4 Flowchart for FSMPC2 scheme.

standard 61 voltage vector scheme. The results show that this MPC is very effective in reducing the harmonics in the current and while there is a step change in the reference current and therefore shows an excellent steady state and dynamic response.

2.2. Case 2

The proposed FSMPC2, controls the same CMLI with 19 voltage vectors mainly reduces the average switching frequency, which is done by including this in the cost function. Thus, FSMPC2 in addition to controlling the inverter output current reduces the average switching frequency and therefore the switching losses. These objectives are achieved using 19 switching states and thus reducing the calculation complexity and the computational burden of the processor for each sampling time. This scheme is compared to the 61 vector scheme which also includes the reduction in average switching frequency as its second objective.

3. Model predictive control

Predictive control presents a group of controllers that have found a forefront position nowadays in power converters. A classification for different predictive control methods is deadbeat based controllers, hysteresis based controllers, trajectory based controllers and MPC. Out of which MPC is advantageous comparatively because of its lower complexity, ability to perform online optimization and the absence of the modulator stage [16]. MPC uses the system model for the variable prediction, until a time in the horizon by taking the actual or optimal actuations by the cost function minimization. Due to the wide range of advantages such as intuition, inclusion of the multi variables, and constraints, the designing quality of the model has an influence on the controller.

The basic ideas of MPC are as follows: building a model for prediction, representing the required behavior of the system using cost function and minimizing this cost function to produce the actual command [17]. The main advantage lies in control of the various variables at the same time including the restrictions. This is especially important because, here we are dealing with units of different kind and magnitude of variables that are getting controlled.

The discrete time model of the MPC using the state space model is

$$x(k + 1) = Ax(k) + Bu(k) \tag{1}$$
$$y(k) = Cx(k) + Du(K) \tag{2}$$

where x, u, and y denote, the state, input, and output variables. Eq. (3) defines the cost function of the system denoted by J in such a way the behavior of entire system is described taking the references, future states and their actuations into account as well as the error between the predicted and the reference variables such as power error [18], torque error and in this case load current error.

$$J = f(x(k), u(k), \ldots, u(k + N)) \tag{3}$$
$$u(k) = [1\,0\ldots\ldots0] argmin_u J \tag{4}$$

where J denotes the cost function of MPC problem. Since the MPC is an optimization problem and in each sampling instant the problem is solved using the updated data and a sequence of new actuations each time. Using the system model and the data until the time k the prediction can be up to $k + N$ in the horizon of time. The process is repeated with measured data each time (see Figs. 1 and 4).

4. Predictive current control for a CMLI

A five level CMLI shown in Fig. 2 has 2 cells in each phase [19]. Each cell is fed from separate DC voltage source and will generate a 5 level output voltage. If a CMLI contains X cells and L levels, then a L level CMLI will have X^L number of voltage vectors. So a five level CMLI contains 125 voltage vectors [20].

The MPC algorithm for a CMLI works was explained below:

- The value of the reference current i^* is obtained from the outer control loop and the load current i^m measured in the discrete domain.

Table 1 Voltage level, its corresponding voltage vectors and non-redundant vectors.

Cell	Total number of voltage vectors	Non-redundant voltage vectors	Voltage vectors in the proposed method
2	125	61	19
X	$(2X + 1)^3$	$12X^2 + 6X + 1$	$4X^2 + 3$

Table 2 19 Voltage vectors of the proposed FSMPC.

S. no.	Voltage vectors	Voltage levels	S. no.	Voltage vectors	Voltage levels
1	$v0 = (2 + 1.1547j)^* V_{dc}$	[4 2 4]	10	$v9 = (2.3094j)^* V_{dc}$	[2 4 0]
2	$v1 = 2^* V_{dc}$	[4 1 1]	11	$v10 = (1.1574j)^* V_{dc}$	[2 3 1]
3	$v2 = (2{-}1.1547j)^* V_{dc}$	[4 0 2]	12	$v11 = (-1.1547j)^* V_{dc}$	[2 1 3]
4	$v3 = (1{-}0.5774j)^* V_{dc}$	[3 2 1]	13	$v12 = (-1 + 0.5774j)^* V_{dc}$	[1 3 2]
5	$v4 = (1 + 0.5774j)^* V_{dc}$	[3 2 1]	14	$v13 = (-1{-}0.5774j)^* V_{dc}$	[1 2 3]
6	$v5 = (1{-}1.732j)^* V_{dc}$	[3 0 3]	15	$v14 = (-1 + 1.732j)^* V_{dc}$	[1 4 1]
7	$v6 = (1 + 1.732j)^* V_{dc}$	[3 3 0]	16	$v15 = (-1{-}1.732j)^* V_{dc}$	[1 1 4]
8	$v7 = 0$;	[2 2 2]	17	$v16 = (-2{-}1.1547j)^* V_{dc}$	[0 2 4]
9	$v8 = (-2.3094j)^* V_{dc}$	[2 0 4]	18	$v17 = (-2^* V_{dc})$	[0 3 3]
			19	$v18 = (-2 + 1.1547j)^* V_{dc}$	[0 4 2]

Table 3 Simulation parameters.

Variable	Description	Value
X	Cells per phase	2
R_L	Load resistance	10 (Ω)
L_L	Load inductance	20 (mH)
T_s	Sample time for predictive control	40 (μs)
V_{dc}	Input DC voltage	400 (V)
I_{ref}	Reference current amplitude and frequency	50 (A), 50 (Hz)

(a)

(b)
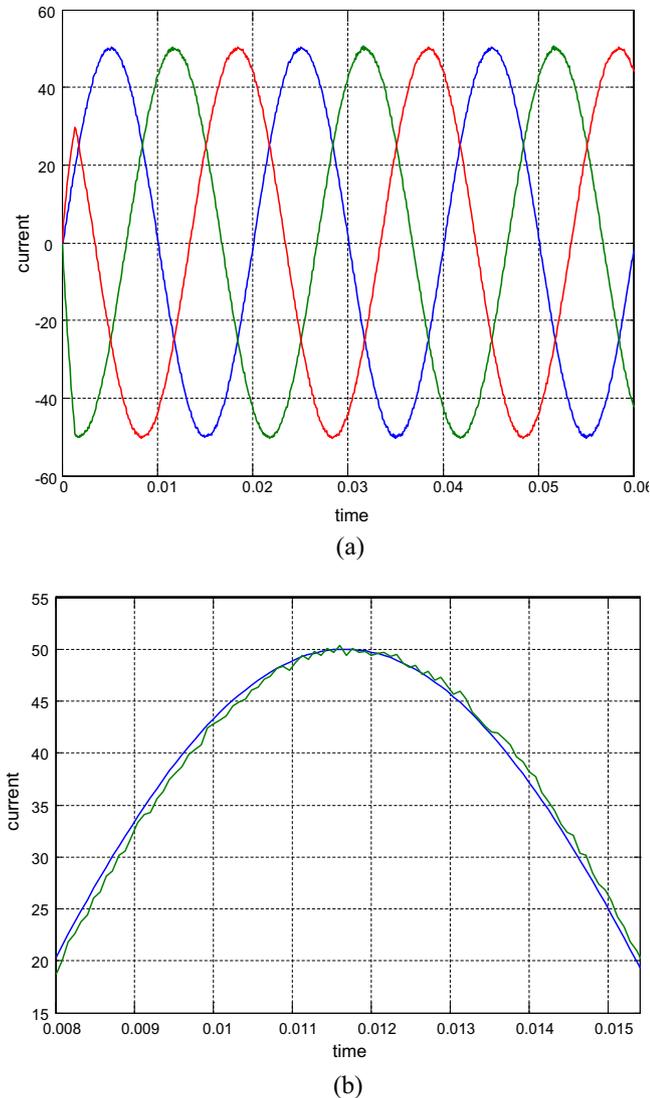
Figure 5 Results for FSMPC1 scheme for 61 vectors: (a) output current and (b) enlarged view of the output current.

- The load current $i(k + 1)$ is predicted in the next sampling instant for different voltage vectors using the model of the system.
- The cost function J is evaluated for all the current errors generated between the reference and the predicted currents.

(a)

(b)
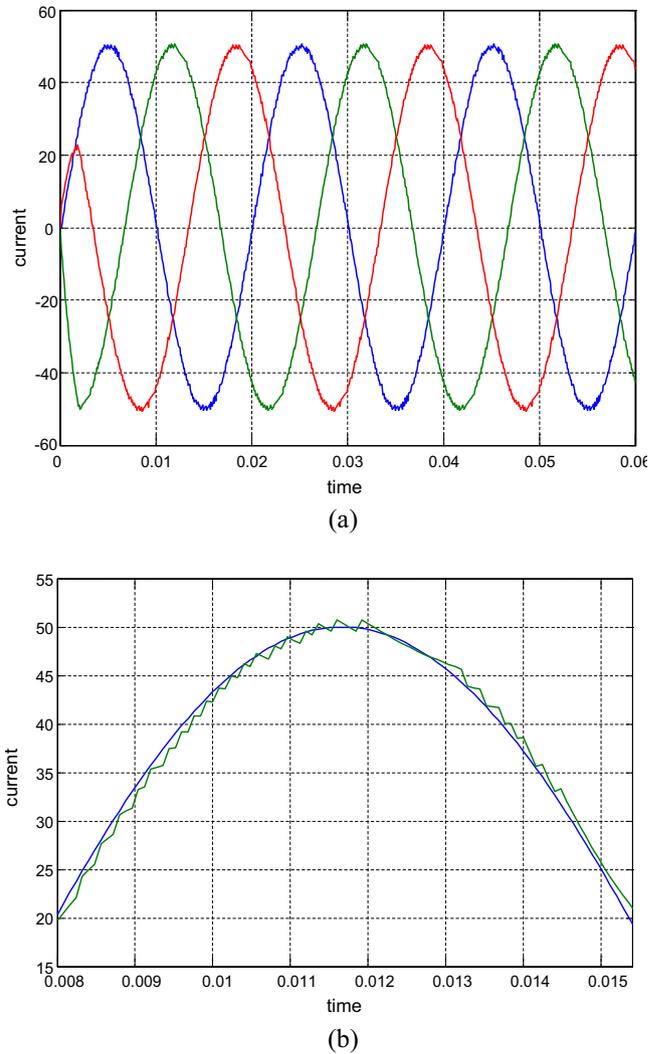
Figure 6 Results for FSMPC1 scheme for 19 vectors: (a) output current and (b) enlarged view of the output current.

- The error value that minimizes the cost function J, is selected and its corresponding voltage vectors and its corresponding switching states are given to the inverter.
- The inverter now implements this switching state, and produces the desired current.
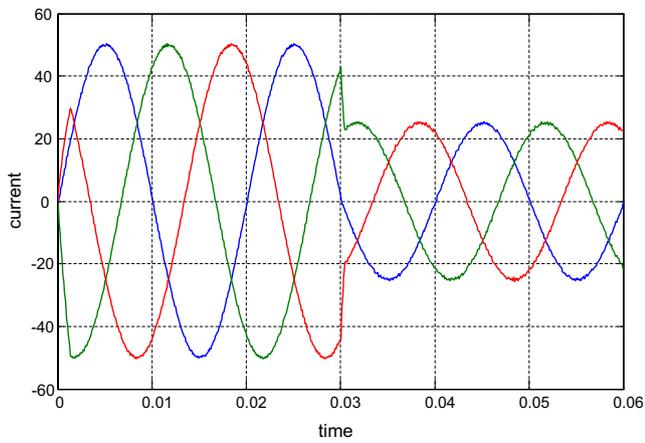
4.1. System model

The inverter modeling is based on the output levels

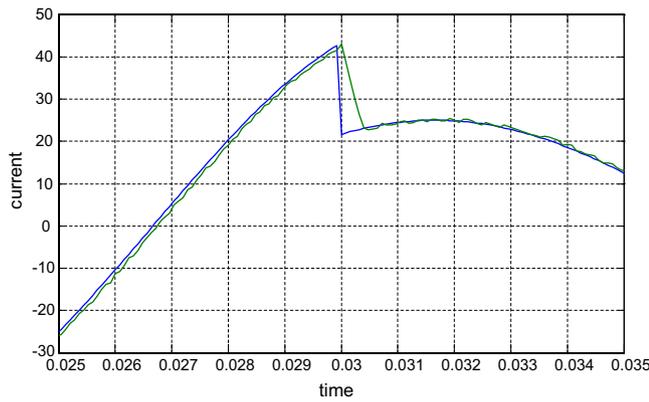$$v_{an}(t) = v_{aN}(t) + v_{Nn}(t) \tag{5}$$

where v_{aN} is the inverter output voltage of phase a, and v_{Nn} is the common-mode voltage, defined in terms of the inverter voltages as

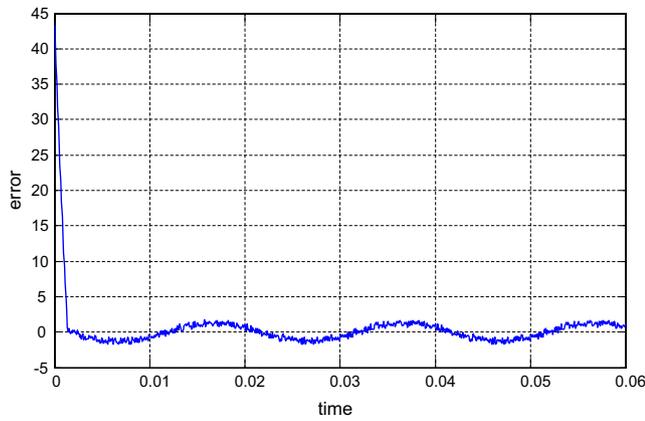$$v_{Nn}(t) = \frac{v_{aN}(t) + v_{bN}(t) + v_{cN}(t)}{3} \tag{6}$$
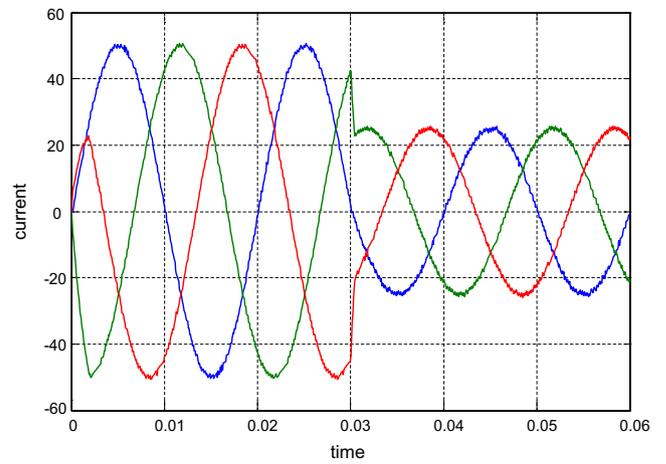
The load model is as follows

(a)

(b)

(c)

Figure 7 Results for (a) output current for a step change in reference, (b) enlarged view of the output current, and (c) current error for 61 vector scheme.
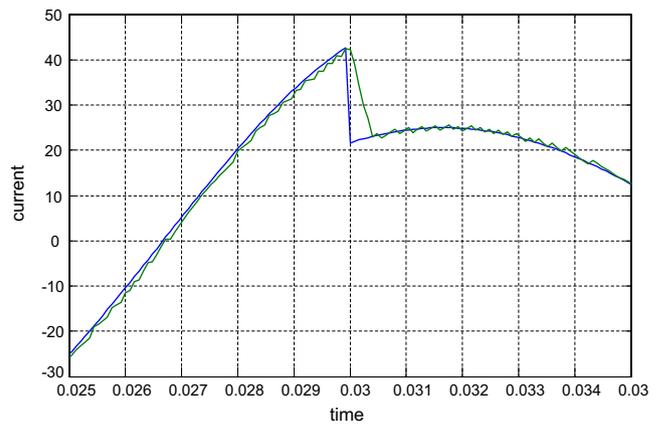
$$v_{an} = L\frac{di_a}{dt} + Ri_a + e_a \qquad (7)$$
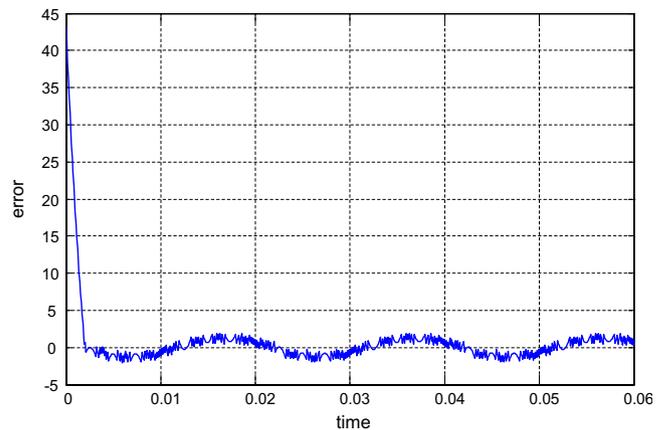
$$v_{bn} = L\frac{di_b}{dt} + Ri_b + e_b \qquad (8)$$

$$v_{cn} = L\frac{di_c}{dt} + Ri_c + e_c \qquad (9)$$

(a)

(b)

(c)

Figure 8 Results for (a) output current for a step change in reference, (b) enlarged view of the output current, and (c) current error for 19 vector scheme.

By applying the Laplace transform to the above equations transfer functions from voltage to current at the R_L load are obtained:

$$\frac{I_a}{V_{an} - E_a} = \frac{1}{Ls + R} \tag{10}$$

$$\frac{I_a}{V_{bn} - E_b} = \frac{1}{Ls + R} \tag{11}$$

$$\frac{I_a}{V_{cn} - E_c} = \frac{1}{Ls + R} \tag{12}$$

For generating the voltage vectors we use the state space analysis in order to find the predictive value of the current

$$a = e^{j2\pi/3} = -\frac{1}{2} + j\frac{\sqrt{3}}{2} \tag{13}$$

$$v = \frac{2}{3}(v_{aN} + v_{bN} + v_{cN}) \tag{14}$$

$$v_{aN} = s_a * V_{dc} \tag{15}$$

$$v_{bN} = s_b * V_{dc} \tag{16}$$

$$v_{cN} = s_c * V_{dc} \tag{17}$$

For example, for switching state $(S_a, S_b, S_c) = (0, 0, 0)$ generates voltage vector V_0 defined as

$$v_0 = \frac{2}{3}(0 + a0 + a^2 0) = 0 \tag{18}$$

Calculation of all 125 vectors for each instant will be burden for the controller instead of calculating all the 125 vectors by removing the residues we will get 61 voltage vectors among (Receding horizon principle) [5]. Those 61 vectors are represented in the hexagon given below.

Fig. 3 shows the 61 voltage vectors for a five level CMLI. This voltage vectors are plotted in real and imaginary axis calculated based on the redundancy of the vectors.

In the hexagon, switching states which are in the inner most layer (•) have one switching state and therefore represent the redundancy value equal to 4. The layer outer to it (•) has 6 switching states and has the redundancy equal to 3. The next layer (•) has the switching states having the redundancy equal to 2. The layer outer (•) to it and the outermost layer (•) have the redundancy equivalent to 1 and 0 respectively.

5. Predictive controller with reduced computation

The number of voltage vectors for the proposed method is deduced through the switching states where we get the algebraic sum of all three phases equal to zero. For example consider a phase for 5- level inverter having voltage $2V_{dc}$ i.e. $V_a = 2V_{dc}$ and if the sum of the voltages of remaining two vectors should be equal to $-2V_{dc}$ i.e. $V_b + V_c = -2V_{dc}$ such that voltage balance occurs which is shown in Eq. (19)

$$V_a + V_b + V_c = 0 \tag{19}$$

The switching states corresponding to these voltage vectors are chosen. The inverter operates for these 19 switching states. Therefore 19 such vectors are chosen this proposed work. Table 1 gives the details about the voltage levels and its corresponding redundant and non-redundant vectors. It also shows the number of voltage vector for our proposed method.

All the 19 voltage vectors used for this work for a five level CMLI are shown in Table 2. It shows the detailed description of each of the 19 voltage vectors and its corresponding voltage levels.
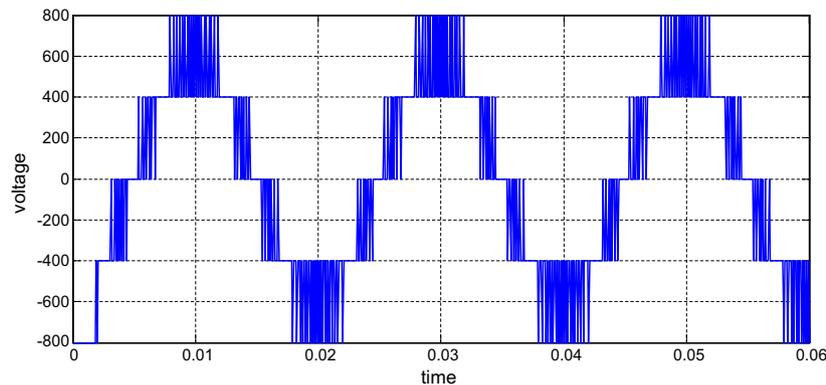

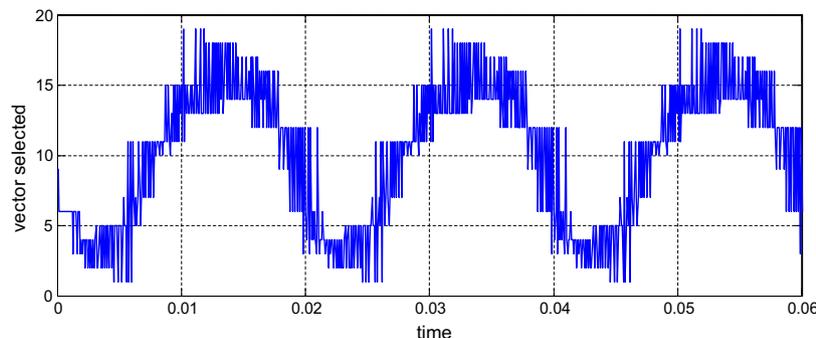**Figure 9** Output voltage of inverter for FSMPC1 scheme.

Figure 10 Selection of 19 voltage vectors for various sampling time (FSMPC1).

5.1. Case 1

In this case, the cost function (J) aims at achieving the control of the inverter load current using the above mentioned 19 vectors. The cost shown in Eq. (20) includes this objective. Cost function for the current control of the inverter is given by

$$J = |i^*_\alpha(k+1) - i^p_\alpha(k+1)| + |i^*_\beta(k+1) - i^p_\beta(k+1)| \qquad (20)$$

where $i^p_\alpha(k+1)$, $i^p_\beta(k+1)$ are the real and imaginary parts of the predicted load current vector $i^p(k+1)$, $i^*_\alpha(k+1)$, $i^*_\beta(k+1)$ are the real and imaginary parts of the reference currents. The current prediction can be done through the Euler equation

$$\frac{di}{dt} = \frac{i(k+1) - i(k)}{T_s} \qquad (21)$$

so the predicted current is as follows

$$i^p(k+1) = (1 - (RT_s)/L)i(k) + T_s/L(v(k) - \hat{e}(k)) \qquad (22)$$

where R is the load resistance, L is the inductance, T_S is the sampling time, $\hat{e}$ represents the back EMF

For every sampling time, the controllers calculates the values of all the 19 vectors and the switching states will be changed, such that the vector which is having minimum error and its corresponding switching state causing it will be fed as the input switching states to the inverter for that sampling. The
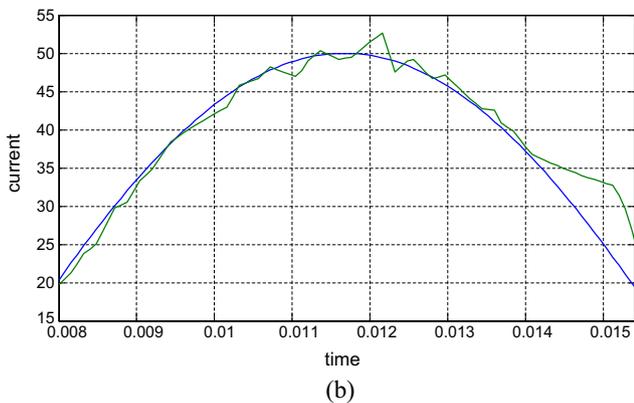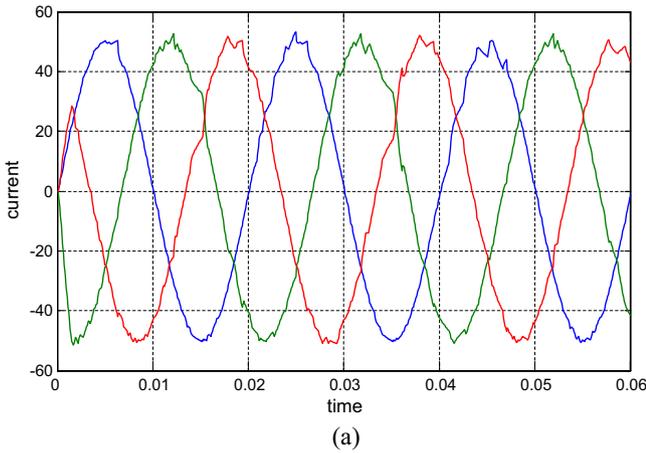
system is simulated for the sampling time of 40 µs, inductance of 20 mH, resistance of 100 Ω and source voltage of 300 V.

5.2. Case 2

In this case, the cost function aims at achieving two objectives viz., controlling the load current and reducing the average switching frequency. The cost shown in Eq. (20) includes only the objective of controlling current. The new objective function for this case is as follows:

$$J = \left|i^*_\alpha(k+1) - i^p_\alpha(k+1)\right| + \left|i^*_\beta(k+1) - i^p_\beta(k+1)\right|$$
$$+ \lambda_2 \left(\sum_{i=a,b,c} \left|S^{k+1}_i - S^k_i\right| \right) \qquad (23)$$

where S^k_i and S^{k+1}_i denote the switching state of phase i ($i = a$, b, c) in the current sampling time (between kth and $(k+1)$th sampling instant) and the subsequent sampling time (between $(k+1)$th and $(k+2)$th sampling instant), respectively. $S^k_i = 0$ or 1, where 0 means that the top switch is off and the lower switch is on, and for 1 it is just the opposite.
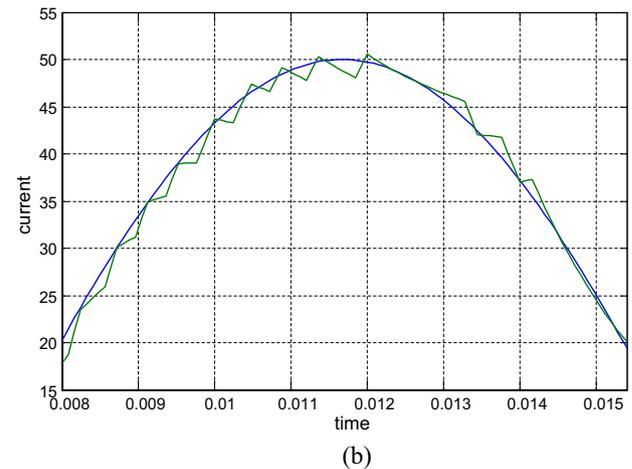

Figure 11 Results for FSMPC2 scheme for 61 vectors: (a) output current and (b) enlarged view of the output current.
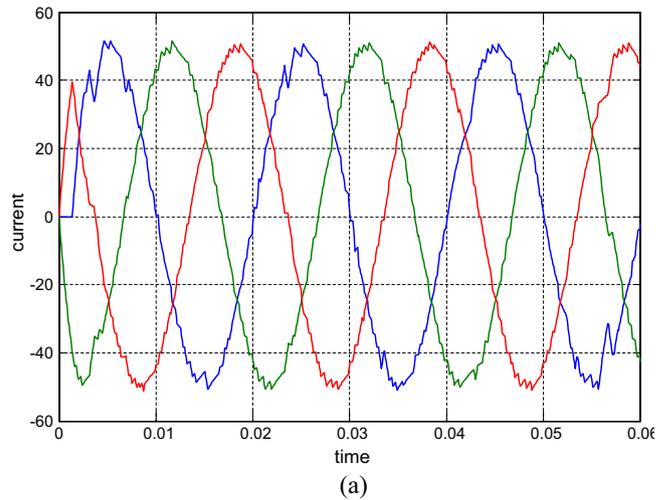

Figure 12 Results for FSMPC2 scheme for 19 vectors: (a) output current and (b) enlarged view of the output current.

For instance, supposing that the voltage vector 1 $V_1(1\,0\,0)$ is applied at the present sampling period and V $3(0\,1\,0)$ at the next sampling period, then one obtains $S_a^k = 1$, $S_b^k = 0$, $S_c^k == 0$; $S_a^{k+1} = 0$, $S_b^{k+1} = 1$, and $S_c^{k+1} = 0$. Consequently, according to the second term of the cost function in Eq. (23), the total commutation instants of the switch, C can be obtained in this way, as $C = |1-0| + |0-1| + |0-0| = 2$. The second term contributes to switching frequency reduction and λ_2 is the weighting factor for second objective. Here the

value of λ_2 is taken as 0.7, so that higher priority is given to the current control. A large value for the weighting factor λ_2 implies a higher priority for this objective. The cost function uses only 19 vectors for the computations in each sampling time reducing the computation time and in turn the effort taken by the processor. Table 3 gives the simulation parameters that are used for this work.
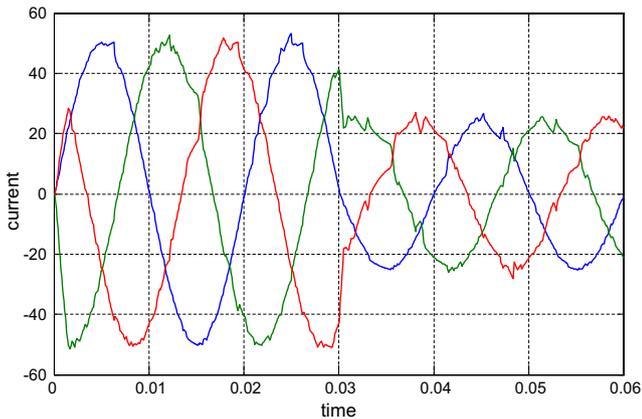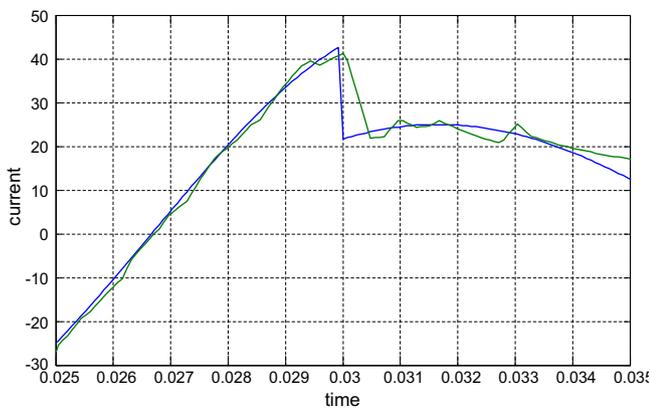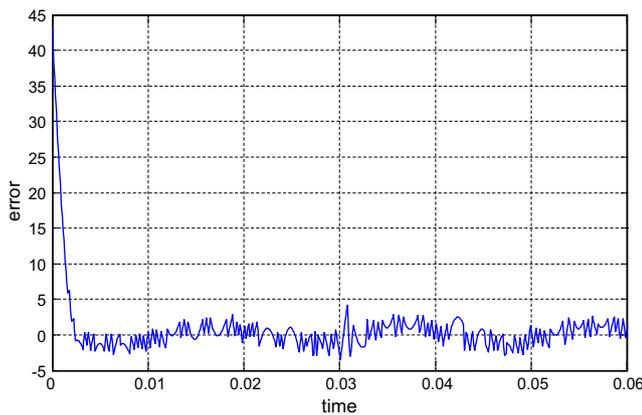
Figure 13   Results for (a) output current for a step change in reference, (b) enlarged view of the output current, and (c) current error for 61 vector scheme.
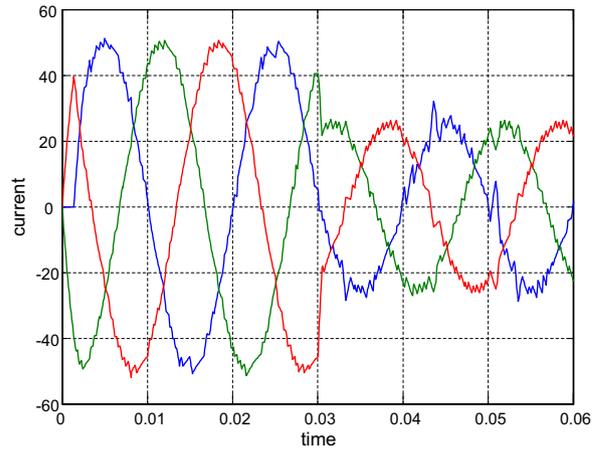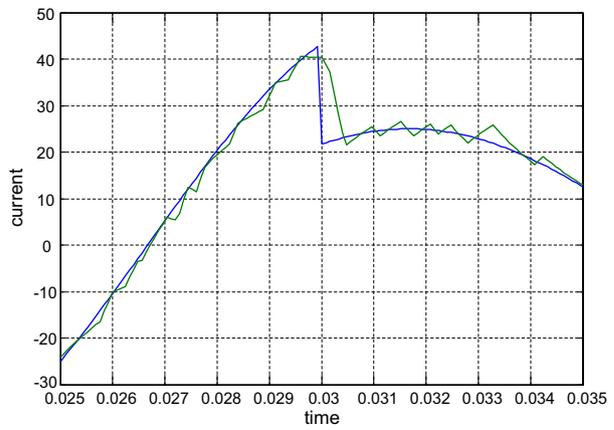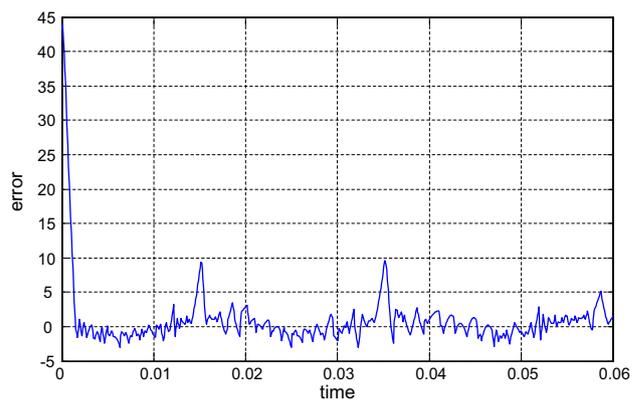

Figure 14   Results for (a) output current for a step change in reference, (b) enlarged view of the output current, and (c) current error for 19 vector scheme.

6. Results and discussion

6.1. FSMPC1

Simulations of a 2-cell 3-phase CHB inverter with a R_L load were carried out using MATLAB/Simulink, using the parameters listed in Table 3. The simulation was carried out in core i5 4200U CPU@1.6 GHz processor. These simulations compare the proposed FSMPC control scheme having 19 inverter voltage vectors and inverter having 61 voltage vectors. Figs. 5 and 6(a) and (b) show the output currents for all the three phases, enlarged view of a section of load current showing the tracking of the predicted current with the reference current, for both the 61 voltage vectors and 19 voltage vectors respectively. It is seen that the output current shows a THD of 1.46% and 2.69% respectively for both the cases. The 19 vector Model of the MPC has the THD slightly more, but well within the IEEE standards.

The ability to respond fast to the dynamic step change in reference current has always been a merit of MPC which is shown in Figs. 7 and 8a and its enlarged view shown in Figs. 7 and 8b. Here it is seen that the proposed methods show very small and insignificant lag when compared to the conventional scheme. Figs. 7 and 8c shows the error of the predicted load current and the reference current, which when compared between the two schemes depicts that 19 vector scheme has more error but is very negligible. So, these are some trade-offs, which are affordable since they are well within the limits.

Fig. 9 shows the phase load voltage of the proposed FSMPC1 control algorithm for 19 vectors.

Fig. 10 shows change in switching frequency with respect to time. This is seen from the variation of the voltage vector (1–19) and time which shows that the switching frequency to be more in FSMPC1. If this inverter is used for high voltage applications the switching losses would be more. The results of the proposed FSMPC1 indicate that inverter works really well for steady state as well as dynamic changes with the quality of current to be exceptionally good.

6.2. FSMPC2

This FSMPC2 includes the reduction in switching frequency as the second objective in the cost function in addition to the current control. Figs. 11 and 12 depict the inverter output current, its enlarged view showing the tracking of predicted current with its reference current, for 61 vector scheme as well as 19 vector scheme.

Table 4   THD analysis of the output current waveforms.

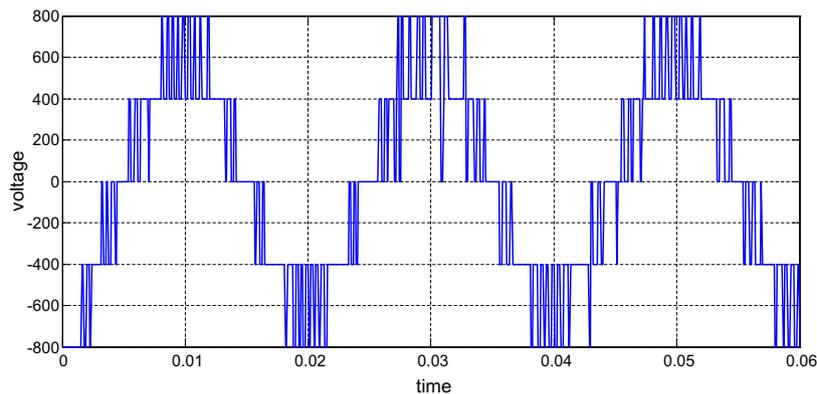| Scheme	61 Vectors (%)	19 Vectors (%)
FSMPC1	1.46	2.65
FSMPC2	2.12	3.47

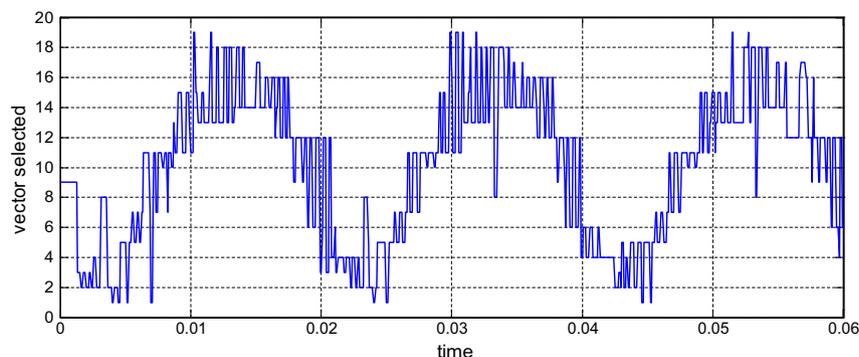**Figure 15**   Output voltage of inverter for FSMPC2.

Figure 16   Selection of 19 voltage vectors for various sampling time (FSMPC2).

The results show that the switching frequency of the inverter is reduced to half without significantly affecting the performance, when THD of the current is found to be 2.12% for 61 vector scheme and 3.47% for the 19 vector scheme. Even though the THD of the 19 vector scheme is more, our objective of reducing the average switching frequency is served.

Figs. 13 and 14(a)–(c) show the response of the output current for dynamic changes. It is seen that the inverter adapts itself quickly. Even though the lag of 19 vector scheme is a bit more than the same for 61 vectors, it's an affordable trade-off, since these values are well within the IEEE standards. Fig. 15 depicts inverter output voltage of the 19 vector scheme.

Fig. 16 shows the voltage vector variation with respect to time for FSMPC2 scheme. When comparing Figs. 10 and 16, it is seen that the average switching frequency for FSMPC2 has been considerably reduced (halved). Based on these results, on comparing the results of 61 vector scheme and 19 vector scheme, it can be decided that the FSMPC2 performs well in steady state as well as dynamic condition. These are obtained even though there is a slight change in the objective function. Table 4 shows the percentage of THD of the output current waveform for 61 vectors and 19 vectors for both the schemes.

61 vector scheme takes about 50 μs for the execution of the algorithm whereas the 19 vector scheme execute in about 27 μs. By using the 19 vector scheme the execution time of both the FSMPC1 and FSMPC2 algorithm reduces to about half the time of the 61 vector scheme.

7. Conclusion

In this work, a computationally efficient FSMPC for a five level CMLI is proposed. The main contribution of this paper is to make the MPC controller work using only 19 voltage vectors in place of conventional 61 voltage vectors for a five level CMLI. This simplifies the execution of the MPC algorithm, paving a way for significant reduction in the computational time. This is achieved by considering two cases namely FSMPC1 and FSMPC2. The first case takes only the control of current as the objective for which the results obtained show an exceptional steady state and dynamic performances. The second case discussed makes use of the excellent ability of MPC to multitask, by adding one more objective which is to reduce the average switching frequency in addition to controlling the load current. This is especially important, since switching losses and therefore switching frequency is significant for high-power applications. The trade-off of this MPC is that the current is distorted, but well within the limits of IEEE standards. The results shown prove that this MPC works well in steady state and dynamic conditions too. Therefore in scenarios where faster computation is required, we can use the FSMPC1 and in applications where the inverter is used for high power rating, the FSMPC2 is used. The work can be further extended to incorporate various other objectives in MPC algorithm.

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